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WT32

DATA SHEET

Tuesday, 25 August 2009

Version 1.5

bluegiga

VERSION HISTORY

Version	Comment
0.992	New images added
0.991	Missing pin added to recommended land pattern design
0.99	Microphone biasing recommendation fixed. Voltage regulator enable pin description added. Some small fixes. Layout guidelines for the audio traces added.
0.98	Version history added. Microphone biasing recommendations specified. Package information added. Pinout AIO0 and AIO1 fixed.
0.97	VREG_ENA pin added to the production version of the module Layout recommendations added
0.98	Fixed cross references
1.0	Soldering recommendations added. Layout guide fixed. Details at VREG_ENA. Operating temperature range fixed.
1.1	Bluetooth and FCC qualification IDs added
1.2	Figure 18 fixed. Recommendation for external ESD protection removed.
1.3	Changed VREG_ANA to VREG_ENA
1.4	Radiocharacteristics updated
1.5	List of pretested antennas added

TABLE OF CONTENTS

DESCRIPTION:

WT32 is the latest generation of Bluetooth modules. It provides highest level of integration with integrated 2.4GHz radio, DSP, battery charger, stereo codec, and antenna ready to hit mono and stereo audio applications. WT32 is also ready to support the latest Bluetooth 2.1 standard.

The embedded DSP core allows enhancement of the product with features such as advanced audio decoding (MP3, AAC, AAC+), echo cancellation, noise reduction, and data manipulation.

Bluegiga's flexible iWRAP firmware enables device manufacturers to easily add wireless, secure, and standard-based Bluetooth connectivity into new or existing applications with very limited development and manufacturing effort. WT32 is Bluetooth End Product, CE and FCC certified meaning that OEMs do not need to apply any additional certifications.

APPLICATIONS:

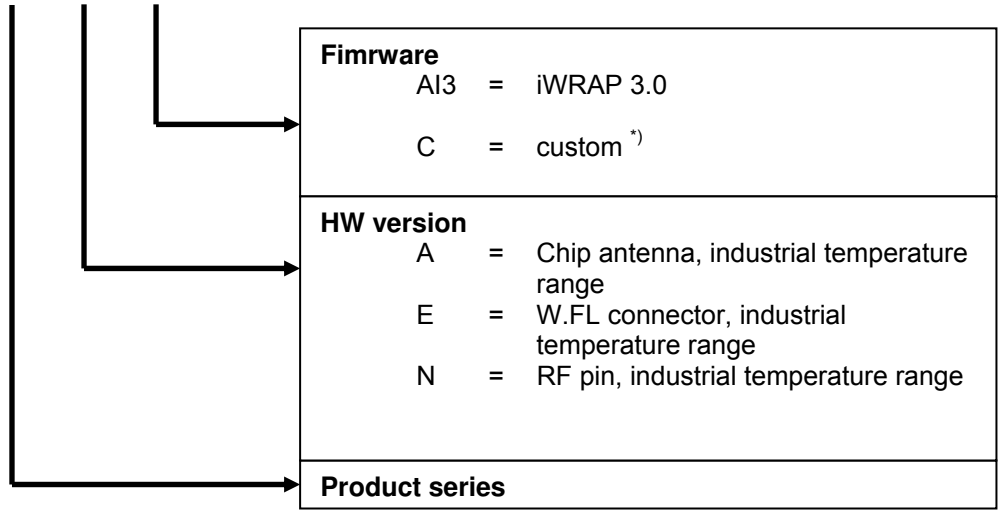
- High quality wireless stereo headsets
- Wireless mono headsets
- Wireless speakers
- USB multimedia dongles
- MP3 players
- VoIP handsets
- Hands-free car kits

FEATURES:

- Plug n' Play Bluetooth Solution for Mono and Stereo Audio Solutions
- Integrated DSP, Stereo Codec, and Battery Charger
- Integrated Antenna and W.FL Connector
- Bluetooth 2.0 Compliant and Bluetooth 2.1 Ready
- Bluetooth End Product, CE and FCC Qualified
- Class 2 - Range up to 30 Meters
- Industrial Temperature Range from -40C to +85C
- Low Power Consumption
- iWRAP™ Firmware for Controlling Connections and Configuring Settings
- Supported Bluetooth Profiles: A2DP, AVRCP, HFP, HFP-AG, SPP, OPP and HID

1 Ordering Information

WT32-A-AI



**) Custom firmware refers to any standard firmware with custom parameters (like UART baud rate), custom firmware developed by customer, or custom firmware developed by Bluegiga for the customer. To order custom firmware, you must have a properly filled Custom Firmware Order Form and a unique ordering code issued by Bluegiga.*

Contact support@bluegiga.com for more information.

2 Block Diagram and Descriptions

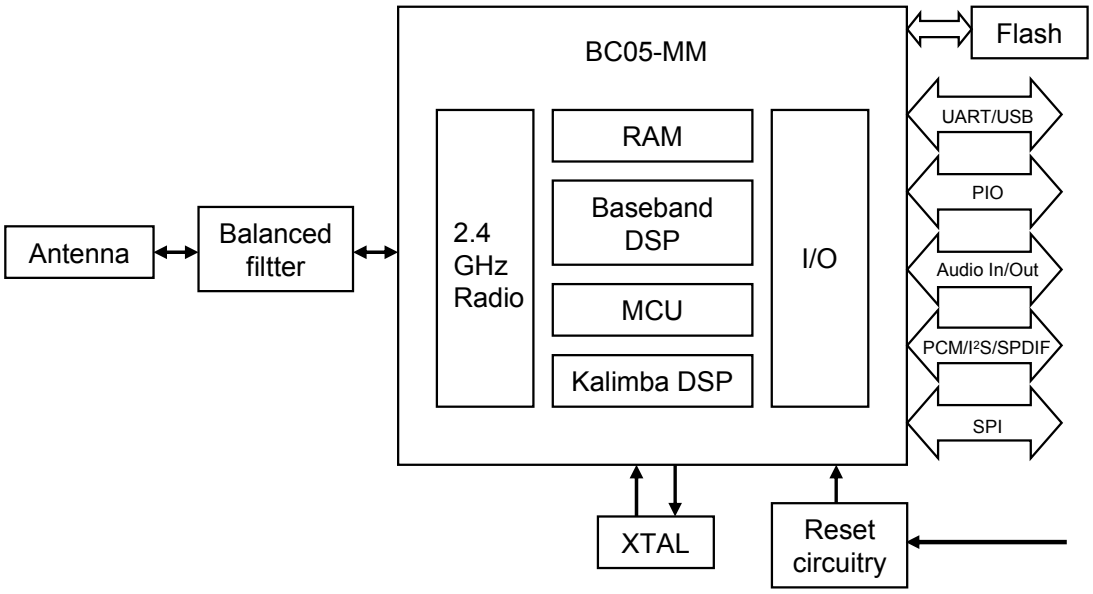


Figure 1: Block diagram of WT32

BC05-MM

The BlueCore05-MM is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems. It provides a fully compliant Bluetooth system to v2.0+EDR of the specification for data and voice.

BlueCore05-MM contains the Kalimba DSP co-processor with double the MIPS of BlueCore03-MM, supporting enhanced audio applications. BlueCore05-MM integrates a 16-bit stereo codec and it has a fully differential audio interface with a low noise microphone bias.

Crystal

The crystal oscillates at 26MHz.

Flash

Flash memory is used for storing the Bluetooth protocol stack and Virtual Machine applications. It can also be used as an optional external RAM for memory-intensive applications.

Balanced Filter

Combined balun and filter changes the balanced input/output signal of the module to unbalanced signal of the antenna. The filter is a band pass filter (ISM band).

Antenna

WT32 uses ceramic chip antenna with high dielectric constant, which makes the antenna very insensitive to surrounding environment and thus gives high design freedom around the antenna.

USB

The USB interface is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. WT32 acts as a USB peripheral, responding to requests from a Master host controller such as a Personal Computer (PC).

Synchronous Serial Interface

This interface is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

UART

This interface is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

PCM / I^2S / SPDIF Interface

This interface is a bi-directional serial programmable audio interface supporting PCM, I2S and SPDIF formats.

Audio Interface

The audio interface of WT32 has fully differential inputs and outputs and a microphone bias output. A high-quality stereo audio Bluetooth application can be implemented with minimum amount of external components.

Programmable I/O

WT32 has a total of 10 digital programmable I/O terminals. These are controlled by the firmware running on the device.

Reset

WT32 has a reset circuitry that is used to reset the module in the startup to ensure proper operation of the flash memory. Alternatively, the reset can be externally driven by using a WT32 reset pin.

802.11 Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH (Adaptive Frequency Hopping), priority signaling, channel signaling, and host passing of channel instructions are all supported. The features are configured in firmware. Since the details of some methods are proprietary (e.g. Intel WCS), please contact Bluegiga Technologies for details.

3 Electrical Characteristics

Absolute maximum ratings

	Min	Max	Unit
Storage temperature	-40	85	°C
Operating temperature	-30	85	°C
VDD_IO	-0.4	3.6	V
VDD_BAT	-0.4	4.4	V
VDD_CHG	-0.4	6.5	V
Terminal voltages	-0.4	Vdd + 0,4	V
Output current from PIOs		TBD	mA

The module should not continuously run under these conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Table 1: Absolute maximum ratings

Recommended operating conditions

	Min	Max	Unit
Operating temperature	-40	85	°C
VDD_IO	1.7	3.6	V
VDD_BAT	2.5	4.4	V
VDD_CHG	0	6.5	V
Terminal voltages	0	Vdd	V

Table 2: Recommended operating conditions

Terminal characteristics

	Min	Typ	Max	Unit
I/O voltage levels				
V_{IL} input logic level low	-0.4	-	0.25xVDD	V
V_{IH} input logic level high	0.625xVDD	-	Vdd + 0.3	V
V_{OL} output logic level low	0	-	0.125	V
V_{OH} output logic level high	0.75xVDD	-	VDD	V
Reset terminal				
$V_{TH,res}$ threshold voltage	0.64	0.85	1.5	V
R_{IRES} input resistance		220		kΩ
C_{IRES} input capacitance		220		nF
Input and tri-state current with				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	10	40	100	µA
Weak pull-up	-5	-1	-0.2	µA
Weak pull-down	0.2	1	5	µA
I/O pad leakage current	-1	0	1	µA
LED driver pad				
Off current	-	1	2	µA
On resistance (V_{PAD} < 0.5 V)	-	20	33	Ω
On resistance, pad enabled by battery charger (V_{PAD} < 0.5 V)	-	20	50	Ω

Table 3: Terminal characteristics

Battery charger

Battery charger		Min	Typ	Max	Unit
VDD_CHG		4.5	-	6.5	V
Charging mode (VDD_BAT rising to 4.2 V)					
Supply current [a]		-	4.5	6	mA
Battery trickle charge current [b] [c]	Maximum setting	-	14	-	mA
	Minimum setting	-	4	-	mA
Maximum battery fast charge current [d] [c]	Headroom > 0.7 V [e]	-	140	-	mA
	Headroom = 0.3 V	-	120	-	mA
Maximum battery fast charge current [d] [c]	Headroom > 0.7 V	-	40	-	mA
	Headroom = 0.3 V	-	35	-	mA
Trickle charge voltage threshold		-	2.9	-	V
Float voltage (with correct trim value set), V_{FLOAT} [f]		4.17	4.2	4.23	V
Float voltage trim step size [f]		-	50	-	mV
Battery charge termination current, as a percentage of the fast charge current		5	10	20	%
Standby Mode (BAT_P falling from 4.2V)					
Supply current [a]		-	1.5	2	mA
Battery current		-	-5	-	µA
Battery recharge hysteresis [g]		100	-	200	mV
Shutdown Mode (VDD_CHG too low or disabled by firmware)					
VDD_CHG under-voltage threshold	VDD_CHG rising	-	3.9	-	V
	VDD_CHG falling	-	3.7	-	V
VDD_CHG - BAT_P lockout threshold	VDD_CHG rising	-	0.22	-	V
	VDD_CHG falling	-	0.17	-	V
Supply current		-	1.5	2	mA
Battery current		-1	-	0	µA

[a] Current into VDD_CHG - does not include current delivered to battery (I VDD_CHG - I BAT_P)

[b] BAT_P < Float voltage

[c] Charge current can be set in 16 equally spaced steps

[d] Trickle charge threshold < BAT_P < Float voltage

[e] Where headroom = VDD_CHG - BAT_P

[f] Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence

[g] Hysteresis of (VFLOAT - BAT_P) for charging to restart

Table 4: Battery charger characteristics

Stereo CODEC Analogue to Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution			-	-	16	Bits
Input Sample Rate, F_{sample}			8	-	44.1	kHz
Signal to Noise Ratio, SNR	fin = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% 150mVpk-pk input	F_{sample}				
		8 kHz	-	82	-	dB
		11.025 kHz	-	81	-	dB
		16 kHz	-	80	-	dB
		22.050 kHz	-	79	-	dB
		32 kHz	-	79	-	dB
		44.1 kHz	-	78	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-3	-	42	dB
Input full scale at maximum gain (differential)			-	4	-	mV rms
Input full scale at minimum gain (differential)			-	800	-	mV rms
3dB Bandwidth			-	20	-	kHz
Microphone mode input impedance			-	6.0	-	kΩ
THD+N (microphone input) @ 30mV rms input			-	0.04	-	%

Table 5: Stereo CODEC ADC characteristics

Stereo CODEC Digital to Analog Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution			-	-	16	Bits
Input Sample Rate, F_{sample}			8	-	48	kHz
Signal to Noise Ratio, SNR	fin = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% 150mVpk-pk input	F_{sample}				
		8 kHz	-	95	-	dB
		11.025 kHz	-	95	-	dB
		16 kHz	-	95	-	dB
		22.050 kHz	-	95	-	dB
		32 kHz	-	95	-	dB
		44.1 kHz	-	95	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		0	-	-21	dB
Output voltage full scale swing (differential)			-	750	-	mV rms
Allowed Load		Resistive	16(8)	-	OC	Ω
		Capacitive	-	-	500	pF
THD+N 100kΩ load			-	-	0.01	%
THD+N 16Ω load			-	-	0.1	%
SNR (Load = 16Ω, 0dBFS input relative to digital silence)			-	95	-	dB

Table 6: Stereo CODEC DAC characteristics

Radio characteristics and general specifications

	Specification		Note
Operating frequency range	(2400 ... 2483,5) MHz		ISM Band
Lower quard band	2 MHz		
Upper quard band	3,5 MHz		
Carrier frequency	2402 MHz ... 2480 MHz		f = 2402 + k, k = 0...78
Modulation method	GFSK (1 Mbps) ∏/4 DQPSK (2Mbps) 8DQPSK (3Mbps)		
Hopping	1600 hops/s, 1 MHz channel space		
Maximum data rate	GFSK:	Asynchronous, 723.2 kbps / 57.6 kbps Synchronous: 433.9 kbps / 433.9 kbps	
	∏/4 DQPSK:	Asynchronous, 1448.5 kbps / 115.2 kbps Synchronous: 869.7 kbps / 869.7 kbps	
	8DQPSK:	Asynchronous, 2178.1 kbps / 177.2 kbps Synchronous: 1306.9 kbps / 1306.9 kbps	
Receiving signal range	TBD		Typical condition
Receiver IF frequency	1.5 MHz		Center frequency
Transmission power	Min	TBD	
	Max	TBD	
RF input impedance	50 Ω		
Compliance	Bluetooth specification, version 2.1 + EDR		
USB specification	USB specification, version 1.1 (USB 2.0 compliant)		

Table 7: Radio characteristics and general specifications

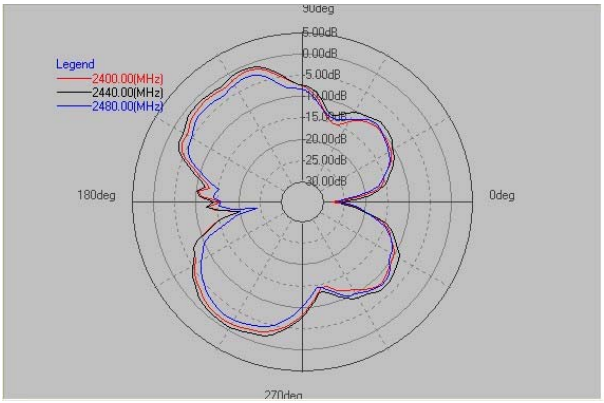
3.1 Radio Characteristics

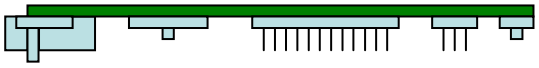
	WT32-A (*)		WT32-E (**)	
	DH1	3DH5	DH1	3DH5
Sensitivity (0.1% BER)	-87 dBm	-81 dBm	-87 dBm	-81 dBm
Max output power (typical)	0 dBm	-1 dBm	8 dBm	5 dBm

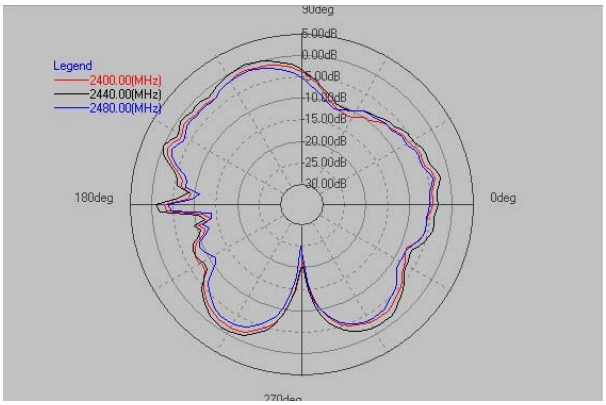
(*) Measured from the antenna
(**) Measured from the w-fl connector

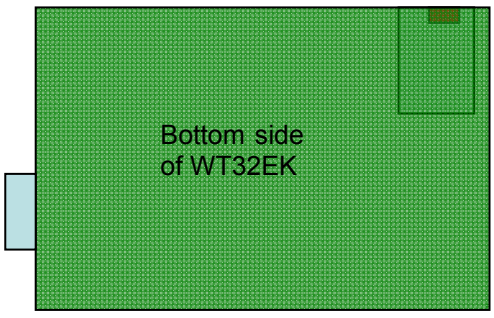
3.1.1 Radiation Pattern (WT32EK)

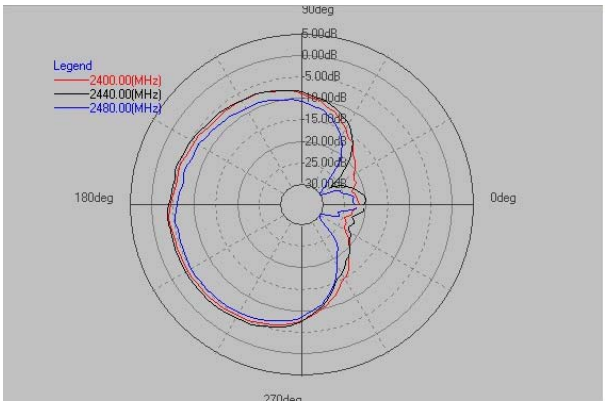
- Peak gain = 1.5 dBi
- Total efficiency = 50%

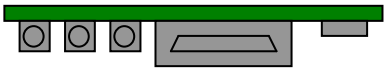












4 WT32 Pin Description

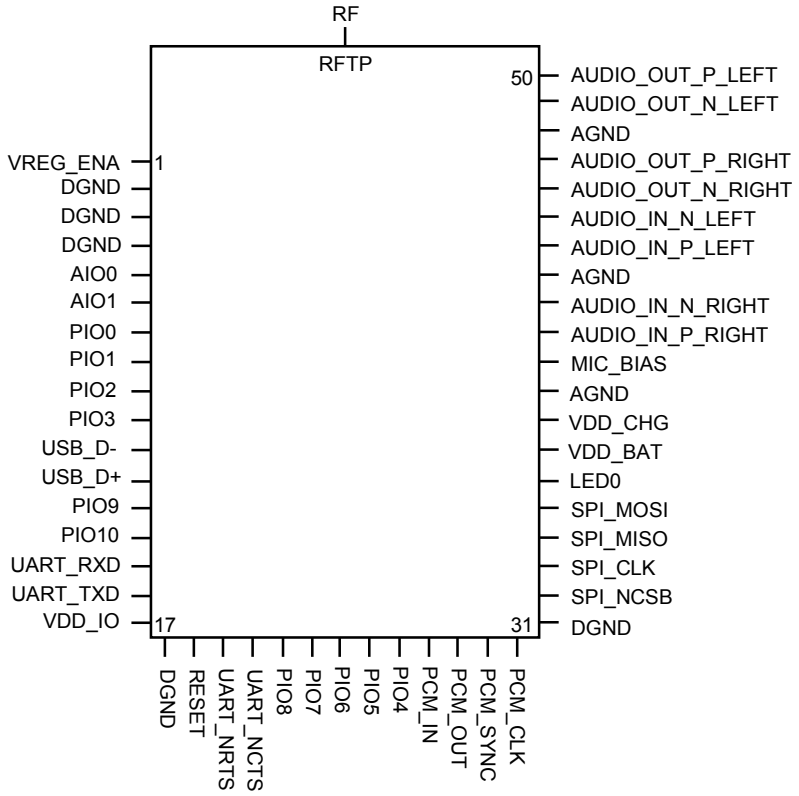


Figure 2: WT32 connection diagram (top view)

NOTE: VREG_ENA pin is only available with the production version of the module. With engineering samples the VREG_ENA is internally connected to VDD_BAT.

DEVICE TERMINALS	
1	VREG_ENA
2	DGND
3	DGND
4	DGND
5	AIO0
6	AIO1
7	PIO0
8	PIO1
9	PIO2
10	PIO3
11	USB_DN
12	USB_DP
13	PIO9
14	PIO10
15	RXD
16	TXD
17	VDD_IO
18	DGND
19	RESET
20	RTS#

21	CTS#
22	PIO8
23	PIO7
24	PIO6
25	PIO5
26	PIO4
27	PCM_IN
28	PCM_OUT
29	PCM_SYNC
30	PCM_CLK
31	DGND
32	SPI_CS#
33	SPI_CLK
34	SPI_MISO
35	SPI_MOSI
36	LED0
37	VDD_BAT
38	VDD_CHG
39	AGND
40	MIC_BIAS
41	AUDIO_IN _P_RIGHT
42	AUDIO_IN _N_RIGHT
43	AGND
44	AUDIO_IN _P_LEFT
45	AUDIO_IN_N_LEFT
46	AUDIO_OUT _N_RIGHT
47	AUDIO_OUT _P_RIGHT
48	AGND
49	AUDIO_OUT_N_LEFT
50	AUDIO_OUT_P_LEFT
RFTP	RF test point

Table 8: WT32 device terminals

4.1 Device Terminal Functions

DGND

Connect digital GND pins to the ground plane of the PCB.

AGND

Ground for the audio signals. AGND and DGND are internally combined in WT32. Use solid ground plane for AGND and keep AGND and DGND planes separated.

VDD_IO

Supply voltage connection for the digital I/Os of the module. Supply voltage at this pin can vary between 1.8 V and 3.3 V. Output voltage swing at the digital terminals of WT32 is 0 to VDD_IO.

VDD_BAT

Input for an internal 1.8 V switched mode regulator combined with output of the internal battery charger. See chapter 5.3 for detailed description for the charger. When not powered from a battery, VDD_IO and VDD_BAT can be combined to a single 3.3 V supply voltage.

VREG_ENA

Enable pin for the internal 1,8 V regulator. This pin is only available with production version. With the engineering samples VREG_ENA is internally connected to VDD_BAT.

VDD_CHG

Charger input voltage. The charger will start operating when voltage to this pin is applied. When the charger is not used, this pin should be left floating. See chapter 5.3 for detailed description of the charger.

RES

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

WT32 has an internal reset circuitry, which keeps the reset pin active until supply voltage has reached stability in the start up. This ensures that supply for the flash memory inside the WT32 will reach stability before BC4 chip fetches instructions from it. Schematic of the reset circuitry is shown in figure 3. Rising supply voltage charges the capacitor, which will activate the reset of WT32. The capacitor discharges through 220 kΩ resistor, which eventually deactivates the reset. Time constant of the RC circuitry is set in a way that the supply voltage is safely stabilized before the reset deactivates. Pull-up or pull-down resistor should not be connected to the reset pin to ensure proper start up of WT32. If the reset pin of WT32 is in use, the designer should verify that WT32 remains in reset during a start-up until all supply voltages have stabilized.

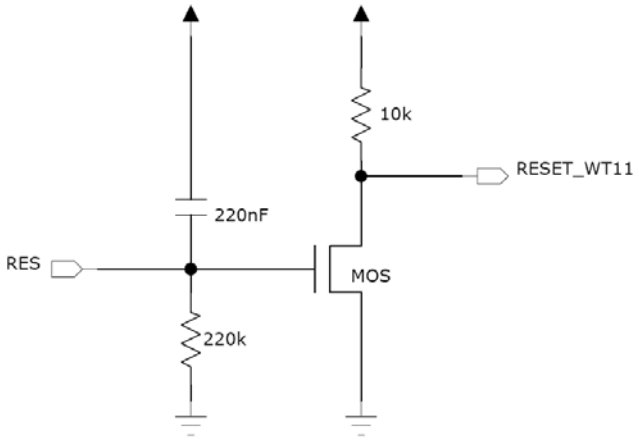


Figure 3: WT32 internal reset circuitry

See chapter 4 for detailed description of reset.

PIO0 – PIO10

Programmable digital I/O lines. All PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. Configuration for each PIO line depends on the application. See section 10 “I/O parallel ports” for detailed descriptions for each terminal. Default configuration for all of the PIO lines is input with weak internal pull-up.

AIO0 – AIO1

AIOs can be used to monitor analogue voltages such as a temperature sensor for the battery charger. AIOs can also be configured to be used as digital I/Os. The voltage level at these pins is 0 V to 1,5 V.

UART_NRTS

A CMOS output with a weak internal pull-up. This pin can be used to implement RS232 hardware flow control where RTS (request to send) is an active low indicator. The UART interface requires an external RS232 transceiver chip.

UART_NCTS

A CMOS input with a weak internal pull-down. This pin can be used to implement RS232 hardware flow control where CTS (clear to send) is an active low indicator. The UART interface requires an external RS232 transceiver chip.

UART_RXD

A CMOS input with a weak internal pull-down. RXD is used to implement UART data transfer from another device to WT32. The UART interface requires an external RS232 transceiver chip.

UART_TXD

A CMOS output with a weak internal pull-up. TXD is used to implement UART data transfer from WT32 to another device. The UART interface requires external RS232 transceiver chip.

PCM_OUT

A CMOS output with a weak internal pull-down. Used in the PCM (pulse code modulation) interface to transmit digitized audio. The PCM interface is shared with the I^2S interface.

PCM_IN

A CMOS input with a weak internal pull-down. Used in the PCM interface to receive digitized audio. The PCM interface is shared with the I^2S interface.

PCM_CLK

A bi-directional synchronous data clock signal pin with a weak internal pull-down. PCMC is used in the PCM interface to transmit or receive the CLK signal. When configured as a master, WT32 generates the clock signal for the PCM interface. When configured as a slave, the PCMC is an input and receives the clock signal from another device. The PCM interface is shared with the I^2S interface.

PCM_SYNC

A bi-directional synchronous data strobe with a weak internal pull-down. When configured as a master, WT32 generates the SYNC signal for the PCM interface. When configured as a slave, the PCMS is an input and receives the SYNC signal from another device. The PCM interface is shared with the I^2S interface.

USB_D+

A bi-directional USB data line with a selectable internal 1.5 kΩ pull-up implemented as a current source (compliant with USB specification v1.2) An external series resistor is required to match the connection to the characteristic impedance of the USB cable.

USB_D-

A bi -directional USB data line. An external series resistor is required to match the connection to the characteristic impedance of the USB cable.

SPI_NCSB

A CMOS input with a weak internal pull-down. Active low chip select for SPI (serial peripheral interface).

SPI_CLK

A CMOS input for the SPI clock signal with a weak internal pull-down. WT32 is the slave and receives the clock signal from the device operating as a master.

SPI_MISO

An SPI data output with a weak internal pull-down.

SPI_MOSI

An SPI data input with a weak internal pull-down.

RF

This pin can be used when not using a chip antenna or w.fl connector of the module.

AUDIO_IN_P_RIGHT and AUDIO_IN_N_RIGHT

Right channel audio inputs. This dual audio input can be configured to be either single-ended or fully differential and programmed for either microphone or line input. Route differential pairs close to each other and use a solid dedicated audio ground plane for the audio signals.

AUDIO_IN_P_LEFT and AUDIO_IN_N_LEFT

Left channel audio input. ESD protection and layout considerations similar to right channel audio should be used.

AUDIO_OUT_P_RIGHT and AUDIO_OUT_N_RIGHT

Right channel audio output. The audio output lines should be routed differentially to either the speakers or to the output amplifier, depending on whether or not a single-ended signal is required. Use low impedance ground plane dedicated for the audio signals.

AUDIO_OUT_P_LEFT and AUDIO_OUT_N_LEFT

Left channel audio output. The same guidelines apply to this section as discussed previously.

MIC_BIAS

Bias voltage output for a microphone. Use the same layout guidelines as discussed previously with other audio signals.

LED0

WT32 includes a pad dedicated to driving LED indicators. This terminal may be controlled by firmware and it can also be set by the battery charger. The terminal is an open-drain output, so the LED must be connected from a positive supply rail to the pad in series with a current limiting resistor.

It is recommended that the LED pad is operated with a pad voltage below 0.5V. In this case, the pad can be thought of as a resistor, RON. The resistance together with the external series resistor will set the current, ILED, in the LED. Value for the external series resistance can be calculated from the Equation 1

$$R_{LED} = \frac{VDD - V_F}{I_{LED}} - R_{ON}$$

Equation 1: LED series resistor

Where V_F is the forward voltage drop of the LED, I_{LED} is the forward current of the LED and R_{ON} is the on resistance (typically 20 Ω) of the LED driver.

5 Power Control

5.1 Power Supply Configuration

WT32 contains an internal battery charger and a switch mode regulator that is mainly used for internal blocks of the module. The module can be powered from a single 3.3 V supply provided that VDD_CHG is floating. Alternatively the module can be powered from a battery connected to VDD_BAT and using an external regulator for VDD_IO. 1.8 V to 3.3 V supply voltage for VDD_IO can be used to give desired signal levels for the digital interfaces of the module. USB, however, requires 3.3 V for proper operation and thus, when USB is in use, 3.3 V for VDD_IO is mandatory.

AIO pins of the module use 1.8 V from the internal regulator and thus voltage level with these pins is within 0 V and 1.8 V.

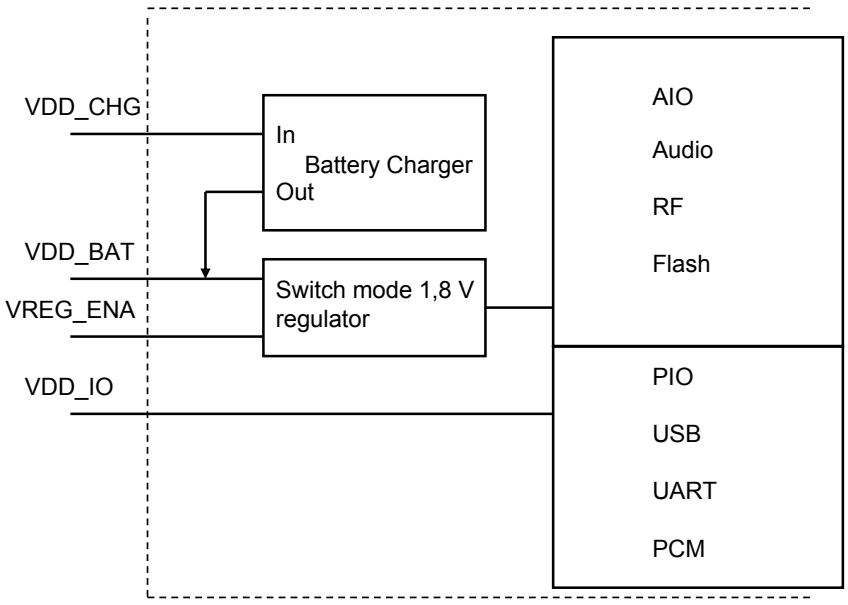


Figure 4: Power supply configuration of WT32

5.2 Voltage Regulator Enable Pin

The regulator enable pin VREG_ENA is used to enable WT32. VREG_ENA enables the on-chip switched mode regulator.

VREG_ENA is active high, with a logic threshold of around 1V, and it has weak pull-down. It can tolerate voltages up to 4.9V, so it may be connected directly to a battery to enable the device.

VREG_ENA can be configured with iWRAP to either latch on/off the internal regulators at the rising edge of the input voltage, or to latch the regulators on at the rising edge and shut down the regulators at the falling edge. Following figure shows an example of how to to implement a power on/off button using the latch feature. See iWRAP user guide for the details on configuration.

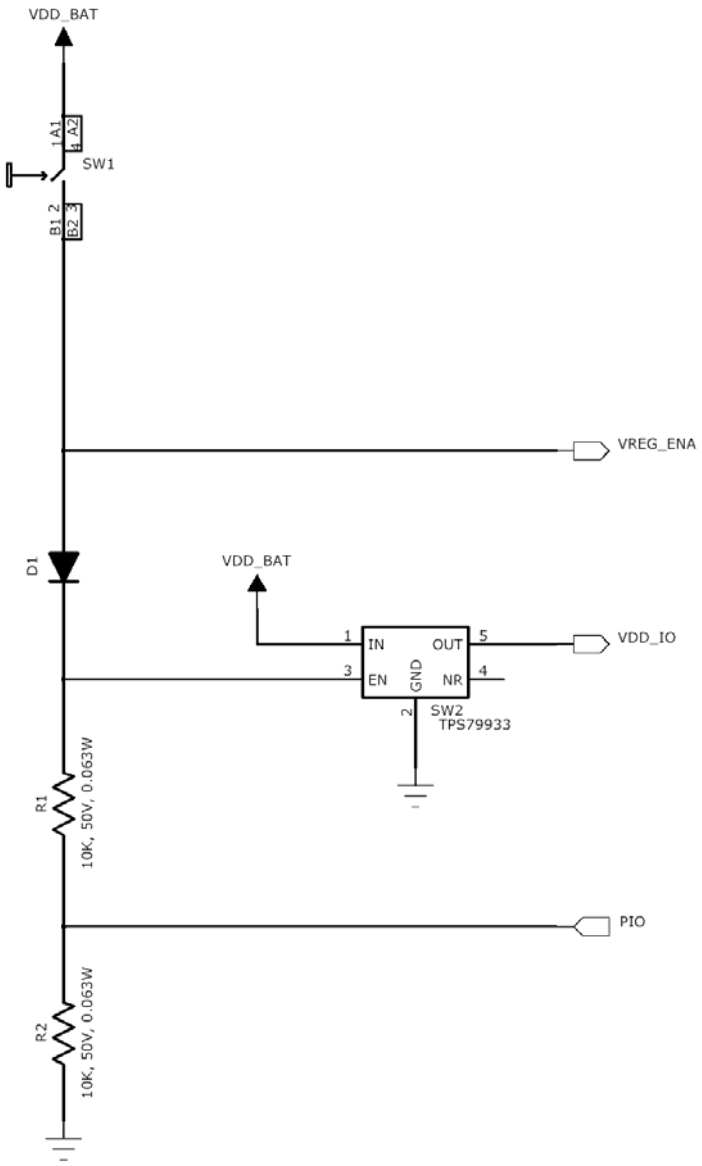


Figure 5: Example of how to make a power on/off button using latch feature of the internal regulators

In figure 6 the internal regulators are latched on at the rising edge, i.e when pressing SW1. One of the PIOs is configured to power hold thus keeping the external regulator on until shut down by pressing SW1 again.

5.3 Battery Charger

The battery charger is a constant current / constant voltage charger circuit, and is suitable for lithium ion/polymer batteries only. It shares a connection to the battery terminal, VDD_BAT, with the switch-mode regulator. The charger is initially calibrated by Bluegiga Technologies to have V_{float} = 4.2 V.

The constant current level can be varied to allow charging of different capacity batteries.

The charger enters various states of operation as it charges a battery. These are shown below:

- Off: entered when the charger is disconnected.
- Trickle Charge: entered when the battery voltage is below 2.9V.
- Fast Charge - Constant Current: entered when the battery voltage is above 2.9V.
- Fast Charge - Constant Voltage: entered when the battery has reached V_{float}, the charger switches mode to maintain the cell voltage at V_{float} voltage by adjusting the constant charge current.
- Standby: this is the state when the battery is fully charged and no charging takes place.

When a voltage is applied to the charger input terminal VDD_CHG, and the battery is not fully charged, the charger will operate and a LED connected to the terminal LED0 will illuminate. By default, until the firmware is running, the LED will pulse at a low-duty cycle to minimize current consumption.

The battery charger circuitry auto-detects the presence of a power source, allowing the firmware to detect, using an internal status bit, when the charger is powered. Therefore, when the charger supply is not connected to VDD_CHG, the terminal must be left open circuit. The VDD_CHG pin, when not connected, must be allowed to float and not be pulled to a power rail. When the battery charger is not enabled, this pin may float to a low undefined voltage. Any DC connection will increase current consumption of the device. Capacitive components such as diodes, FETs, and ESD protection, may be connected.

The battery charger is designed to operate with a permanently connected battery. If the application permits the charger input to be connected while the battery is disconnected, the VDD_BAT pin voltage may become unstable. This, in turn, may cause damage to the internal switch-mode regulator. Connecting a 470µF capacitor to VDD_BAT limits these oscillations thus preventing damage.

WARNING:

Use good consideration for battery safety. Do not charge with too much current. Do not charge when the temperature is above 60°C or below 0°C. WT32 is initially calibrated to stop charging when battery voltage is at 4.2 V. Do not try to charge batteries above 4.2 V. Do not short circuit the battery or discharge below 1.5 V.

5.4 RESET

WT32 may be reset from several sources: reset pin, power on reset, a UART break character or through software configured watchdog timer.

The power on reset occurs when the VDD_CORE supply falls below typically 1.26V and is released when VDD_CORE rises above typically 1.31V. At reset, the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown in Table 9.

The chip status after a reset is as follows:

- Warm Reset: data rate and RAM data remain available
- Cold Reset(10): data rate and RAM data are not available

Table 9 shows the pin states of WT32 on reset. Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

Pin Name / Group	**I/O Type**	**State on Reset**
USB_D+	Digital bi-directional	N/A
USB_D-	Digital bi-directional	N/A
UART_RX	Digital input with PD	PD
UART_CTS	Digital input with PD	PD
UART_TX	Digital bi-directional with PU	PU
UART_RTS	Digital bi-directional with PU	PU
SPI_MOSI	Digital input with PD	PD
SPI_CLK	Digital input with PD	PD
SPI_CS#	Digital input with PU	PU
SPI_MISO	Digital tri-state output with PD	PD
PCM_IN	Digital input with PD	PD
PCM_CLK	Digital bi-directional with PD	PD
PCM_SYNC	Digital bi-directional with PD	PD
PCM_OUT	Digital tri-state output with PD	PD
PIO[10:0]	Digital bi-directional with PU/PD	PD

Table 9: Pin states on reset

6 Serial Interfaces

6.1 UART Interface

WT32 Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard. The UART interface of WT32 uses voltage levels from 0 to VDD_IO and thus an external transceiver IC is required to meet the voltage level specifications of RS232.

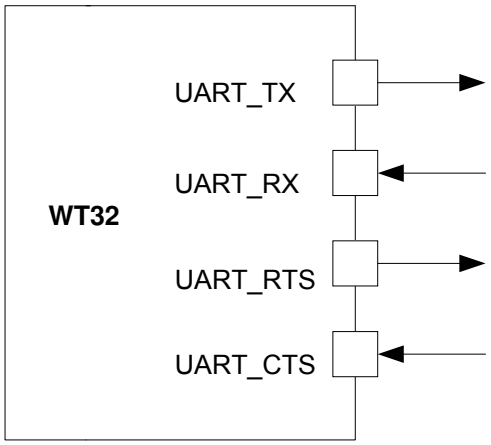


Figure 6: WT32 UART interface

Four signals are used to implement the UART function, as shown in Figure 7. When WT32 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. DTR, DSR and DCD signals can be implemented by using PIO terminals of WT32. All UART connections are implemented by using CMOS technology and have signaling levels of 0V and VDD_IO.

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		**Possible values**
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	3.0Mbaud (≤1%Error)
Flow control		RTS/CTS, none
Parity		None, Odd, Even
Number of stop bits		1 or 2
Bits per channel		8

Table 10: Possible UART settings

The UART interface is capable of resetting WT32 upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 8. If tBRK is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialize the system to a known state. Also, WT32 can emit a Break character that may be used to wake the Host.

Since UART_RX terminal includes a weak internal pull-down, it cannot be left open unless disabling UART interface using PS_KEY settings. If UART is not disabled, a pull-up resistor has to be connected to UART_RX. The UART interface requires an external RS232 transceiver, which usually includes the required pull-up.