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Dual DCP, POR, Dual Voltage Monitors

FEATURES

- Two Digitally Controlled Potentiometers (DCPs)
  - —100 Tap - 10kΩ
  - —256 Tap - 100kΩ
  - —Nonvolatile
  - —Write Protect Function
- 2-Wire Industry Standard Serial Interface
- Power-On Reset (POR) Circuitry
  - —Programmable Threshold Voltage
  - —Software Selectable reset timeout
  - —Manual Reset
- Two Supplementary Voltage Monitors
  - —Programmable Threshold Voltages
- Single Supply Operation
  - —2.7V to 5.5V
- **Hot Pluggable**
- 20 Pin Package
  - —TSSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

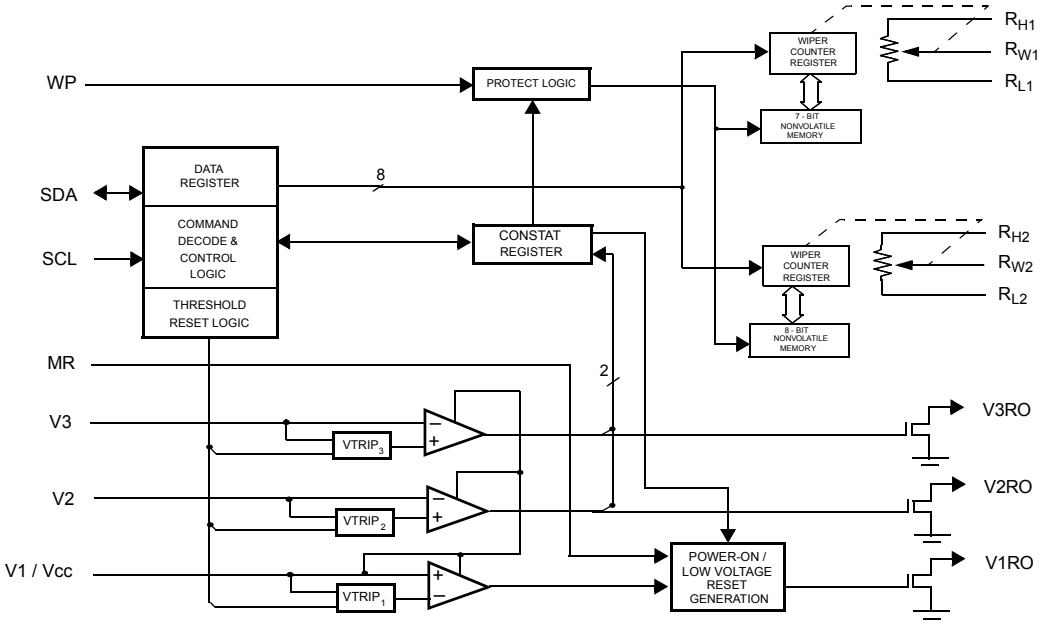
DESCRIPTION

The X9523 combines two Digitally Controlled Potentiometers (DCPs), V1 / Vcc Power-on Reset (POR) circuitry, qnd two programmable voltage monitor inputs with software and hardware indicators. All functions of the X9523 are accessed by an industry standard 2-Wire serial interface.

The DCPs of the X9523 may be utilized to control the bias and modulation currents of the laser diode in a Fiber Optic module. The programmable POR circuit may be used to ensure that V1 / Vcc is stable before power is applied to the laser diode / module. The programmable voltage monitors may be used for monitoring various module alarm levels.

The features of the X9523 are ideally suited to simplifying the design of fiber optic modules . The integration of these functions into one package significantly reduces board area, cost and increases reliability of laser diode modules.

BLOCK DIAGRAM



Ordering Information

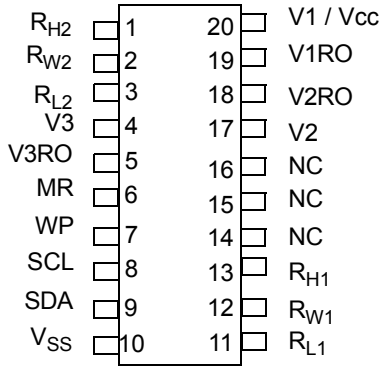
PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE
X9523V20I-A	X9523VIA	-40 to +85	20 Ld TSSOP
X9523V20I-B	X9523VIB	-40 to +85	20 Ld TSSOP
X9523V20IZ-A (Note)	X9523VZIA	-40 to +85	20 Ld TSSOP (Pb-free)
X9523V20IZ-B (Note)	X9523VZIB	-40 to +85	20 Ld TSSOP (Pb-free)

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PIN CONFIGURATION

20 Pin TSSOP



NOT TO SCALE

DETAILED DEVICE DESCRIPTION

The X9523 combines two Intersil Digitally Controlled Potentiometer (DCP) devices, V1/Vcc power-on reset control, V1/Vcc low voltage reset control, and two supplementary voltage monitors in one package. These functions are suited to the control, support, and monitoring of various system parameters in fiber optic modules. The combination of the X9523 functionality lowers system cost, increases reliability, and reduces board space requirements.

Two high resolution DCPs allow for the “set-and-forget” adjustment of Laser Driver IC parameters such as Laser Diode Bias and Modulation Currents.

Applying voltage to V_{CC} activates the Power-on Reset circuit which allows the V1RO output to go HIGH, until the supply the supply voltage stabilizes for a period of time (selectable via software). The V1RO output then goes LOW. The Low Voltage Reset circuitry allows the V1RO output to go HIGH when V_{CC} falls below the minimum V_{CC} trip point. V1RO remains HIGH until V_{CC} returns to proper operating level. A Manual Reset (MR) input allows the user to externally trigger the V1RO output (HIGH).

Two supplementary Voltage Monitor circuits continuously compare their inputs to individual trip voltages. If an input voltage exceeds it’s associated trip level, a hardware output (V3RO, V2RO) are allowed to go HIGH. If the input voltage becomes lower than it’s associated trip level, the corresponding output is driven LOW. A corresponding binary representation of the two monitor circuit outputs (V2RO and V3RO) are also stored in latched, volatile (CONSTAT) register bits. The status of these two monitor outputs can be read out via the 2-wire serial port.

Intersil’s unique circuits allow for all internal trip voltages to be individually programmed with high accuracy. This gives the designer great flexibility in changing system parameters, either at the time of manufacture, or in the field.

The device features a 2-Wire interface and software protocol allowing operation on an I^2C™ compatible serial bus.

PIN ASSIGNMENT

Pin	Name	Function
1	R_{H2}	Connection to end of resistor array for (the 256 Tap) DCP 2.
2	R_{w2}	Connection to terminal equivalent to the “Wiper” of a mechanical potentiometer for DCP 2.
3	R_{L2}	Connection to other end of resistor array for (the 256 Tap) DCP 2.
4	V3	V3 Voltage Monitor Input. V3 is the input to a non-inverting voltage comparator circuit. When the V3 input is higher than the V_{TRIP3} threshold voltage, V3RO makes a transition to a HIGH level. Connect V3 to V_{SS} when not used.
5	V3RO	V3 RESET Output. This open drain output makes a transition to a HIGH level when V3 is greater than V_{TRIP3} and goes LOW when V3 is less than VTRIP3. There is no delay circuitry on this pin. The V3RO pin requires the use of an external “pull-up” resistor.
6	MR	Manual Reset. MR is a TTL level compatible input. Pulling the MR pin active (HIGH) initiates a reset cycle to the V1RO pin (V1/Vcc RESET Output pin). V1RO will remain HIGH for time t_{purst} after MR has returned to it’s normally LOW state. The reset time can be selected using bits POR1 and POR0 in the CONSTAT Register. The MR pin requires the use of an external “pull-down” resistor.
7	WP	Write Protect Control Pin. WP pin is a TTL level compatible input. When held HIGH, Write Protection is enabled. In the enabled state, this pin prevents all nonvolatile “write” operations. Also, when the Write Protection is enabled, and the device DCP Write Lock feature is active (i.e. the DCP Write Lock bit is “1”), then no “write” (volatile or nonvolatile) operations can be performedon the wiper position of any of the integrated Digitally Controlled Potentiometers (DCPs). The WP pin uses an internal “pull-down” resistor, thus if left floating the write protection feature is disabled.
8	SCL	Serial Clock. This is a TTL level compatible input pin used to control the serial bus timing for data input and output.
9	SDA	Serial Data. SDA is a bidirectional TTL level compatible pin used to transfer data into and out of the device. The SDA pin input buffer is always active (not gated). This pin requires an external pull up resistor.
10	Vss	Ground.
11	R_{L1}	Connection to other end of resistor for (the 100 Tap) DCP 1.
12	R_{w1}	Connection to terminal equivalent to the “Wiper” of a mechanical potentiometer for DCP 1.
13	R_{H1}	Connection to end of resistor array for (the 100 Tap) DCP 1.
17	V2	V2 Voltage Monitor Input. V2 is the input to a non-inverting voltage comparator circuit. When the V2 input is greater than the V_{TRIP2} threshold voltage, V2RO makes a transition to a HIGH level. Connect V2 to V_{SS} when not used.
18	V2RO	V2 RESET Output. This open drain output makes a transition to a HIGH level when V2 is greater than V_{TRIP2}, and goes LOW when V2 is less than V_{TRIP2}. There is no power-up reset delay circuitry on this pin. The V2RO pin requires the use of an external “pull-up” resistor.
19	V1RO	V1 / Vcc RESET Output. This is an active HIGH, open drain output which becomes active whenever V1 / Vcc falls below V_{TRIP1}. V1RO becomes active on power-up and remains active for a time t_{purst} after the power supply stabilizes (t_{purst} can be changed by varying the POR0 and POR1 bits of the internal control register). The V1RO pin requires the use of an external “pull-up” resistor. The V1RO pin can be forced active (HIGH) using the manual reset (MR) input pin.
20	V1 / Vcc	Supply Voltage.
14, 15, 16,	NC	No Connect.

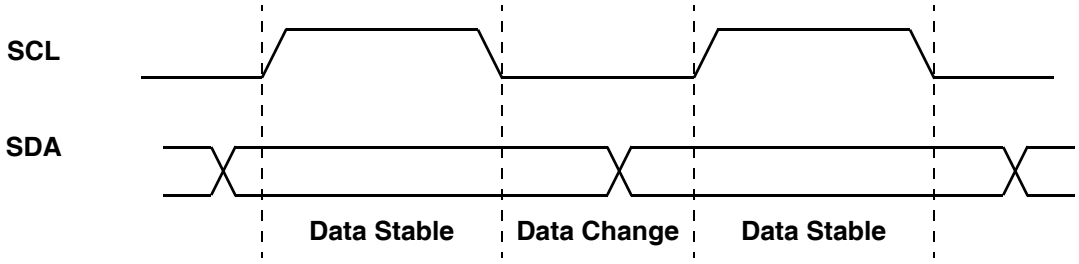


Figure 1. Valid Data Changes on the SDA Bus

PRINCIPLES OF OPERATION

SERIAL INTERFACE

Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the X9523 operates as a slave in all applications.

Serial Clock and Data

Data states on the SDA line can change only while SCL is LOW. SDA state changes while SCL is HIGH are reserved for indicating START and STOP conditions. See Figure 1.On power-up of the X9523, the SDA pin is in the input mode.

Serial Start Condition

All commands are preceded by the START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition has been met. See Figure 2.

Serial Stop Condition

All communications must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. The STOP condition is also used to place the device into the Standby power mode after a read sequence. A STOP condition can only be issued after the transmitting device has released the bus. See Figure 2.

Serial Acknowledge

An ACKNOWLEDGE (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKNOWLEDGE that it received the eight bits of data. Refer to Figure 3.

The device will respond with an ACKNOWLEDGE after recognition of a START condition if the correct Device Identifier bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an ACKNOWLEDGE after the receipt of each subsequent eight bit word.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an ACKNOWLEDGE. If an ACKNOWLEDGE is detected and no STOP condition is generated by the master, the device will continue to transmit data. The device will ter-

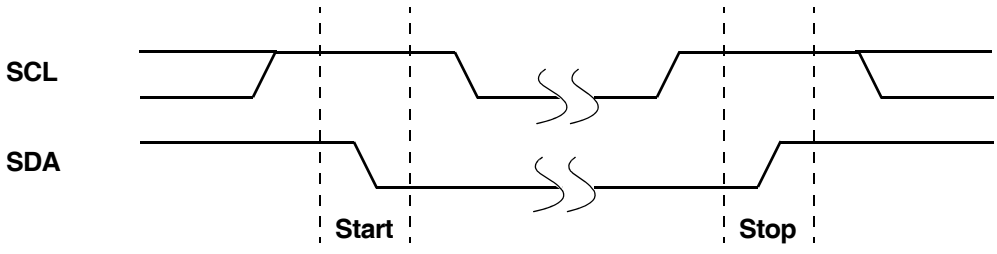


Figure 2. Valid Start and Stop Conditions

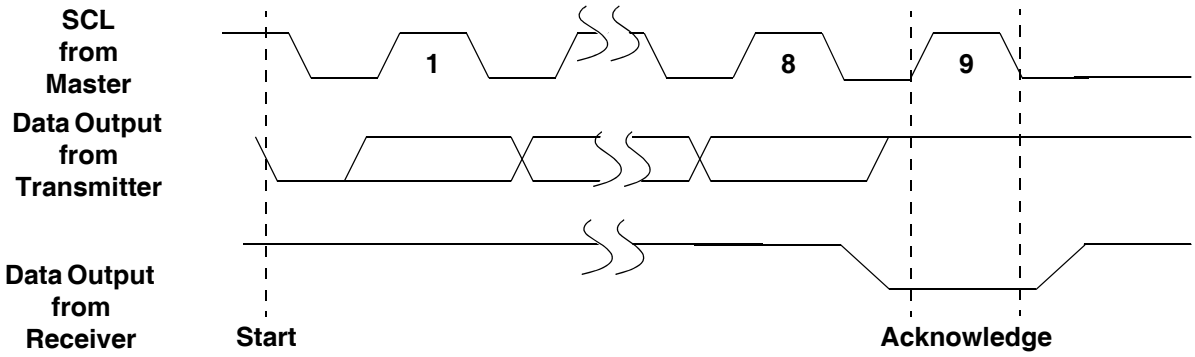


Figure 3. Acknowledge Response From Receiver

minate further data transmissions if an ACKNOWLEDGE is not detected. The master must then issue a STOP condition to place the device into a known state.

DEVICE INTERNAL ADDRESSING

Addressing Protocol Overview

The user addressable internal components of the X9523 can be split up into two main parts:

—Two Digitally Controlled Potentiometers (DCPs)

—Control and Status (CONSTAT) Register

Depending upon the operation to be performed on each of these individual parts, a 1, 2 or 3 Byte protocol is used. All operations however must begin with the Slave Address Byte being issued on the SDA pin. The Slave address selects the part of the X9523 to be addressed, and specifies if a Read or Write operation is to be performed.

It should be noted that in order to perform a write operation to a DCP, the Write Enable Latch (WEL) bit must first be set (See “WEL: Write Enable Latch (Volatile)” on page 10.).

Slave Address Byte

Following a START condition, the master must output a Slave Address Byte (Refer to Figure 4.). This byte consists of three parts:

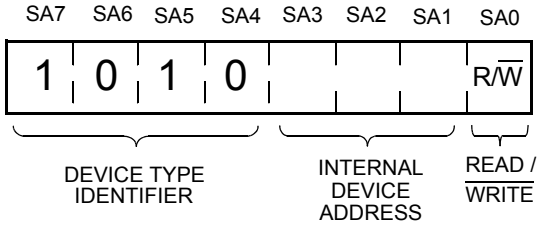
—The Device Type Identifier which consists of the most significant four bits of the Slave Address (SA7 - SA4). The Device Type Identifier must always be set to 1010 in order to select the X9523.

—The next three bits (SA3 - SA1) are the Internal Device Address bits. Setting these bits to 111 internally selects the DCP structures in the X9523. The CONSTAT Register may be selected using the Internal Device Address 010.

—The Least Significant Bit of the Slave Address (SA0) Byte is the R/$\overline{W}$ bit. This bit defines the operation to be performed on the device being addressed (as defined in the bits SA3 - SA1). When the R/$\overline{W}$ bit is “1”, then a READ operation is selected. A “0” selects a WRITE operation (Refer to Figure 4.)

Nonvolatile Write Acknowledge Polling

After a nonvolatile write command sequence (for either the Non Volatile Memory of a DCP (NVM), or the CONSTAT Register) has been correctly issued (including the



Internal Address (SA3 - SA1)	Internally Addressed Device
010	CONSTAT Register
111	DCP
All Others	RESERVED

Bit SA0	Operation
0	WRITE
1	READ

Figure 4. Slave Address Format

final STOP condition), the X9523 initiates an internal high voltage write cycle. This cycle typically requires 5 ms. During this time, no further Read or Write commands can be issued to the device. Write Acknowledge Polling is used to determine when this high voltage write cycle has been completed.

To perform acknowledge polling, the master issues a START condition followed by a Slave Address Byte. The Slave Address issued must contain a valid Internal Device Address. The LSB of the Slave Address (R/$\overline{W}$) can be set to either 1 or 0 in this case. If the device is still busy with the high voltage cycle then no ACKNOWLEDGE will be returned. If the device has completed the write operation, an ACKNOWLEDGE will be returned and the host can then proceed with a read or write operation. (Refer to Figure 5.).

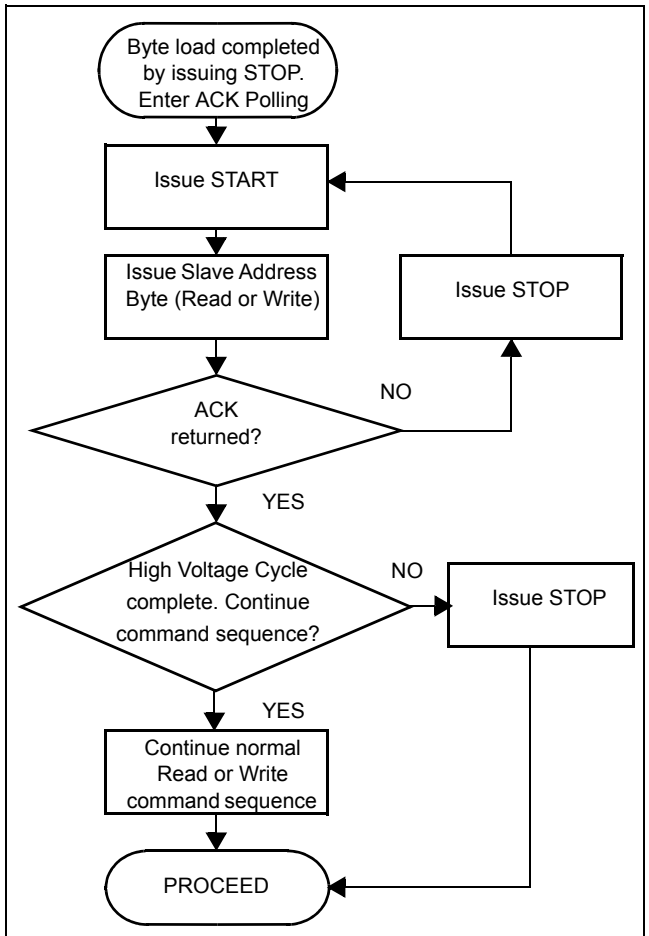


Figure 5. Acknowledge Polling Sequence

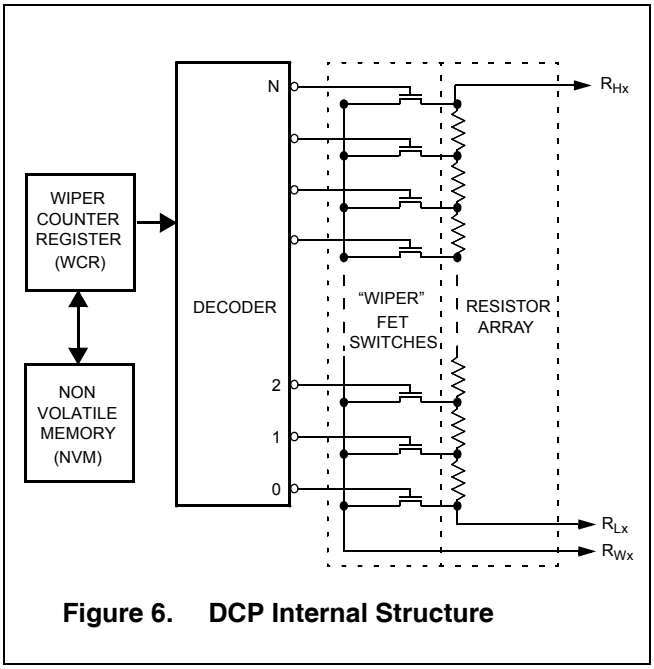


Figure 6. DCP Internal Structure

DIGITALLY CONTROLLED POTENTIOMETERS

DCP Functionality

The X9523 includes two independent resistor arrays. These arrays respectively contain 99 and 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_{Hx} and R_{Lx} inputs - where x = 1,2).

At both ends of each array and between each resistor segment there is a CMOS switch connected to the wiper (R_{Wx}) output. Within each individual array, only one switch may be turned on at any one time. These switches are controlled by the Wiper Counter Register (WCR) (See Figure 6). The WCR is a volatile register.

On power-up of the X9523, wiper position data is automatically loaded into the WCR from its associated Non Volatile Memory (NVM) Register. The Table below shows the Initial Values of the DCP WCR's before the contents of the NVM is loaded into the WCR.

DCP	Initial Values Before Recall
R_1 / 100 TAP	V_L / TAP = 0
R_2 / 256 TAP	V_H / TAP = 255

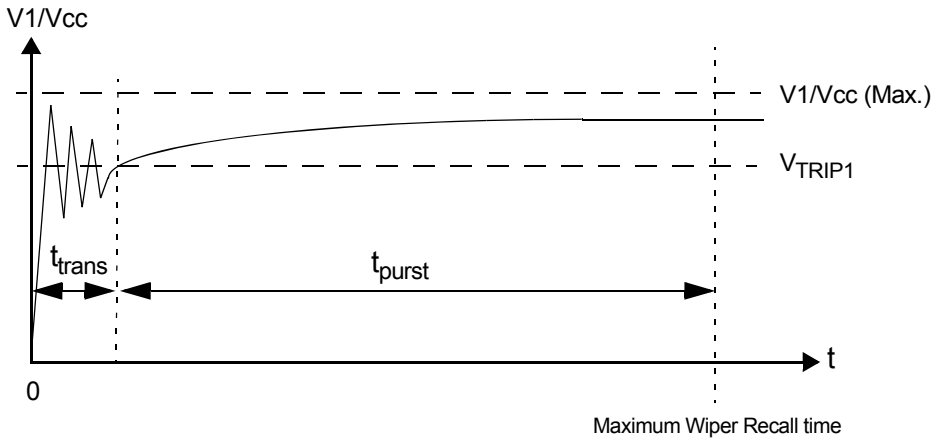


Figure 7. DCP Power-up

The data in the WCR is then decoded to select and enable one of the respective FET switches. A “make before break” sequence is used internally for the FET switches when the wiper is moved from one tap position to another.

Hot Pluggability

Figure 7 shows a typical waveform that the X9523 might experience in a Hot Pluggable situation. On power-up, V1 / Vcc applied to the X9523 may exhibit some amount of ringing, before it settles to the required value.

The device is designed such that the wiper terminal (R_{Wx}) is recalled to the correct position (as per the last stored in the DCP NVM), when the voltage applied to V1/Vcc exceeds V_{TRIP1} for a time exceeding t_{purst} (the Power-on Reset time, set in the CONSTAT Register - See “CONTROL AND STATUS REGISTER” on page 10.).

Therefore, if t_{trans} is defined as the time taken for V1 / Vcc to settle above V_{TRIP1} (Figure 7): then the desired wiper terminal position is recalled by (a maximum) time: $t_{trans} + t_{purst}$. It should be noted that t_{trans} is determined by system hot plug conditions.

DCP Operations

In total there are three operations that can be performed on any internal DCP structure:

—DCP Nonvolatile Write

—DCP Volatile Write

—DCP Read

A nonvolatile write to a DCP will change the “wiper position” by simultaneously writing new data to the associated WCR and NVM. Therefore, the new “wiper position” setting is recalled into the WCR after V1/Vcc of the X9523 is powered down and then powered back up.

A volatile write operation to a DCP however, changes the “wiper position” by writing new data to the associated WCR only. The contents of the associated NVM register remains unchanged. Therefore, when V1/Vcc to the device is powered down then back up, the “wiper position” reverts to that last position written to the DCP using a nonvolatile write operation.

Both volatile and nonvolatile write operations are executed using a three byte command sequence: (DCP) Slave Address Byte, Instruction Byte, followed by a Data Byte (See Figure 9)

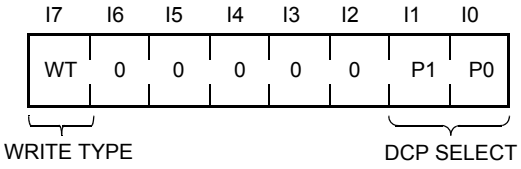
A DCP Read operation allows the user to “read out” the current “wiper position” of the DCP, as stored in the associated WCR. This operation is executed using the Random Address Read command sequence, consisting of the (DCP) Slave Address Byte followed by an Instruction Byte and the Slave Address Byte again (Refer to Figure 10.).

Instruction Byte

While the Slave Address Byte is used to select the DCP devices, an Instruction Byte is used to determine which DCP is being addressed.

The Instruction Byte (Figure 8) is valid only when the Device Type Identifier and the Internal Device Address bits of the Slave Address are set to 1010111. In this case, the two Least Significant Bit’s (I1 - I0) of the Instruction Byte are used to select the particular DCP (0 - 2). In the case of a Write to any of the DCPs (i.e. the LSB of the Slave Address is 0), the Most Significant Bit of the Instruction Byte (I7), determines the Write Type (WT) performed.

If WT is “1”, then a Nonvolatile Write to the DCP occurs. In this case, the “wiper position” of the DCP is changed by simultaneously writing new data to the associated



WT†	Description
0	Select a Volatile Write operation to be performed on the DCP pointed to by bits P1 and P0
1	Select a Nonvolatile Write operation to be performed on the DCP pointed to by bits P1 and P0

†This bit has no effect when a Read operation is being performed.

Figure 8. Instruction Byte Format

WCR and NVM. Therefore, the new "wiper position" setting is recalled into the WCR after V1/Vcc of the X9523 has been powered down then powered back up.

If WT is "0" then a DCP Volatile Write is performed. This operation changes the DCP "wiper position" by writing new data to the associated WCR only. The contents of the associated NVM register remains unchanged. Therefore, when V1/Vcc to the device is powered down then back up, the "wiper position" reverts to that last written to the DCP using a nonvolatile write operation.

DCP Write Operation

A write to DCPx (x = 1,2) can be performed using the three byte command sequence shown in Figure 9.

In order to perform a write operation on a particular DCP, the Write Enable Latch (WEL) bit of the CONSTAT Register must first be set (See "WEL: Write Enable Latch (Volatile)" on page 10.).

The Slave Address Byte 10101110 specifies that a Write to a DCP is to be conducted. An ACKNOWLEDGE is returned by the X9523 after the Slave Address, if it has been received correctly.

Next, an Instruction Byte is issued on SDA. Bits P1 and P0 of the Instruction Byte determine which WCR is to be written, while the WT bit determines if the Write is to be volatile or nonvolatile. If the Instruction Byte format is valid, another ACKNOWLEDGE is then returned by the X9523.

Following the Instruction Byte, a Data Byte is issued to the X9523 over SDA. The Data Byte contents is latched into the WCR of the DCP on the first rising edge of the clock signal, after the LSB of the Data Byte (D0) has been issued on SDA (See Figure 29).

The Data Byte determines the "wiper position" (which FET switch of the DCP resistive array is switched ON) of the DCP. The maximum value for the Data Byte depends upon which DCP is being addressed (see Table below).

P1- P0		DCPx	# Taps	Max. Data Byte
0	0	RESERVED		
0	1	x = 1	100	Refer to Appendix 1
1	0	x = 2	256	FFh
1	1	RESERVED		

Using a Data Byte larger than the values specified above results in the "wiper terminal" being set to the highest tap position. The "wiper position" does NOT roll-over to the lowest tap position.

For DCP2 (256 Tap), the Data Byte maps one to one to the "wiper position" of the DCP "wiper terminal". Therefore, the Data Byte 00001111 (15_{10}) corresponds to setting the "wiper terminal" to tap position 15. Similarly, the Data Byte 00011100 (28_{10}) corresponds to setting the "wiper terminal" to tap position 28. The mapping of the Data Byte to "wiper position" data for DCP1 (100 Tap), is shown in "APPENDIX 1" . An example of a simple C language function which "translates" between the tap position (decimal) and the Data Byte (binary) for DCP1, is given in "APPENDIX 2" .

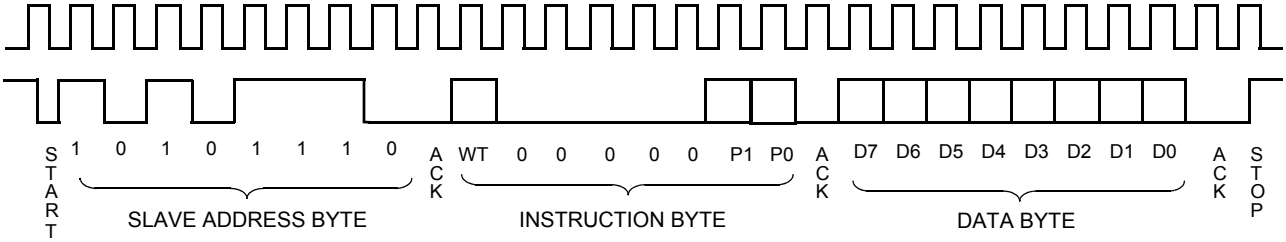


Figure 9. DCP Write Command Sequence

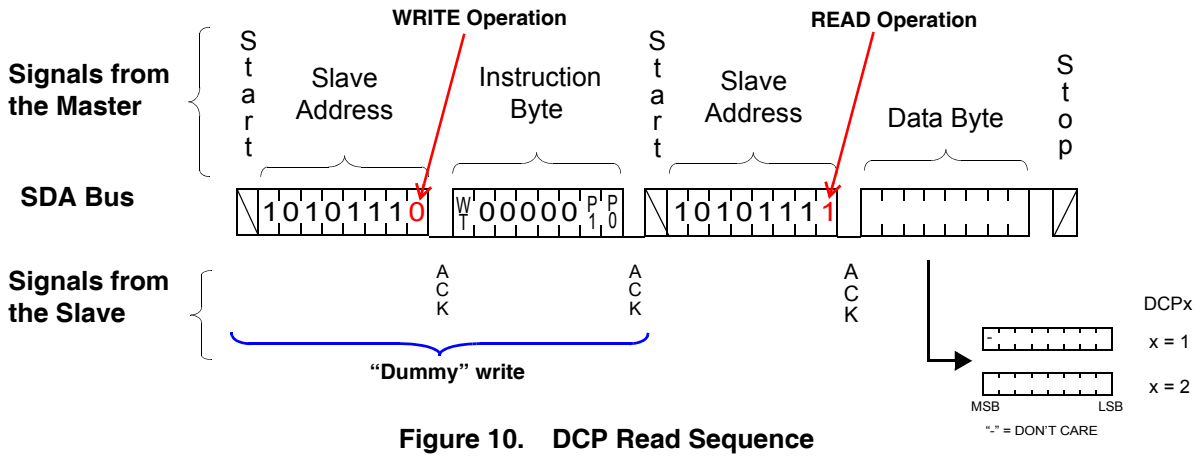


Figure 10. DCP Read Sequence

It should be noted that all writes to any DCP of the X9523 are random in nature. Therefore, the Data Byte of consecutive write operations to any DCP can differ by an arbitrary number of bits. Also, setting the bits P1 = 1, P0 = 1 is a reserved sequence, and will result in no ACKNOWLEDGE after sending an Instruction Byte on SDA.

The factory default setting of all "wiper position" settings is with 00h stored in the NVM of the DCPs. This corresponds to having the "wiper teminal" R_{WX} (x = 1,2) at the "lowest" tap position, Therefore, the resistance between R_{WX} and R_{LX} is a minimum (essentially only the Wiper Resistance, R_W).

DCP Read Operation

A read of DCPx (x = 1,2) can be performed using the three byte random read command sequence shown in Figure 10.

The master issues the START condition and the Slave Address Byte 10101110 which specifies that a "dummy" write" is to be conducted. This "dummy" write operation sets which DCP is to be read (in the preceding Read operation). An ACKNOWLEDGE is returned by the X9523 after the Slave Address if received correctly. Next, an Instruction Byte is issued on SDA. Bits P1-P0 of the Instruction Byte determine which DCP "wiper position" is to be read. In this case, the state of the WT bit is "don't care". If the Instruction Byte format is valid, then another ACKNOWLEDGE is returned by the X9523.

Following this ACKNOWLEDGE, the master immediately issues another START condition and a valid Slave address byte with the R/$\overline{W}$ bit set to 1. Then the X9523 issues an ACKNOWLEDGE followed by Data Byte, and finally, the master issues a STOP condition. The Data Byte read in this operation, corresponds to the "wiper position" (value of the WCR) of the DCP pointed to by bits P1 and P0.

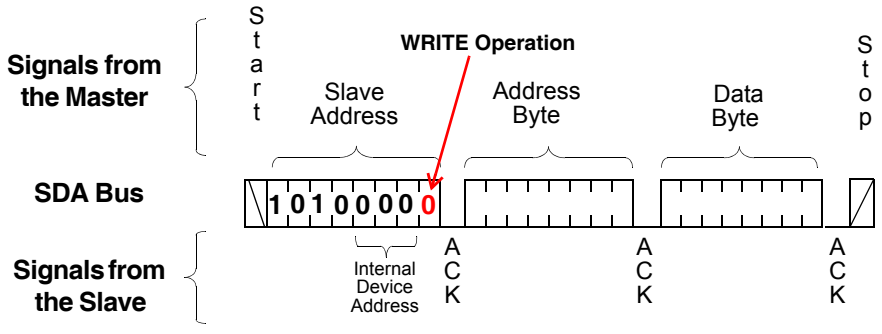
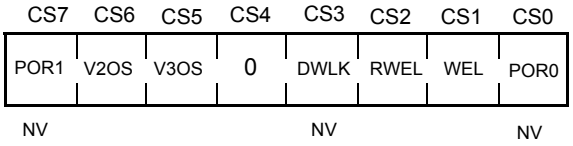


Figure 11. EEPROM Byte Write Sequence



Bit(s)	Description
POR1	Power-on Reset bit
V2OS	V2 Output Status flag
V1OS	V1 Output Status flag
CS4	Always set to “0” (RESERVED)
DWLK	Sets the DCP Write Lock
RWEL	Register Write Enable Latch bit
WEL	Write Enable Latch bit
POR0	Power-on Reset bit

NOTE: Bits labelled NV are nonvolatile (See “CONTROL AND STATUS REGISTER”).

Figure 12. CONSTAT Register Format

It should be noted that when reading out the data byte for DCP1 (100 Tap), the upper most significant bit is an “unknown”. For DCP2 (256 Tap) however, all bits of the data byte are relevant (See Figure 10).

CONTROL AND STATUS REGISTER

The Control and Status (CONSTAT) Register provides the user with a mechanism for changing and reading the status of various parameters of the X9523 (See Figure 12).

The CONSTAT register is a combination of both volatile and nonvolatile bits. The nonvolatile bits of the CONSTAT register retain their stored values even when V1/Vcc is powered down, then powered back up. The volatile bits however, will always power-up to a known logic state “0” (irrespective of their value at power-down).

A detailed description of the function of each of the CONSTAT register bits follows:

WEL: Write Enable Latch (Volatile)

The WEL bit controls the Write Enable status of the entire X9523 device. This bit must first be enabled before ANY write operation (to DCPs, or the CONSTAT register). If the WEL bit is not first enabled, then ANY proceeding (volatile or nonvolatile) write operation to DCPs or the CONSTAT register, is aborted and no ACKNOWLEDGE is issued after a Data Byte.

The WEL bit is a volatile latch that powers up in the disabled, LOW (0) state. The WEL bit is enabled / set by writing 00000010 to the CONSTAT register. Once enabled, the WEL bit remains set to “1” until either it is reset to “0” (by writing 00000000 to the CONSTAT register) or until the X9523 powers down, and then up again.

Writes to the WEL bit do not cause an internal high voltage write cycle. Therefore, the device is ready for another operation immediately after a STOP condition is executed in the CONSTAT Write command sequence (See Figure 13).

RWEL: Register Write Enable Latch (Volatile)

The RWEL bit controls the (CONSTAT) Register Write Enable status of the X9523. Therefore, in order to write to any of the bits of the CONSTAT Register (except WEL), the RWEL bit must first be set to “1”. The RWEL bit is a volatile bit that powers up in the disabled, LOW (“0”) state.

It must be noted that the RWEL bit can only be set, once the WEL bit has first been enabled (See "CONSTAT Register Write Operation").

The RWEL bit will reset itself to the default “0” state, in one of two cases:

—After a successful write operation to any bits of the CONSTAT register has been completed (See Figure 13).

—When the X9523 is powered down.

DWLK: DCP Write Lock bit - (Nonvolatile)

The DCP Write Lock bit (DWLK) is used to inhibit a DCP write operation (changing the “wiper position”).

When the DCP Write Lock bit of the CONSTAT register is set to “1”, then the “wiper position” of the DCPs cannot be changed - i.e. DCP write operations cannot be conducted:

DWLK	DCP Write Operation Permissible
0	YES (Default)
1	NO

The factory default setting for this bit is DWLK = 0.

IMPORTANT NOTE: If the Write Protect (WP) pin of the X9523 is active (HIGH), then nonvolatile write operations to the DCPs are inhibited, irrespective of the DCP Write Lock bit setting (See "WP: Write Protection Pin").

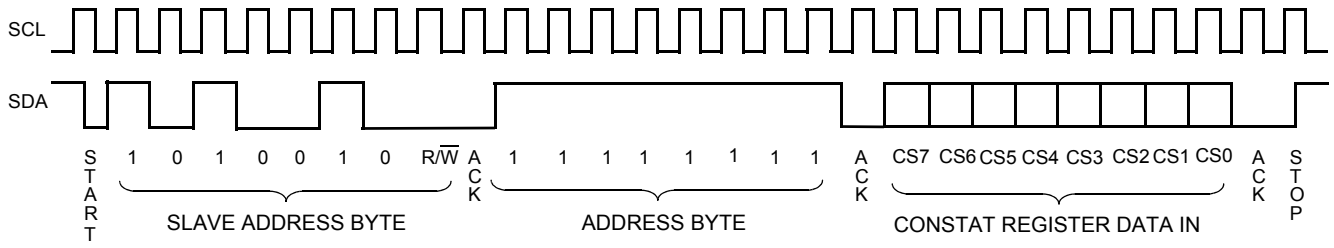


Figure 13. CONSTAT Register Write Command Sequence

POR1, POR0: Power-on Reset bits - (Nonvolatile)

Applying voltage to V_{CC} activates the Power-on Reset circuit which holds V1RO output HIGH, until the supply voltage stabilizes above the V_{TRIP1} threshold for a period of time, t_{PURST} (See Figure 25).

The Power-on Reset bits, POR1 and POR0 of the CONSTAT register determine the tPURST delay time of the Power-on Reset circuitry (See "VOLTAGE MONITORING FUNCTIONS"). These bits of the CONSTAT register are nonvolatile, and therefore power-up to the last written state.

The nominal Power-on Reset delay time can be selected from the following table, by writing the appropriate bits to the CONSTAT register:

POR1	POR0	Power-on Reset delay (t_{PUV1RO})
0	0	50ms
0	1	100ms (Default)
1	0	200ms
1	1	300ms

The default for these bits are POR1 = 0, POR0 = 1.

V2OS, V3OS: Voltage Monitor Status Bits (Volatile)

Bits V2OS and V3OS of the CONSTAT register are latched, volatile flag bits which indicate the status of the Voltage Monitor reset output pins V2RO and V3RO.

At power-up the VxOS (x = 2,3) bits default to the value “0”. These bits can be set to a “1” by writing the appropriate value to the CONSTAT register. To provide consistency between the VxRO and VxOS however, the status of the VxOS bits can only be set to a “1” when the corresponding VxRO output is HIGH.

Once the VxOS bits have been set to “1”, they will be reset to “0” if:

—The device is powered down, then back up,

—The corresponding VxRO output becomes LOW.

CONSTAT Register Write Operation

The CONSTAT register is accessed using the Slave Address set to 1010010 (Refer to Figure 4.). Following the Slave Address Byte, access to the CONSTAT register requires an Address Byte which must be set to FFh. Only one data byte is allowed to be written for each CONSTAT register Write operation. The user must issue a STOP, after sending this byte to the register, to initiate the nonvolatile cycle that stores the DWLK, POR1 and POR0 bits. The X9523 will not ACKNOWLEDGE any data bytes written after the first byte is entered (Refer to Figure 13.).

When writing to the CONSTAT register, the bit CS4 must always be set to “0”. Writing a “1” to bit CS4 of the CONSTAT register is a reserved operation.

Prior to writing to the CONSTAT register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps

—Write a 02H to the CONSTAT Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceded by a START and ended with a STOP).

—Write a 06H to the CONSTAT Register to set the Register Write Enable Latch (RWEL) AND the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceded by a START and ended with a STOP).

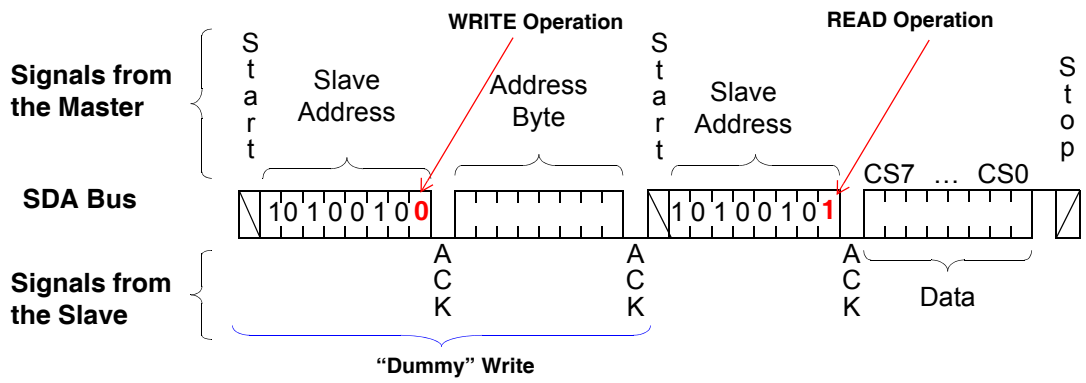


Figure 14. CONSTAT Register Read Command Sequence

—Write a one byte value to the CONSTAT Register that has all the bits set to the desired state. The CONSTAT register can be represented as qxyst01r in binary, where xy are the Voltage Monitor Output Status (V2OS and V3OS) bits, t is the DCP Write Lock (DWLK) bit, and qr are the Power-on Reset delay time (t_{PUV1RO}) control bits (POR1 - POR0). This operation is proceeded by a START and ended with a STOP bit. Since this is a nonvolatile write cycle, it will typically take 5ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (qxys t11r) then the RWEL bit is set, but the V2OS, V3OS, POR1, POR0, and DWLK bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and the X9523 does not return an ACKNOWLEDGE.

For example, a sequence of writes to the device CONSTAT register consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the CONSTAT Register to "0".

It should be noted that a write to any nonvolatile bit of CONSTAT register will be ignored if the Write Protect pin of the X9523 is active (HIGH) (See "WP: Write Protection Pin").

CONSTAT Register Read Operation

The contents of the CONSTAT Register can be read at any time by performing a random read (See Figure 14). Using the Slave Address Byte set to 10100101, and an Address Byte of FFh. Only one byte is read by each register read operation. The X9523 resets itself after the first byte is read. The master should supply a STOP condition to be consistent with the bus protocol.

After setting the WEL and / or the RWEL bit(s) to a “1”, a CONSTAT register read operation may occur, without interrupting a proceeding CONSTAT register write operation.

When performing a read operation on the CONSTAT registerm, bit CS4 will always return a “0” value.

DATA PROTECTION

There are a number of levels of data protection features designed into the X9523. Any write to the device first requires setting of the WEL bit in the CONSTAT register. A write to the CONSTAT register itself, further requires the setting of the RWEL bit. DCP Write Lock protection of the device enables the user to inhibit writes to all the DCPs. One further level of data protection in the X9523, is incorporated in the form of the Write Protection pin.

X9523 Write Permission Status

DWLK (DCP Write Lock bit status)	WP (Write Protect pin status)	DCP Volatile Write Permitted	DCP Nonvolatile Write Permitted	Write to CONSTAT Register Permitted	
				Volatile Bits	Nonvolatile Bits
1	1	NO	NO	NO	NO
0	1	YES	NO	NO	NO
1	0	NO	NO	YES	YES
0	0	YES	YES	YES	YES

WP: Write Protection Pin

When the Write Protection (WP) pin is active (HIGH), it disables nonvolatile write operations to the X9523.

The table (X9523 Write Permission Status) summarizes the effect of the WP pin (and DCP Write Lock), on the write permission status of the device.

Additional Data Protection Features

In addition to the preceding features, the X9523 also incorporates the following data protection functionality:

—The proper clock count and data bit sequence is required prior to the STOP bit in order to start a nonvolatile write cycle.

VOLTAGE MONITORING FUNCTIONS

V1 / Vcc Monitoring

The X9523 monitors the supply voltage and drives the V1RO output HIGH (using an external “pull up” resistor) if V1/Vcc is lower than V_{TRIP1} threshold. The V1RO output will remain HIGH until V1/Vcc exceeds V_{TRIP1} for a minimum time of t_{PURST}. After this time, the V1RO pin is driven to a LOW state. See Figure 25.

For the Power-on/Low Voltage Reset function of the X9523, the V1RO output may be driven HIGH down to a V1/Vcc of 1V (V_{RVALID}). See Figure 25. Another feature of the X9523, is that the value of t_{PURST} may be selected in software via the CONSTAT register (See “POR1, POR0: Power-on Reset bits - (Nonvolatile)” on page 11.).

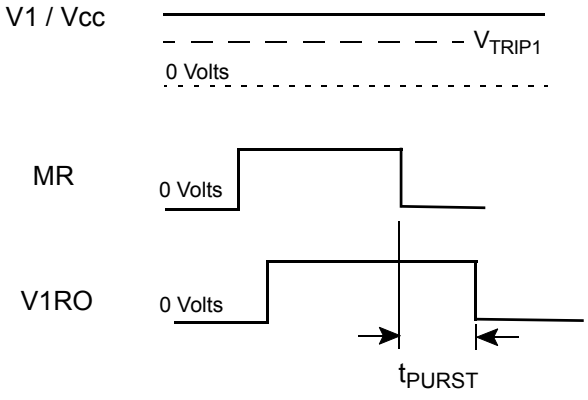


Figure 15. Manual Reset Response

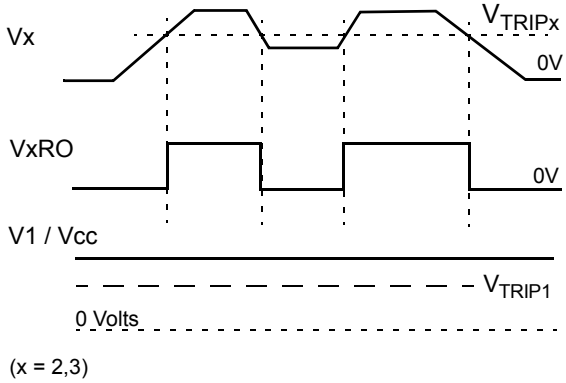


Figure 16. Voltage Monitor Response

It is recommended to stop communication to the device while while V1RO is HIGH. Also, setting the Manual Reset (MR) pin HIGH overrides the Power-on/Low Voltage circuitry and forces the V1RO output pin HIGH (See "Manual Reset").

Manual Reset

The V1RO output can be forced HIGH externally using the Manual Reset (MR) input. MR is a de-bounced, TTL compatible input, and so it may be operated by connecting a push-button directly from V1/Vcc to the MR pin.

V1RO remains HIGH for time t_{PURST} after MR has returned to its LOW state (See Figure 15). An external “pull down” resistor is required to hold this pin (normally) LOW.

V2 monitoring

The X9523 asserts the V2RO output HIGH if the voltage V2 exceeds the corresponding V_{TRIP2} threshold (See Figure 16). The bit V2OS in the CONSTAT register is then set to a “0” (assuming that it has been set to “1” after system initilization).

The V2RO output may remain active HIGH with V_{CC} down to 1V.

V3 monitoring

The X9523 asserts the V3RO output HIGH if the voltage V3 exceeds the corresponding V_{TRIP3} threshold (See Figure 16). The bit V3OS in the CONSTAT register is then set to a “0” (assuming that it has been set to “1” after system initilization).

The V3RO output may remain active HIGH with V_{CC} down to 1V.

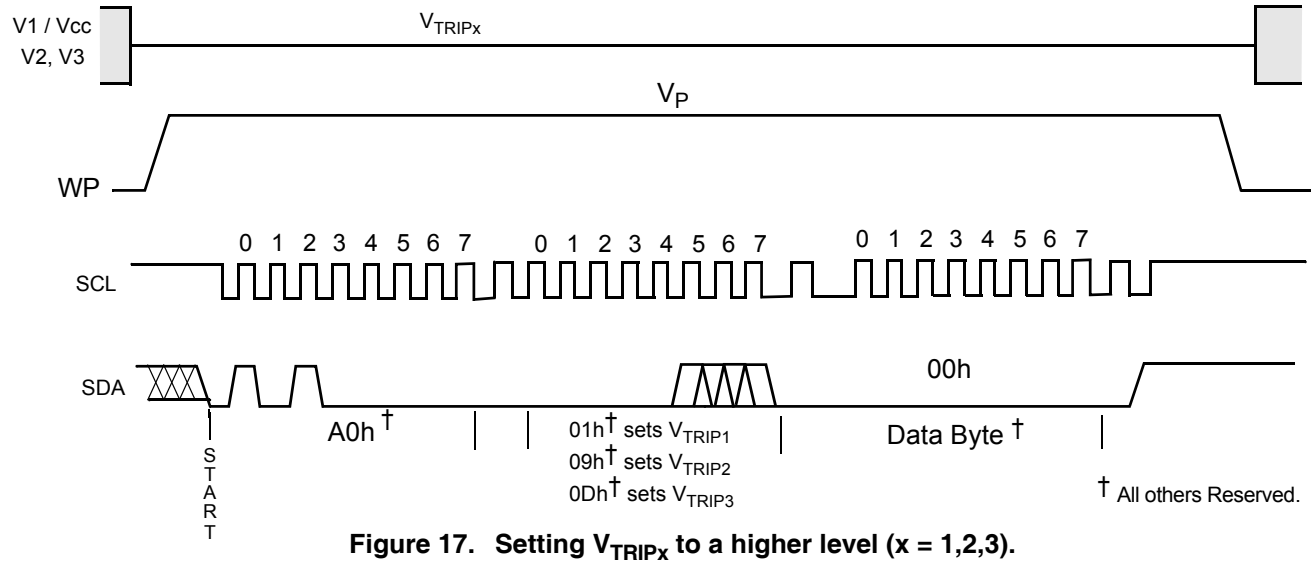


Figure 17. Setting V_{TRIPx} to a higher level (x = 1,2,3).

V_{TRIPX} THRESHOLDS (X = 1,2,3)

The X9523 is shipped with pre-programmed threshold (V_{TRIPx}) voltages. In applications where the required thresholds are different from the default values, or if a higher precision/tolerance is required, the X9523 trip points may be adjusted by the user, using the steps detailed below.

Setting a V_{TRIPx} Voltage (x = 1,2,3)

There are two procedures used to set the threshold voltages (V_{TRIPx}), depending if the threshold voltage to be stored is higher or lower than the present value. For example, if the present V_{TRIPx} is 2.9 V and the new V_{TRIPx} is 3.2 V, the new voltage can be stored directly into the V_{TRIPx} cell. If however, the new setting is to be lower than the present setting, then it is necessary to “reset” the V_{TRIPx} voltage before setting the new value.

Setting a Higher V_{TRIPx} Voltage (x = 1,2,3)

To set a V_{TRIPx} threshold to a new voltage which is higher than the present threshold, the user must apply the desired V_{TRIPx} threshold voltage to the corresponding input pin (V1/Vcc, V2 or V3). Then, a programming voltage (Vp) must be applied to the WP pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h, followed by the Byte Address 01h for V_{TRIP1}, 09h for V_{TRIP2}, and 0Dh for V_{TRIP3}, and a 00h Data Byte in order to program V_{TRIPx}. The STOP bit following a valid write operation initiates the programming sequence. Pin WP must then be brought LOW to complete the operation (See Figure 18). The user does not have to set the WEL bit in the CONSTAT register before performing this write sequence.

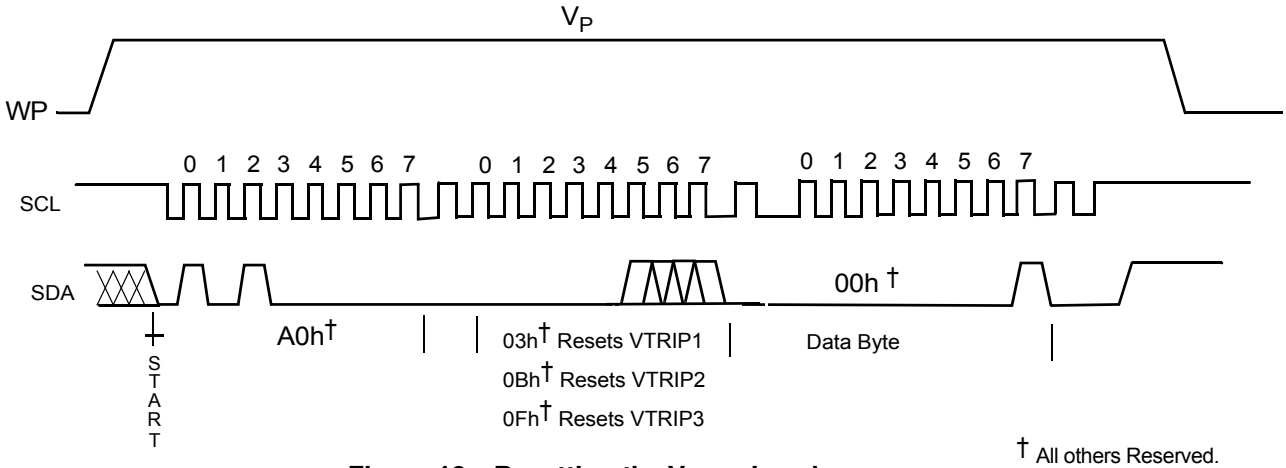


Figure 18. Resetting the V_{TRIPx} Level

Setting a Lower V_{TRIPx} Voltage (x = 1,2,3).

In order to set V_{TRIPx} to a lower voltage than the present value, then V_{TRIPx} must first be “reset” according to the procedure described below. Once V_{TRIPx} has been “reset”, then V_{TRIPx} can be set to the desired voltage using the procedure described in “Setting a Higher V_{TRIPx} Voltage”.

Resetting the V_{TRIPx} Voltage (x = 1,2,3).

To reset a V_{TRIPx} voltage, apply the programming voltage (Vp) to the WP pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h followed by the Byte Address 03h for V_{TRIP1}, 0Bh for V_{TRIP2}, and 0Fh for V_{TRIP3}, followed by 00h for the Data Byte in order to reset V_{TRIPx}. The STOP bit following a valid write operation initiates the programming sequence. Pin WP must then be brought LOW to complete the operation (See Figure 18).The user does not have to set the WEL bit in the CONSTAT register before performing this write sequence.

After being reset, the value of V_{TRIPx} becomes a nominal value of 1.7V.

V_{TRIPx} Accuracy (x = 1,2,3).

The accuracy with which the V_{TRIPx} thresholds are set, can be controlled using the iterative process shown in Figure 19.

If the desired threshold is less that the present threshold voltage, then it must first be “reset” (See "Resetting the VTRIPx Voltage (x = 1,2,3).") .

The desired threshold voltage is then applied to the appropriate input pin (V1/Vcc, V2 or V3) and the procedure described in Section “Setting a Higher V_{TRIPx} Voltage“ must be followed.

Once the desired V_{TRIPx} threshold has been set, the error between the desired and (new) actual set threshold can be determined. This is achieved by applying V1/Vcc to the device, and then applying a test voltage higher than the desired threshold voltage, to the input pin of the voltage monitor circuit whose V_{TRIPx} was programmed. For example, if V_{TRIP2} was set to a desired level of 3.0V, then a test voltage of 3.4 V may be applied to the voltage monitor input pin V2. In the case of setting of V_{TRIP1} then only V1/Vcc need be applied. In all cases, care should be taken not to exceed the maximum input voltage limits.

After applying the test voltage to the voltage monitor input pin, the test voltage can be decreased (either in discrete steps, or continuously) until the output of the voltage monitor circuit changes state. At this point, the error between the actua measured, and desired threshold levels is calculated.

For example, the desired threshold for V_{TRIP2} is set to 3.0V, and a test voltage of 3.4V was applied to the input pin V2 (after applying power to V1/Vcc). The input voltage is decreased, and found to trip the associated output level of pin V2RO from a LOW to a HIGH, when V2 reaches 3.09V. From this, it can be calculated that the programming error is 3.09 - 3.0 = 0.09V.

If the error between the desired and measured V_{TRIPx} is less than the maximum desired error, then the programming process may be terminated. If however, the error is greater than the maximum desired error, then another iteration of the V_{TRIPx} programming sequence can be performed (using the calculated error) in order to further increase the accuracy of the threshold voltage.

If the calculated error is greater than zero, then the V_{TRIPx} must first be “reset”, and then programmed to the a value equal to the previously set V_{TRIPx} minus the calculated error. If it is the case that the error is less than zero, then the V_{TRIPx} must be programmed to a value equal to the previously set V_{TRIPx} plus the absolute value of the calculated error.

Continuing the previous example, we see that the calculated error was 0.09V. Since this is greater than zero, we must first “reset” the V_{TRIP2} threshold, then apply a voltage equal to the last previously programmed voltage, minus the last previously calculated error. Therefore, we must apply V_{TRIP2} = 2.91 V to pin V2 and execute the programming sequence (See "Setting a Higher VTRIPx Voltage (x = 1,2,3)") .

Using this process, the desired accuracy for a particular V_{TRIPx} threshold may be attained using a successive number of iterations.

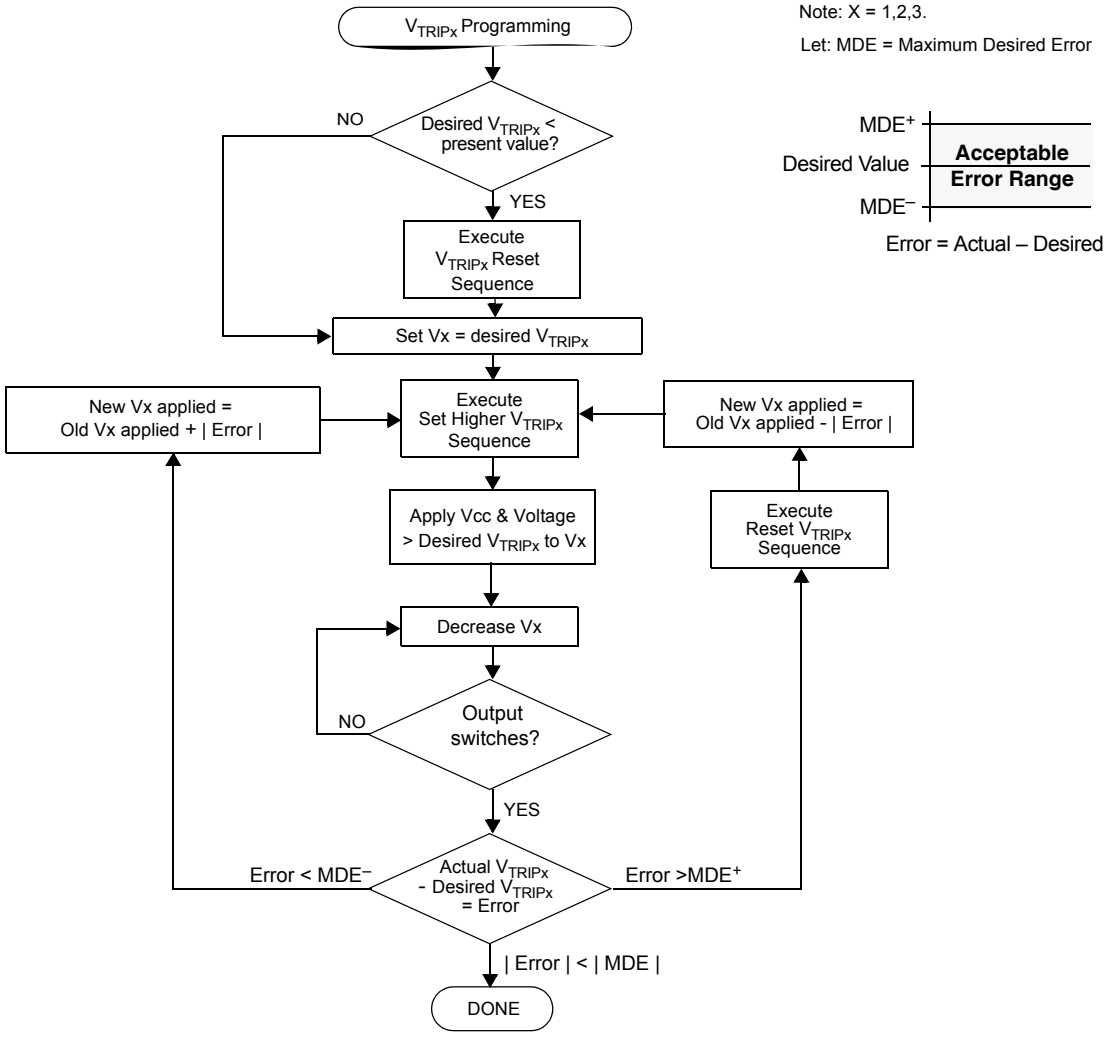


Figure 19. V_{TRIPx} Setting / Reset Sequence (x = 1,2,3)

ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Max.	Units
Temperature under Bias	-65	+135	°C
Storage Temperature	-65	+150	°C
Voltage on WP pin (With respect to Vss)	-1.0	+15	V
Voltage on other pins (With respect to Vss)	-1.0	+7	V
| Voltage on R_{Hx} - Voltage on R_{Lx} | (x = 0,1,2. Referenced to Vss)		V1/Vcc	V
D.C. Output Current (SDA,V1RO,V2RO,V3RO)	0	5	mA
Lead Temperature (Soldering, 10 seconds)		300	°C
Supply Voltage Limits (Applied V1/Vcc voltage, referenced to Vss)	2.7	5.5	V

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.	Units
Industrial	-40	+85	°C

NOTE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 20. Equivalent A.C. Circuit

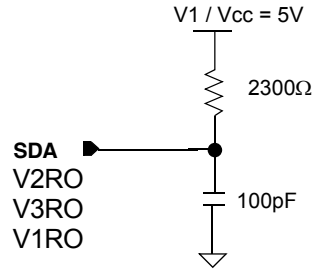
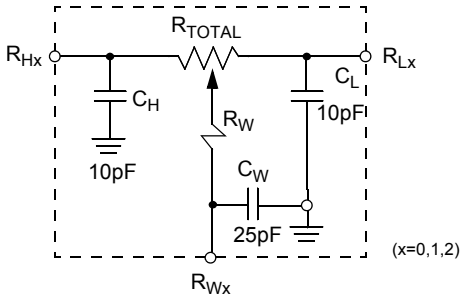


Figure 21. DCP SPICE Macromodel



TIMING DIAGRAMS

Figure 22. Bus Timing

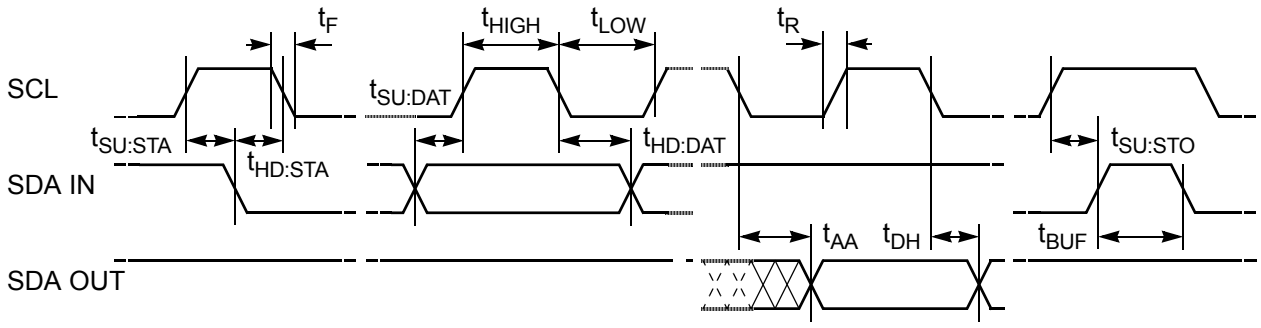


Figure 23. WP Pin Timing

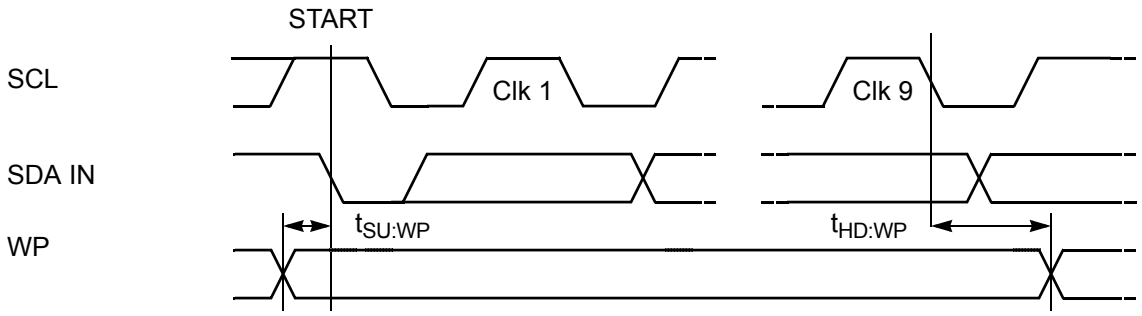


Figure 24. Write Cycle Timing

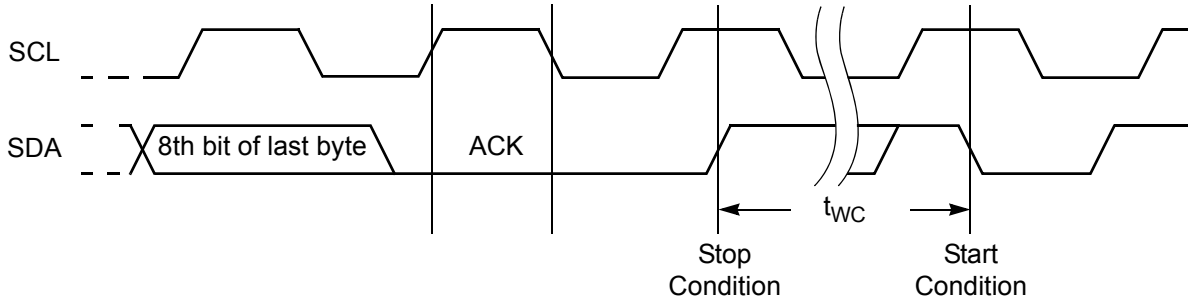


Figure 25. Power-Up and Power-Down Timing

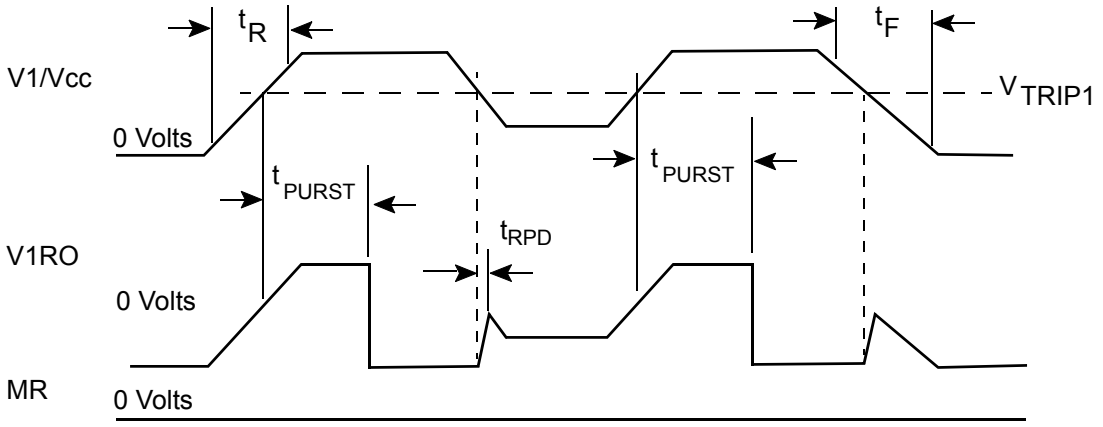


Figure 26. Manual Reset Timing Diagram

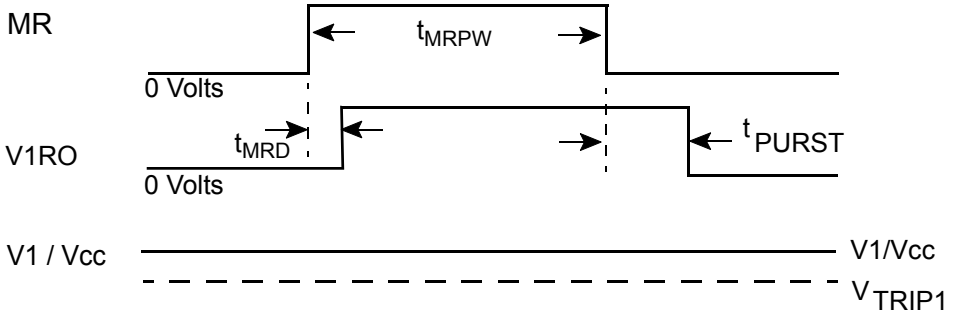
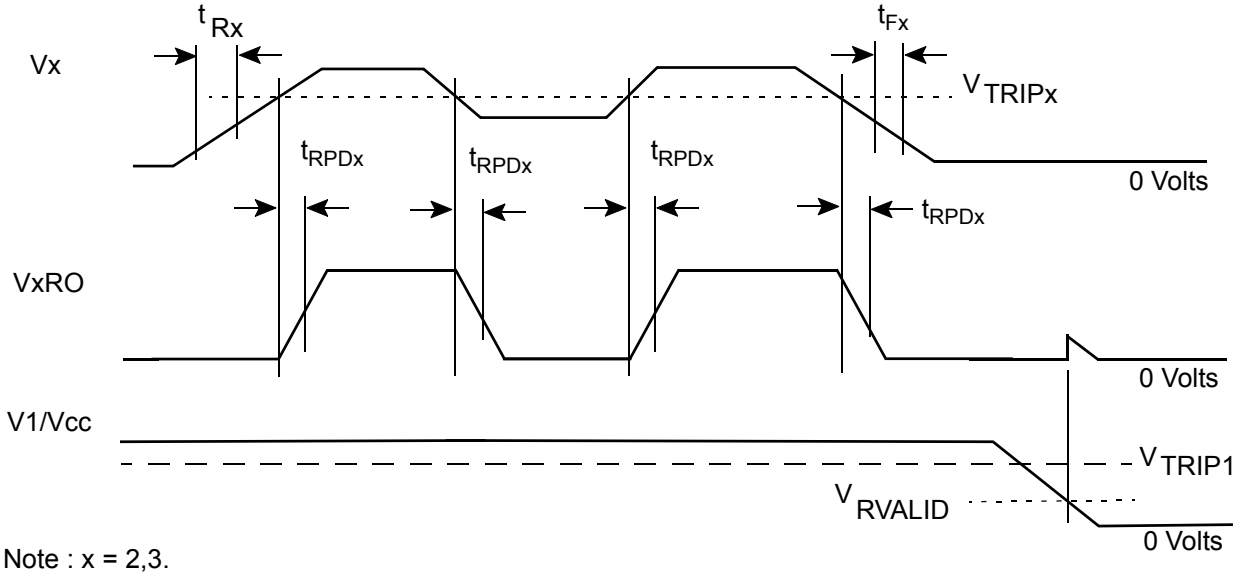


Figure 27. V2, V3 Timing Diagram



Note : x = 2,3.

Figure 28. V_{TRIPX} Programming Timing Diagram (x = 1,2,3).

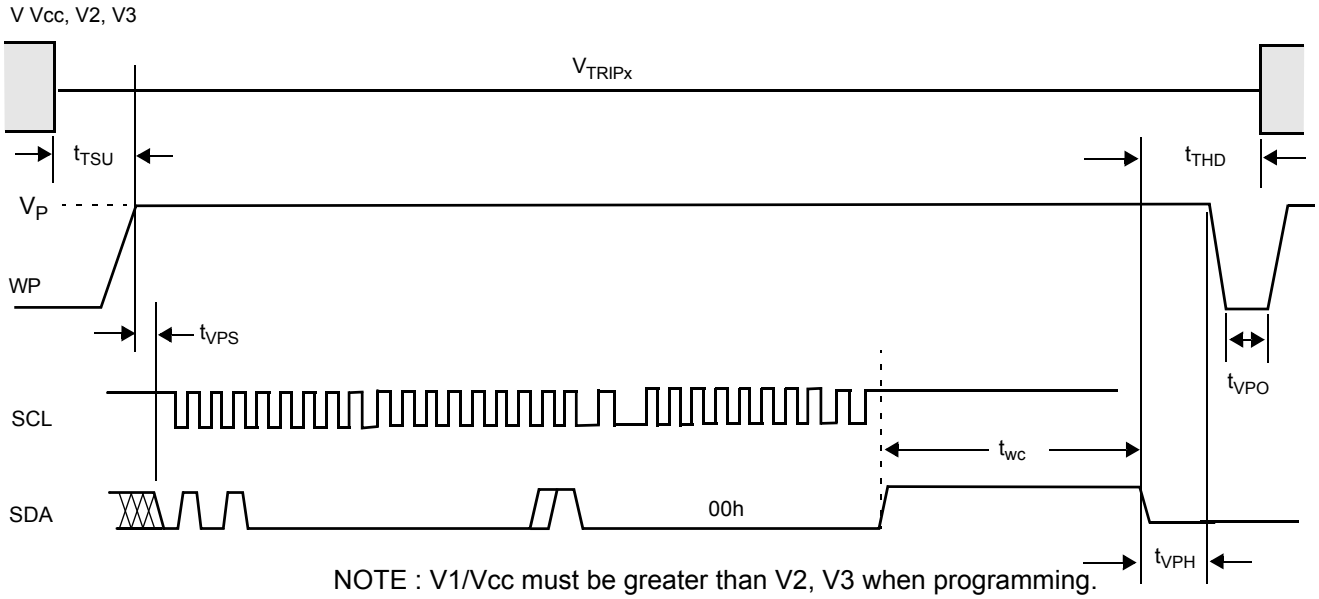
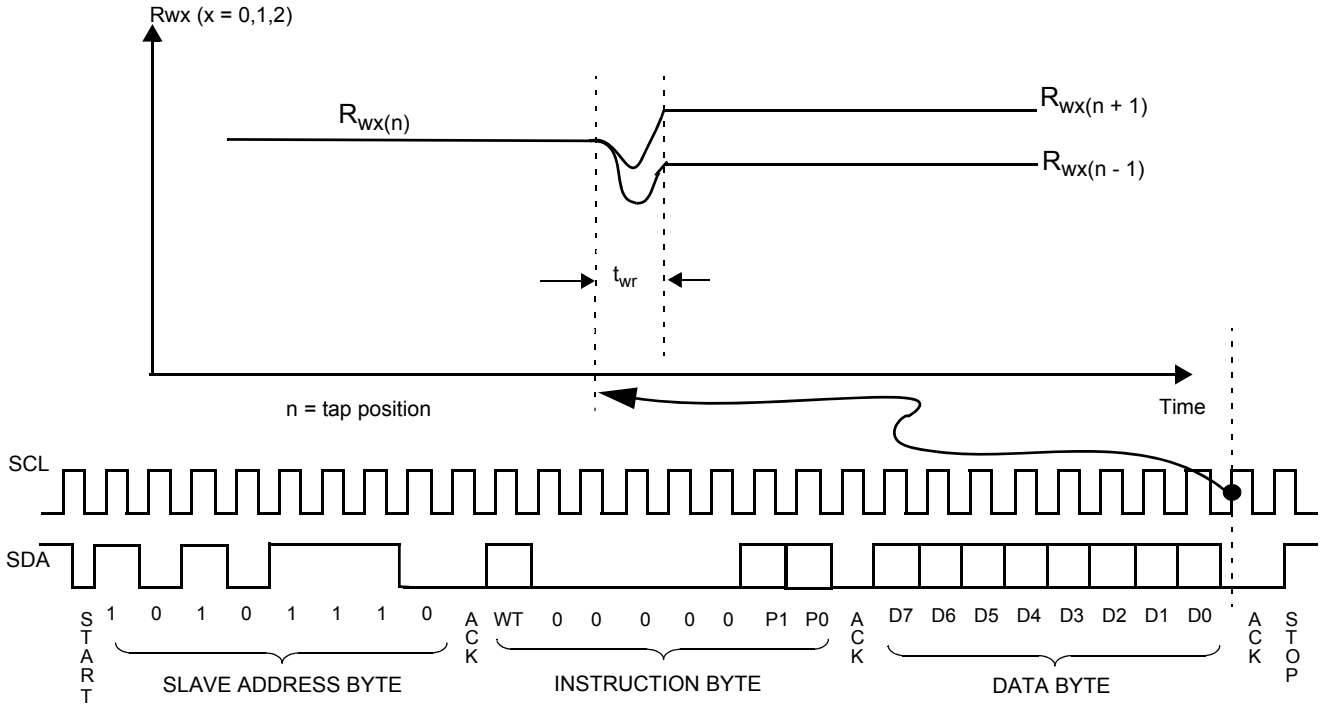


Figure 29. DCP "Wiper Position" Timing



D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions / Notes
I_{CC1} (1)	Current into V_{CC} Pin (X9523: Active) Read memory array (3) Write nonvolatile memory			0.4 1.5	mA	f_{SCL} = 400kHz
I_{CC2} (2)	Current into V_{CC} Pin (X9523:Standby) With 2-Wire bus activity (3) No 2-Wire bus activity			50 50	µA	$V_{SDA} = V_{CC}$ MR = Vss WP = Vss or Open/Floating $V_{SCL} = V_{CC}$ (when no bus activity else f_{SCL} = 400kHz)
I_{LI}	Input Leakage Current (SCL, SDA, MR)		0.1	10	µA	V_{IN} (4) = GND to V_{CC}.
	Input Leakage Current (WP)			10	µA	
I_{ai}	Analog Input Leakage		1	10	µA	$V_{IN} = V_{SS}$ to V_{CC} with all other analog pins floating
I_{LO}	Output Leakage Current (SDA, V1RO, V2RO, V3RO)		0.1	10	µA	V_{OUT} (5) = GND to V_{CC}. X9523 is in Standby(2)
$V_{TRIP1PR}$	V_{TRIP1} Programming Range	2.75		4.70	V	
$V_{TRIPxPR}$	V_{TRIPx} Programming Range (x = 2,3)	1.8		4.70	V	
V_{TRIP1} (6)	Pre - programmed V_{TRIP1} threshold	2.85 4.55	3.0 4.7	3.05 4.75	V	Factory shipped default option A Factory shipped default option B
V_{TRIP2} (6)	Pre - programmed V_{TRIP2} threshold	1.65 2.85	1.8 3.0	1.85 3.05	V	Factory shipped default option A Factory shipped default option B
V_{TRIP3} (6)	Pre - programmed V_{TRIP3} threshold	1.65 2.85	1.8 3.0	1.85 3.05	V	Factory shipped default option A Factory shipped default option B
I_{Vx}	V2 Input leakage current V3 Input leakage current			1 1	µA	$V_{SDA} = V_{SCL} = V_{CC}$ Others=GND or V_{CC}
V_{IL} (7)	Input LOW Voltage (SCL, SDA, WP, MR)	-0.5		0.8	V	
V_{IH} (7)	Input HIGH Voltage (SCL,SDA, WP, MR)	2.0		V_{CC} +0.5	V	
V_{OLx}	V1RO, V2RO, V3RO, SDA Output Low Voltage			0.4	V	I_{SINK} = 2.0mA

Notes: 1. The device enters the Active state after any START, and remains active until: 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200nS after a STOP ending a read operation; or t_{WC} after a STOP ending a write operation.

Notes: 2.The device goes into Standby: 200nS after any STOP, except those that initiate a high voltage write cycle; t_{WC} after a STOP that initiates a high voltage cycle; or 9 clock cycles after any START that is not followed by the correct Device Select Bits in the Slave Address Byte.

Notes: 3.Current through external pull up resistor not included.

Notes: 4.V_{IN} = Voltage applied to input pin.

Notes: 5.V_{OUT} = Voltage applied to output pin.

Notes: 6.See Ordering Information on page 2.

Notes: 7.V_{IL} Min. and V_{IH} Max. are for reference only and are not tested

A.C. CHARACTERISTICS (See Figure 22, Figure 23, Figure 24)

Symbol	Parameter	400kHz		
		Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	400	kHz
t_{IN}(5)	Pulse width Suppression Time at inputs	50		ns
t_{AA}(5)	SCL LOW to SDA Data Out Valid	0.1	0.9	µs
t_{BUF}(5)	Time the bus free before start of new transmission	1.3		µs
t_{LOW}	Clock LOW Time	1.3		µs
t_{HIGH}	Clock HIGH Time	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	0.6		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
$t_{SU:DAT}$	Data In Setup Time	100		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}(5)	Data Output Hold Time	50		ns
t_R (5)	SDA and SCL Rise Time	20 +.1Cb (2)	300	ns
t_F (5)	SDA and SCL Fall Time	20 +.1Cb (2)	300	ns
$t_{SU:WP}$	WP Setup Time	0.6		µs
$t_{HD:WP}$	WP Hold Time	0		µs
Cb(5)	Capacitive load for each bus line		400	pF

A.C. TEST CONDITIONS

Input Pulse Levels	$0.1V_{CC}$ to $0.9V_{CC}$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$0.5V_{CC}$
Output Load	See Figure 20

NONVOLATILE WRITE CYCLE TIMING

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}(4)	Nonvolatile Write Cycle Time		5	10	ms

CAPACITANCE (T_A = 25°C, F = 1.0 MHZ, V_{CC} = 5V)

Symbol	Parameter	Max	Units	Test Conditions
C_{OUT} (5)	Output Capacitance (SDA, V1RO, V2RO, V3RO)	8	pF	V_{OUT} = 0V
C_{IN} (5)	Input Capacitance (SCL, WP, MR)	6	pF	V_{IN} = 0V

Notes: 1.Typical values are for T_A = 25°C and V_{CC} = 5.0V

Notes: 2.Cb = total capacitance of one bus line in pF.

Notes: 3.Over recommended operating conditions, unless otherwise specified

Notes: 4.t_{WC} is the time from a valid STOP condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

Notes: 5.This parameter is not 100% tested.

POTENTIOMETER CHARACTERISTICS

Symbol	Parameter	Limits				Test Conditions/Notes
		Min.	Typ.	Max.	Units	
R_{TOL}	End to End Resistance Tolerance	-20		+20	%	
V_{RHx}	R_H Terminal Voltage (x = 0,1,2)	Vss		V_{CC}	V	
V_{RLx}	R_L Terminal Voltage (x = 0,1,2)	Vss		V_{CC}	V	
P_R	Power Rating (1)(6)			10	mW	R_{TOTAL} = 10kΩ (DCP0, DCP1)
				5	mW	R_{TOTAL} = 100kΩ (DCP2)
R_W	DCP Wiper Resistance		200	400	Ω	I_W = 1mA, V_{CC} = 5V, V_{RHx} = Vcc, V_{RLx} = Vss (x = 0,1,2).
			400	1200	Ω	I_W = 1mA, V_{CC} = 2.7V, V_{RHx} = Vcc, V_{RLx} = Vss (x = 0,1,2)
I_W	Wiper Current (6)			4.4	mA	
	Noise				mV/ sqt(Hz)	R_{TOTAL} = 10kΩ (DCP0, DCP1)
					mV/ sqt(Hz)	R_{TOTAL} = 100kΩ (DCP2)
	Absolute Linearity (2)	-1		+1	MI(4)	$R_{w(n)(actual)} - R_{w(n)(expected)}$
	Relative Linearity (3)	-1		+1	MI(4)	$R_{w(n+1)} - [R_{w(n)} + MI]$
	R_{TOTAL} Temperature Coefficient		±300		ppm/°C	R_{TOTAL} = 10kΩ (DCP0, DCP1)
			±300		ppm/°C	R_{TOTAL} = 100kΩ (DCP2)
$C_H/C_L/C_W$	Potentiometer Capacitances		10/10/25		pF	See Figure 21.
t_{wr}	Wiper Response time(6)			200	µs	See Figure 29.

Notes: 1.Power Rating between the wiper terminal $R_{WX(n)}$ and the end terminals R_{HX} or R_{LX} - for ANY tap position n, (x = 0,1,2).

Notes: 2.Absolute Linearity is utilized to determine actual wiper resistance versus, expected resistance = ($R_{wx(n)}$(actual) - $R_{wx(n)}$(expected)) = ±1 MI Maximum (x = 0,1,2).

Notes: 3.Relative Linearity is a measure of the error in step size between taps = $R_{Wx(n+1)} - [R_{wx(n)} + MI]$ = ±1 MI (x = 0,1,2)

Notes: 4.1 MI = Minimum Increment = R_{TOT} / (Number of taps in DCP - 1).

Notes: 5.Typical values are for T_A = 25°C and nominal supply voltage.

Notes: 6.This parameter is periodically sampled and not 100% tested.

V_{TRIPX} (X = 1,2,3) PROGRAMMING PARAMETERS (See Figure 28)

Parameter	Description	Min	Typ	Max	Units
t_{VPS}	V_{TRIPx} Program Enable Voltage Setup time	10			µs
t_{VPH}	V_{TRIPx} Program Enable Voltage Hold time	10			µs
t_{TSU}	V_{TRIPx} Setup time	10			µs
t_{THD}	V_{TRIPx} Hold (stable) time	10			µs
t_{VPO}	V_{TRIPx} Program Enable Voltage Off time (Between successive adjustments)	1			ms
t_{wc}	V_{TRIPx} Write Cycle time		5	10	ms
V_P	Programming Voltage	10		15	V
V_{ta}	V_{TRIPx} Program Voltage accuracy (Programmed at 25ºC.)	-100		+100	mV
V_{tv}	V_{TRIP} Program variation after programming (-40 - 85ºC). (Programmed at 25ºC.)	-25	+10	+25	mV

Notes: The above parameters are not 100% tested.

V1RO, V2RO, V3RO OUTPUT TIMING. (See Figure 25, Figure 26, Figure 27)

Symbol	Description	Condition	Min.	Typ.	Max.	Units
t_{PURST}(5)	Power-on Reset delay time	POR1 = 0, POR0 = 0	25	50	75	ms
		POR1 = 0, POR0 = 1	50	100	150	ms
		POR1 = 1, POR0 = 0	100	200	300	ms
		POR1 = 1, POR0 = 1	150	300	450	ms
t_{MRD} (26)(2)(5)	MR to V1RO propagation delay	See (1)(2)(4)			5	µs
t_{MRDPW}(5)	MR pulse width		500			ns
t_{RPDx}(5)	V Vcc, V2, V3 to V1RO, V2RO, V3RO propagation delay (respectively)				20	µs
t_{Fx}(5)	V1/Vcc, V2, V3 Fall Time		20			mV/µs
t_{Rx}(5)	V1/Vcc, V2, V3 Rise Time		20			mV/µs
V_{RVALID}(5)	V1/Vcc for V1RO, V2RO, V3RO Valid (3).		1			V

Notes: 1.See Figure 26 for timing diagram.

Notes: 2.See Figure 20 for equivalent load.

Notes: 3.This parameter describes the lowest possible V1/Vcc level for which the outputs V1RO, V2RO, and V3RO will be correct with respect to their inputs (V1/Vcc, V2, V3).

Notes: 4.From MR rising edge crossing V_{IH}, to V1RO rising edge crossing V_{OH}.

Notes: 5.The above parameters are not 100% tested.