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XA Spartan-3A DSP Automotive FPGA Family Data Sheet

DS705 (v2.0) April 18, 2011 **Product Specification**

Summary

The Xilinx Automotive (XA) Spartan®-3A DSP family of FPGAs solves the design challenges in most high-volume, cost-sensitive, high-performance DSP automotive applications. The two-member family offers densities ranging from 1.8 to 3.4 million system gates, as shown in Table 1.

Introduction

XA devices are available in both extended-temperature Q-Grade (–40°C to +125°C T_J) and I-Grade (–40°C to +100°C T_J) and are qualified to the industry recognized AEC-Q100 standard.

The XA Spartan-3A DSP family builds on the success of the earlier XA Spartan-3E and XA Spartan-3 FPGA families by adding hardened DSP MACs with pre-adders, significantly increasing the throughput and performance of this low-cost family. These XA Spartan-3A DSP family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost,
XA Spartan-3A DSP FPGAs are ideally suited to a wide range of automotive electronics applications, including infotainment, driver information, and driver assistance modules.

The XA Spartan-3A DSP family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial mask set costs and lengthy development cycles, while also permitting design upgrades in the field with no hardware replacement necessary because of its inherent programmability, an impossibility with conventional ASICs and ASSPs with their inflexible architecture.

Features

- Very low cost, high-performance DSP solution for high-volume, cost-conscious applications
- 250 MHz DSP48A slices using XtremeDSP™ solution
  - Dedicated 18-bit by 18-bit multiplier
  - Available pipeline stages for enhanced performance of at least 250 MHz in the standard -4 speed grade
  - 48-bit accumulator for multiply-accumulate (MAC) operation
  - Integrated adder for complex multiply or multiply-add operation
  - Integrated 18-bit pre-adder
  - Optional cascaded Multiply or MAC
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend and Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 519 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ± 10% compatibility and hot-swap compliance
  - 622+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 266 Mb/s
  - Fully compliant 32-bit, 33 MHz PCI® technology support
- Abundant, flexible logic resources
  - Densities up to 53,712 logic cells, including optional shift register
  - Efficient wide multiplexers, wide logic
  - Fast look-ahead carry logic
  - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
  - Up to 2,268 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 373 Kbits of efficient distributed RAM
  - Registered outputs on the block RAM with operation of at least 280 MHz in the standard -4 speed grade
- Eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 parallel NOR Flash PROM
  - Unique Device DNA identifier for design authentication
- Complete Xilinx ISE® and WebPACK™ software support plus Spartan-3A DSP FPGA Starter Kit
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- BGA packaging, Pb-free only
  - Common footprints support easy density migration

Table 1: **Summary of XA Spartan-3A DSP FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM Bits (1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XA3SD1800A	1800K	37,440	88	48	4,160	16,640	260K	1512K	84	8	519	227
XA3SD3400A	3400K	53,712	104	58	5,968	23,872	373K	2268K	126	8	469	213

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

Refer to DS610, *Spartan-3A DSP FPGA Family Data Sheet* for a full product description, AC and DC specifications, and package pinout descriptions. Any values shown specifically in this XA Spartan-3A DSP Automotive FPGA Family data sheet override those shown in DS610.

For information regarding reliability qualification, refer to RPT103, *Xilinx Spartan-3A Family Automotive Qualification Report* and RPT070, *Spartan-3A Commercial Qualification Report*. Contact your local Xilinx representative for more details on these reports.

Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specifications over the T_J = –40°C to +125°C temperature range (Q-Grade)
- XA Spartan-3A DSP devices are available in the -4 speed grade only
- PCI-66 and PCI-X are not supported in the XA Spartan-3A DSP FPGA product line
- Platform Flash is not supported within the XA family
- XA Spartan-3A DSP devices are available in Pb-free packaging only
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3A DSP device must be power cycled prior to reconfiguration.

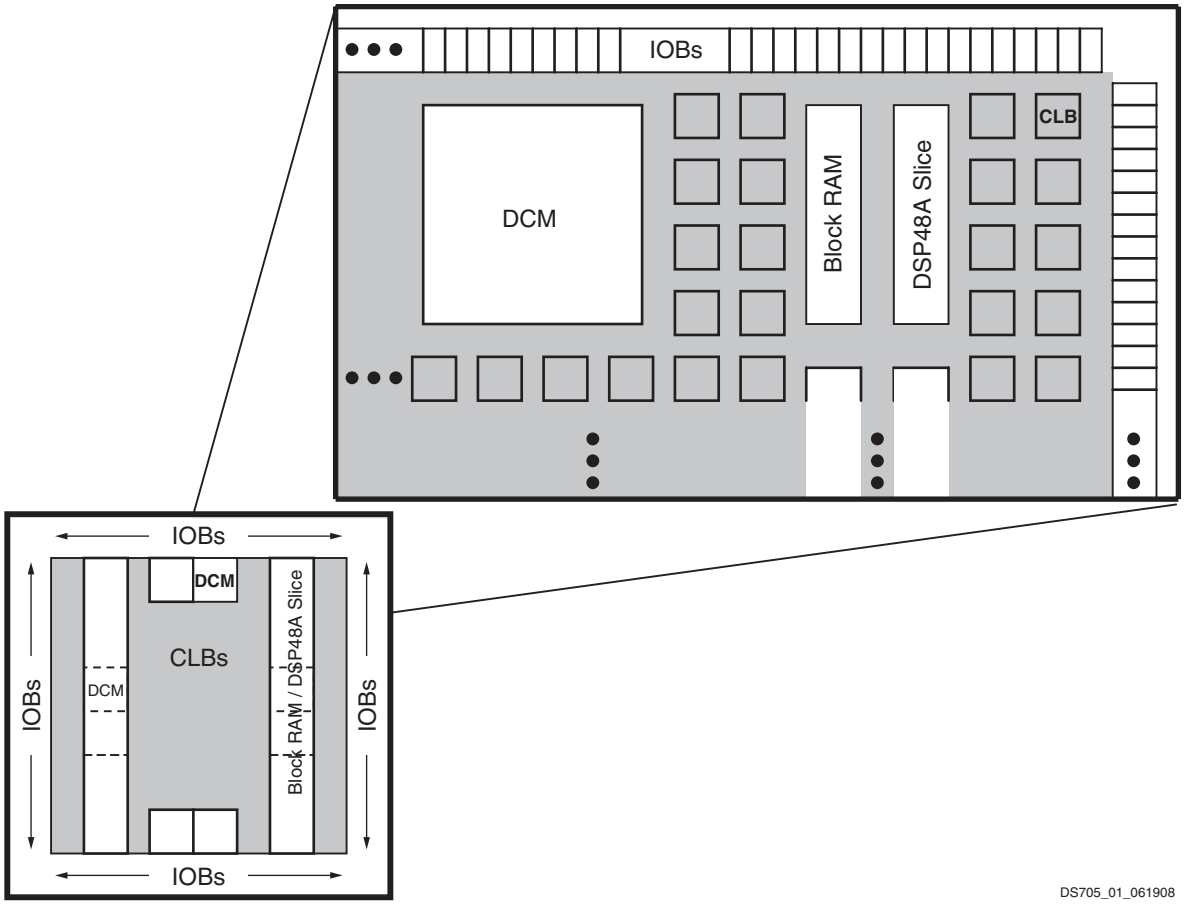
Architectural Overview

The XA Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kb dual-port blocks.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XA3SD1800A has four columns of DSP48A slices, and the XA3SD3400A has five columns of DSP48A slices. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the four or five columns of block RAM and DSP48As.

The XA Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XA3SD1800A and XA3SD3400A have two DCMs on both the left and right sides, as well as the two DCMs at the top and bottom of the devices. The two DCMs on the left and right of the chips are in the middle of the outer block RAM/DSP48A columns of the four or five columns in the selected device, as shown in the diagram.
2. A detailed diagram of the DSP48A can be found in UG431, *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide.*

Figure 1: **XA Spartan-3A DSP Family Architecture**

Configuration

XA Spartan-3A DSP FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board.

After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary-scan (JTAG), typically downloaded from a processor or system tester

Additionally, each XA Spartan-3A DSP FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The XA Spartan-3A DSP FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

XA Spartan-3A DSP FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

XA Spartan-3A DSP FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential I/O Pairs**

Device	CSG484		FGG676	
	User	Differential	User	Differential
XA3SD1800A	**309** *(60)*	**140** *(78)*	**519** *(110)*	**227** *(131)*
XA3SD3400A	**309** *(60)*	**140** *(78)*	**469** *(60)*	**213** *(117)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Production Status

Table 3 indicates the production status of each XA Spartan-3A DSP FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **XA Spartan-3A DSP FPGA Family Production Status (Production Speed File)**

Temperature Range		I-Grade	Q-Grade
Speed Grade		Standard (-4)	Standard (-4)
Part Number	XA3SD1800A	Production (v1.32)	Production (v1.32)
	XA3SD3400A	Production (v1.32)	–

Package Marking

Figure 2 shows the top marking for XA Spartan-3A DSP FPGAs in BGA packages.

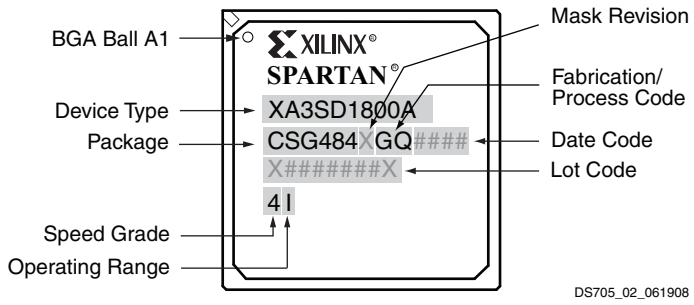


Figure 2: **XA Spartan-3A DSP FPGA Package Marking Example**

Ordering Information

XA Spartan-3A DSP FPGAs are available in Pb-free packaging only for all device/package combinations.

Pb-Free Packaging

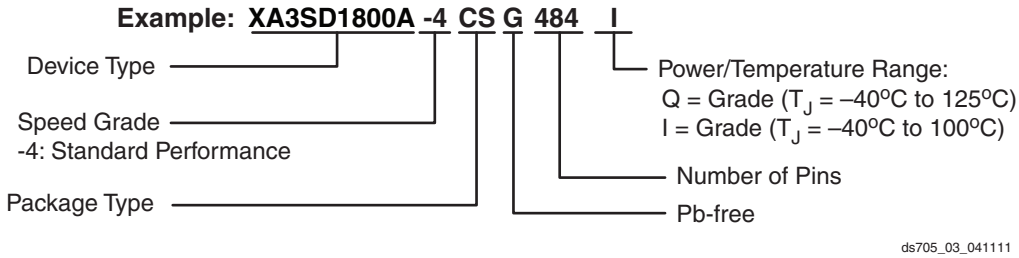


Figure 3: **Ordering Information**

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
XA3SD1800A	-4	Standard Performance	CSG484	484-ball Chip-Scale Ball Grid Array (CSBGA)	I	I-Grade (–40°C to 100°C)
XA3SD3400A			FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)	Q	Q-Grade (–40°C to 125°C)

Notes:

1. The XA Spartan-3A DSP FPGA product line is available in -4 speed grade only.
2. The XA3SD3400A is available in I-Grade only.

DC Electrical Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the published parameter values apply to all XA Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.

Absolute Maximum Ratings

Stresses beyond those listed under Table 4, *Absolute Maximum Ratings* might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Power Supply Specifications

Table 5: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.8	2.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: **Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

General Recommended Operating Conditions

Table 8: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	I-Grade		–40	–	100	°C
		Q-Grade		–40	–	125	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage(2)	V_{CCAUX} = 2.5		2.25	2.50	2.75	V
		V_{CCAUX} = 3.3		3.00	3.30	3.60	V
V_{IN} (3)	Input voltage	PCI™ IOSTANDARD		–0.5	–	V_{CCO}+0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_#(4)	–0.5	–	4.10	V
T_{IN}	Input signal transition time(5)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 11 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 13 lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*.
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

General DC Characteristics for I/O Pins

Table 9: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins** (1)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L (2)	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins, FPGA powered	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested		–10	–	+10	µA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		–10	–	+10	µA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add I_{HS} + I_{RPU}			µA
I_{RPU} (3)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = GND	V_{CCO} or V_{CCAUX} = 3.0V to 3.6V	–151	–315	–710	µA
			V_{CCO} or V_{CCAUX} = 2.3V to 2.7V	–82	–182	–437	µA
			V_{CCO} = 1.7V to 1.9V	–36	–88	–226	µA
			V_{CCO} = 1.4V to 1.6V	–22	–56	–148	µA
			V_{CCO} = 1.14V to 1.26V	–11	–31	–83	µA
R_{PU} (3)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 3)	V_{IN} = GND	V_{CCO} = 3.0V to 3.6V	5.1	11.4	23.9	kΩ
			V_{CCO} = 2.3V to 2.7V	6.2	14.8	33.1	kΩ
			V_{CCO} = 1.7V to 1.9V	8.4	21.6	52.6	kΩ
			V_{CCO} = 1.4V to 1.6V	10.8	28.4	74.0	kΩ
			V_{CCO} = 1.14V to 1.26V	15.3	41.1	119.4	kΩ
I_{RPD} (3)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = V_{CCO}	V_{CCAUX} = 3.0V to 3.6V	167	346	659	µA
			V_{CCAUX} = 2.25V to 2.75V	100	225	457	µA
R_{PD} (3)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 3)	V_{CCAUX} = 3.0V to 3.6V	V_{IN} = 3.0V to 3.6V	5.5	10.4	20.8	kΩ
			V_{IN} = 2.3V to 2.7V	4.1	7.8	15.7	kΩ
			V_{IN} = 1.7V to 1.9V	3.0	5.7	11.1	kΩ
			V_{IN} = 1.4V to 1.6V	2.7	5.1	9.6	kΩ
			V_{IN} = 1.14V to 1.26V	2.4	4.5	8.1	kΩ
		V_{CCAUX} = 2.25V to 2.75V	V_{IN} = 3.0V to 3.6V	7.9	16.0	35.0	kΩ
			V_{IN} = 2.3V to 2.7V	5.9	12.0	26.3	kΩ
			V_{IN} = 1.7V to 1.9V	4.2	8.5	18.6	kΩ
			V_{IN} = 1.4V to 1.6V	3.6	7.2	15.7	kΩ
			V_{IN} = 1.14V to 1.26V	3.0	6.0	12.5	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		–10	–	+10	µA
C_{IN}	Input capacitance	–		–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{CCO} = 3.3V ± 10%	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		V_{CCO} = 2.5V ± 10%	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO}/I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	I-Grade Maximum(2)	Q-Grade Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3SD1800A	41	500	900	mA
		XA3SD3400A	64	725	–	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3SD1800A	0.4	5	5	mA
		XA3SD3400A	0.4	5	–	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XA3SD1800A	25	110	145	mA
		XA3SD3400A	39	160	–	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A DSP FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480, *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Single-Ended I/O Standards

Table 11: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[2]			V_{REF}			V_{IL}	V_{IH}[3]
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33[4]	3.0	3.3	3.6				0.8	2.0
LVCMOS25[4,5]	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3[6]	3.0	3.3	3.6				$0.3 \bullet V_{CCO}$	$0.5 \bullet V_{CCO}$
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III	1.4	1.5	1.6	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL2_II	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs when V_{CCAUX} = 3.3V range and for PCI I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 4.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS25 or LVCMOS33 standard depending on V_{CCAUX}. The Dual-Purpose configuration pins use the LVCMOS25 standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins.

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL[3]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24[6]	–24		
LVCMOS33[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16[6]		
	24[4]	24	–24[6]		
LVCMOS25[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16[4]	16	–16[6]		
	24[4]	24[6]	–24[6]		
LVCMOS18[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6[6]		
	8	8	–8		
	12[4]	12	–12[6]		
	16[4]	16	–16		
LVCMOS15[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8[4]	8	–8		
	12[4]	12	–12		
LVCMOS12[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4[4]	4	–4		
	6[4]	6	–6		
PCI33_3[5]		1.5	–0.5	10% V_{CCO}	90% V_{CCO}

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
HSTL_I[4]	8	–8	0.4	V_{CCO} – 0.4
HSTL_III[4]	24[7]	–8	0.4	V_{CCO} – 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} – 0.4
HSTL_II_18[4]	16	–16[7]	0.4	V_{CCO} – 0.4
HSTL_III_18	24[7]	–8	0.4	V_{CCO} – 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II[4]	13.4	–13.4	V_{TT} – 0.475	V_{TT} + 0.475
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II[4]	16.2	–16.2	V_{TT} – 0.80	V_{TT} + 0.80
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 11.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} – the output current condition under which V_{OL} is tested
   I_{OH} – the output current condition under which V_{OH} is tested
   V_{OL} – the output voltage that indicates a Low logic level
   V_{OH} – the output voltage that indicates a High logic level
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{TT} – the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
4. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
5. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see http://www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics, but no PCI-X IP is supported.
6. Derate by 20% for T_J above 100ºC
7. Derate by 5% for T_J above 100ºC

Differential I/O Standards

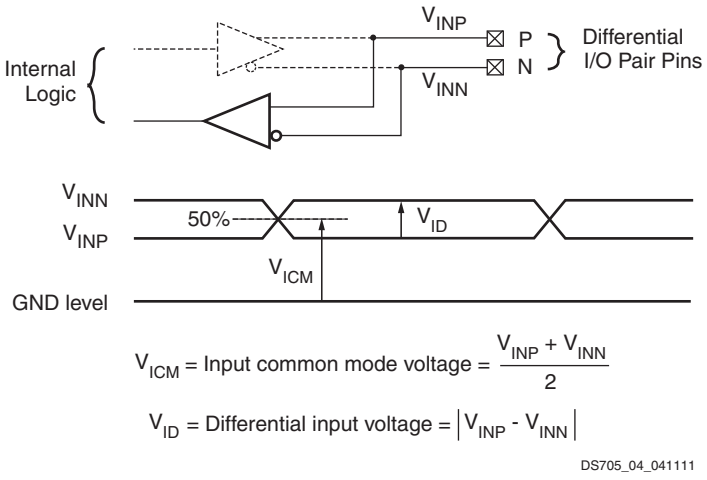


Figure 4: **Differential Input Voltages**

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25[3]	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33[3]	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25[4]	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25[3]	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33[3]	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25[5]	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33[5]	Inputs Only			100	800	1000	0.3	1.2	2.8[6]
RSDS_25[3]	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33[3]	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33[3,4,7]	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25[3]	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33[3]	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18[8]	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II[8]	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II[8]	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See External Termination Requirements for Differential I/O, page 16.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX} = 3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID}/2)$.
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \le V_{ICM} \le (V_{CCAUX} - 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in Table 11. Other differential standards do not use V_{REF}.

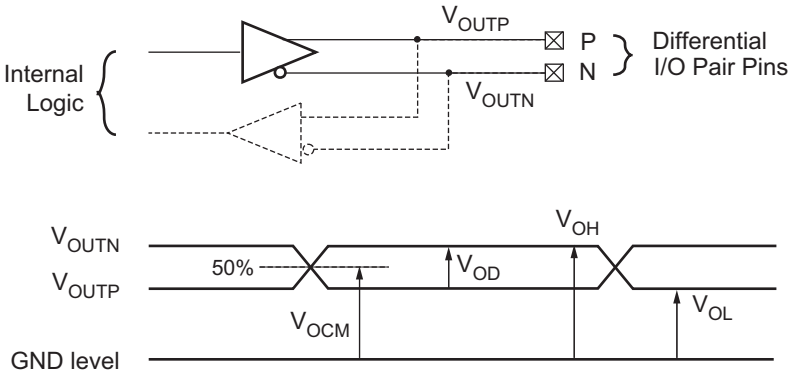


Figure 5: **Differential Output Voltages**

Table 14: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8

Notes:
1. The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
2. See External Termination Requirements for Differential I/O, page 16.
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V.

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

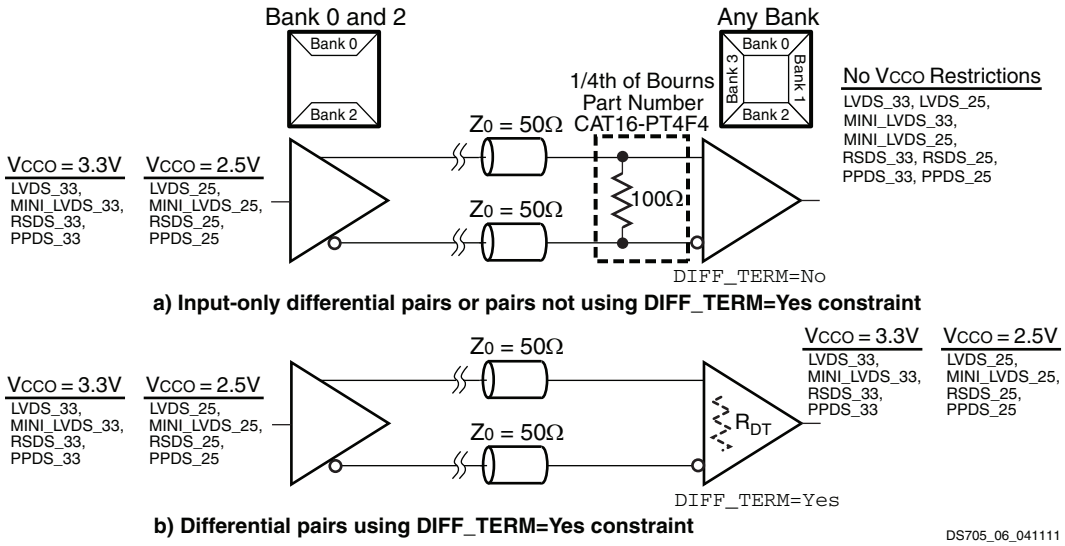


Figure 6: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

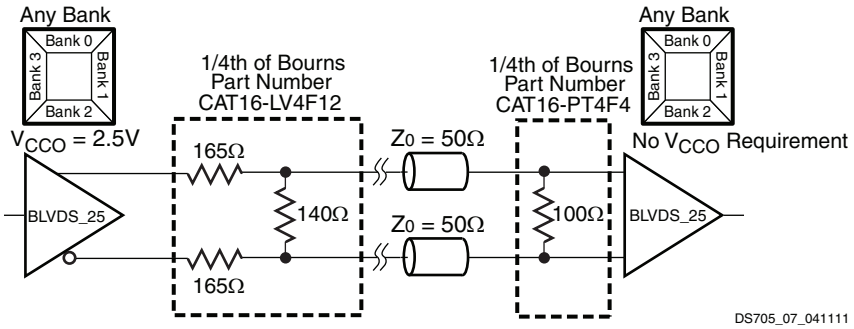


Figure 7: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

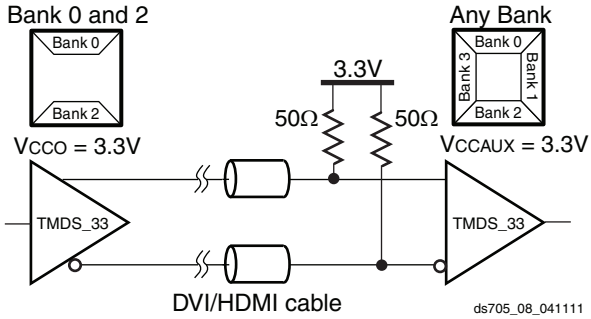


Figure 8: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Read Endurance

Table 15: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All XA Spartan-3A DSP FPGAs ship in the -4 speed grade. Switching characteristics in this document are designated as Production, as shown in Table 16.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the published parameter values apply to all XA Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The XA Spartan-3A DSP FPGA speed files (v1.32), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 16. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 16: **XA Spartan-3A DSP FPGA v1.32 Speed Grade Designations**

Device	Production
XA3SD1800A	-4
XA3SD3400A	-4

Table 17 provides the recent history of the XA Spartan-3A DSP FPGA speed files.

Table 17: **XA Spartan-3A DSP Speed File Version History**

Version	ISE Software Release	Description
1.32	ISE 10.1 SP2	Support for Automotive.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Max	
Clock-to-Output Times					
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	XA3SD1800A	3.51	ns
			XA3SD3400A	3.82	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	XA3SD1800A	5.58	ns
			XA3SD3400A	6.13	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 23. If the latter is true, *add* the appropriate Output adjustment from Table 26.
3. DCM output jitter is included in all measurements.

Pin-to-Pin Setup and Hold Times

Table 19: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Min	
Setup Times					
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XA3SD1800A	3.11	ns
			XA3SD3400A	2.49	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 6, without DCM	XA3SD1800A	3.39	ns
			XA3SD3400A	3.08	ns
Hold Times					
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XA3SD1800A	–0.38	ns
			XA3SD3400A	–0.26	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 6, without DCM	XA3SD1800A	–0.71	ns
			XA3SD3400A	–0.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 23. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 23. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 20: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4	Units
					Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2)	0	XA3SD1800A	1.81	ns
				XA3SD3400A	1.88	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XA3SD1800A	2.24	ns
			2		2.83	ns
			3		3.64	ns
			4		4.20	ns
			5		4.16	ns
			6		5.09	ns
			7		6.02	ns
			8		6.63	ns
			1	XA3SD3400A	2.44	ns
			2		3.02	ns
			3		3.81	ns
			4		4.39	ns
			5		4.26	ns
			6		5.08	ns
			7		5.95	ns
			8		6.55	ns

Table 20: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4 Min	Units
Hold Times						
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3)	0	XA3SD1800A	–0.52	ns
				XA3SD3400A	–0.56	ns
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XA3SD1800A	–1.40	ns
			2		–2.11	ns
			3		–2.48	ns
			4		–2.77	ns
			5		–2.62	ns
			6		–3.06	ns
			7		–3.42	ns
			8		–3.65	ns
			1	XA3SD3400A	–1.31	ns
			2		–1.88	ns
			3		–2.44	ns
			4		–2.89	ns
			5		–2.83	ns
			6		–3.33	ns
			7		–3.63	ns
			8		–3.96	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	–	–	All	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 23.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 23. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 21: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Input Propagation Times

Table 22: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4	Units
					Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2)	0	XA3SD1800A	2.04	ns
				XA3SD3400A	2.11	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	1	XA3SD1800A	2.47	ns
			2		3.06	ns
			3		3.86	ns
			4		4.43	ns
			5		4.39	ns
			6		5.32	ns
			7		6.24	ns
			8		6.86	ns
			1	XA3SD3400A	2.67	ns
			2		3.25	ns
			3		4.04	ns
			4		4.62	ns
			5		4.49	ns
			6		5.31	ns
			7		6.18	ns
			8		6.78	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 23.

Input Timing Adjustments

Table 23: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	Speed Grade: -4	
Single-Ended Standards		
LVTTL	0.62	ns
LVCMOS33	0.54	ns
LVCMOS25	0.00	ns
LVCMOS18	0.83	ns
LVCMOS15	0.60	ns
LVCMOS12	0.31	ns
PCI33_3	0.45	ns

Table 23: **Input Timing Adjustments by IOSTANDARD *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	Speed Grade: -4	
HSTL_I	0.72	ns
HSTL_III	0.85	ns
HSTL_I_18	0.69	ns
HSTL_II_18	0.83	ns
HSTL_III_18	0.79	ns
SSTL18_I	0.71	ns
SSTL18_II	0.71	ns
SSTL2_I	0.71	ns
SSTL2_II	0.71	ns
SSTL3_I	0.78	ns
SSTL3_II	0.78	ns
Differential Standards		
LVDS_25	0.79	ns
LVDS_33	0.79	ns
BLVDS_25	0.79	ns
MINI_LVDS_25	0.84	ns
MINI_LVDS_33	0.84	ns
LVPECL_25	0.80	ns
LVPECL_33	0.80	ns
RSDS_25	0.83	ns
RSDS_33	0.83	ns
TMDS_33	0.80	ns
PPDS_25	0.81	ns
PPDS_33	0.81	ns
DIFF_HSTL_I_18	0.80	ns
DIFF_HSTL_II_18	0.98	ns
DIFF_HSTL_III_18	1.05	ns
DIFF_HSTL_I	0.77	ns
DIFF_HSTL_III	1.05	ns
DIFF_SSTL18_I	0.76	ns
DIFF_SSTL18_II	0.76	ns
DIFF_SSTL2_I	0.77	ns
DIFF_SSTL2_II	0.77	ns
DIFF_SSTL3_I	1.06	ns
DIFF_SSTL3_II	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Output Propagation Times

Table 24: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Max	
Clock-to-Output Times					
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	All	3.13	ns
Propagation Times					
T_{IOOP}	The time it takes for data to travel from the JOB's O input to the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	All	2.91	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		All	2.85	ns
Set/Reset Times					
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	All	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin		All	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Three-State Output Propagation Times

Table 25: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Max	
Synchronous Output Enable/Disable Times					
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.39	ns
T_{IOCKON}[2]	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.35	ns
Asynchronous Output Enable/Disable Times					
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	10.36	ns
Set/Reset Times					
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.86	ns
T_{IOSRON}[2]	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 26.

Output Timing Adjustments

Table 26: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
Single-Ended Standards				
LVTTL	Slow	2 mA	5.58	ns
		4 mA	3.44	ns
		6 mA	3.44	ns
		8 mA	2.26	ns
		12 mA	1.66	ns
		16 mA	1.29	ns
		24 mA	2.97	ns
	Fast	2 mA	3.37	ns
		4 mA	2.26	ns
		6 mA	2.26	ns
		8 mA	0.62	ns
		12 mA	0.61	ns
		16 mA	0.59	ns
		24 mA	0.60	ns
	QuietIO	2 mA	27.67	ns
		4 mA	27.67	ns
		6 mA	27.67	ns
		8 mA	16.71	ns
		12 mA	16.67	ns
		16 mA	16.22	ns
		24 mA	12.11	ns

Table 26: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
LVCMOS33	Slow	2 mA	5.58	ns
		4 mA	3.30	ns
		6 mA	3.30	ns
		8 mA	2.26	ns
		12 mA	1.29	ns
		16 mA	1.21	ns
		24 mA	2.79	ns
	Fast	2 mA	3.72	ns
		4 mA	2.04	ns
		6 mA	2.08	ns
		8 mA	0.53	ns
		12 mA	0.59	ns
		16 mA	0.59	ns
		24 mA	0.51	ns
	QuietIO	2 mA	27.67	ns
		4 mA	27.67	ns
		6 mA	27.67	ns
		8 mA	16.71	ns
		12 mA	16.29	ns
		16 mA	16.18	ns
		24 mA	12.11	ns