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XB1014-QT

Buffer Amplifier
37.0 - 40.0 GHz

Rev. V3

Features

- 21.0 dB Small Signal Gain
- +22.0 dBm Psat
- +20.0 dBm P1dB
- +30.5 dBm Output IP3
- Variable Gain with Adjustable Bias
- Lead-free 3 mm 16-lead PQFN Package
- 100% RF, DC and Output Power Testing
- RoHS* Compliant and 260°C Reflow Compatible

Description

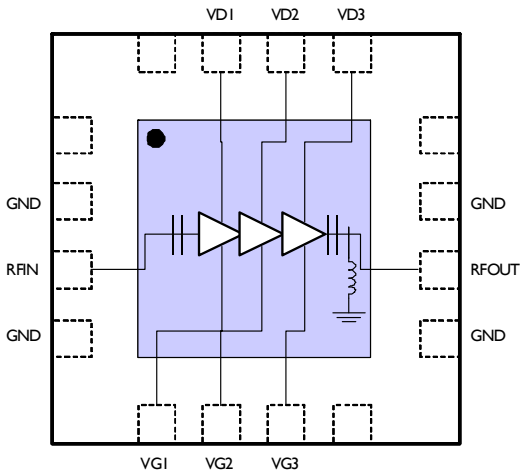
The XB1014-QT is a three stage 37.0-40.0 GHz GaAs MMIC buffer amplifier that has a small signal gain of 21.0 dB and 20.0 dBm P1dB output compression point. The device also provides variable gain regulation with adjustable bias. The device is ideally suited as an LO or RF buffer stage with broadband performance at a very low cost.

The device comes in an RoHS compliant 3x3mm QFN surface mount package offering excellent RF and thermal properties. This device has been designed for use in 38 GHz Point-to-Point Microwave Radio applications.

Ordering Information

Part Number	Package
XB1014-QT-0G00	bulk quantity
XB1014-QT-0G0T	tape and reel
XB1014-QT-EV1	evaluation board

Functional Schematic



Pin Configuration[1]

Pin No.	Function	Pin No.	Function
3	RF Input	10	RF Output
5	Gate 1 Bias	13	Drain 3 Bias
6	Gate 2 Bias	14	Drain 2 Bias
7	Gate 3 Bias	15	Drain 1 Bias

1. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Buffer Amplifier
37.0 - 40.0 GHz

Rev. V3

Electrical Specifications: 37-40.15 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	-	7.0	40.0
Output Return Loss (S22)	dB	-	10.0	-
Small Signal Gain (S21)	dB	17.0	21.0	-
Reverse isolation (S12)	dB	-	40.0	24.5
Output Power for 1dB Compression Point (P1dB)	dBm	-	20.0	-
Saturated Output Power (Psat)	dBm	19.5	22.0	-
Output IP3 (Psci = 4 dBm)	dBm	27.0	30.5	-
Drain Bias Voltage (Vd1,2,3)	V	-	4.0	4.0
Gate Bias Voltage (Vg1,2,3)	V	-1.0	-0.3	-0.1
Supply Current (Id1,2,3)	mA	-	250	300

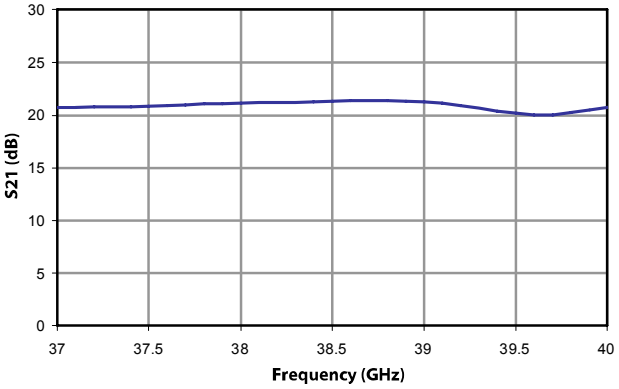
Absolute Maximum Ratings [2,3]

Parameter	Absolute Max.
Supply Voltage (Vd1,2,3)	+4.3 V
Supply Voltage (Vg1,2,3)	-1.5V < Vg < 0V
Input Power (Pin)	+20 dBm
Abs. Max Junction/Channel Temp	MTTF Graph
Max. Operating Junction/Channel Temp	150°C
Continuous Power Dissipation (Pdiss) at 85°C	1.2 W
Thermal Resistance	47°C/W
Operating Temperature (Ta)	-55°C to MTTF Graph
Storage Temperature (Tstg)	-65°C to +165°C
Mounting Temperature	See solder reflow profile
ESD Min. - Machine Model (MM)	Class A
ESD Min. - Human Body Model (HBM)	Class 1A
MSL Level	MSL1

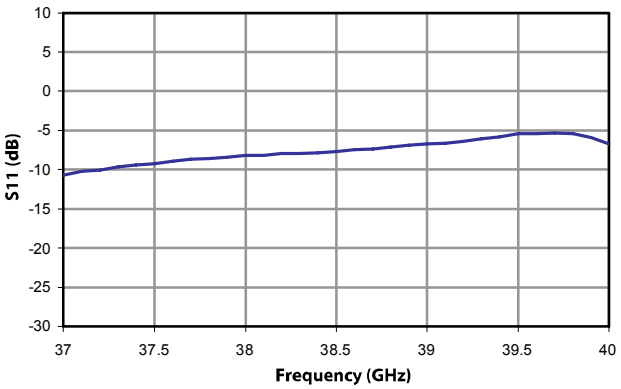
2. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
3. For saturated performance it is recommended that the sum of (2*Vdd + abs (Vgg)) <9V

Typical Performance Curves

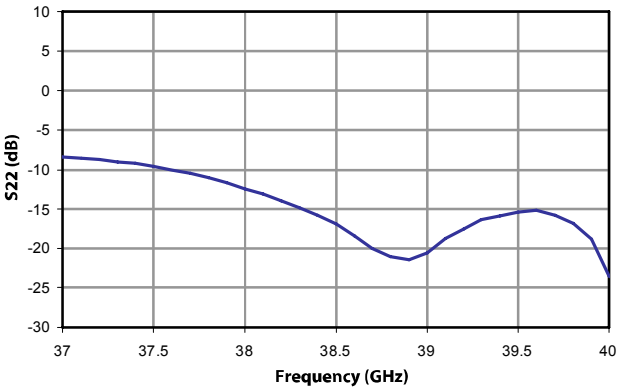
XB1014-QT: Small Signal Gain (S21)
Vd = 4V, Id1 = Id2 = 62.5 mA, Id3 = 125 mA



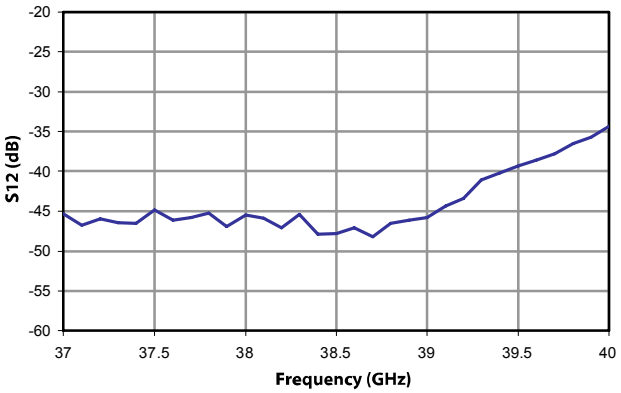
XB1014-QT: Input Return Loss (S11)
Vd = 4V, Id1 = Id2 = 62.5 mA, Id3 = 125 mA



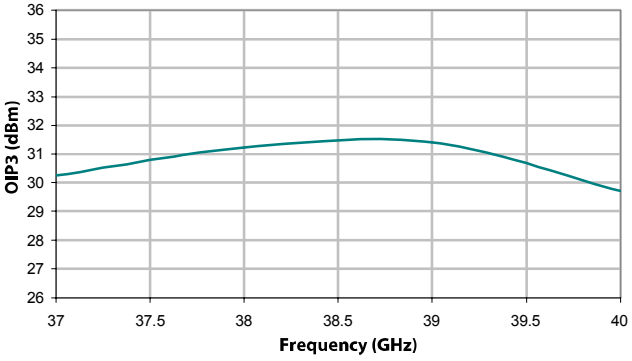
XB1014-QT: Output Return Loss (S22)
Vd = 4V, Id1 = Id2 = 62.5 mA, Id3 = 125 mA



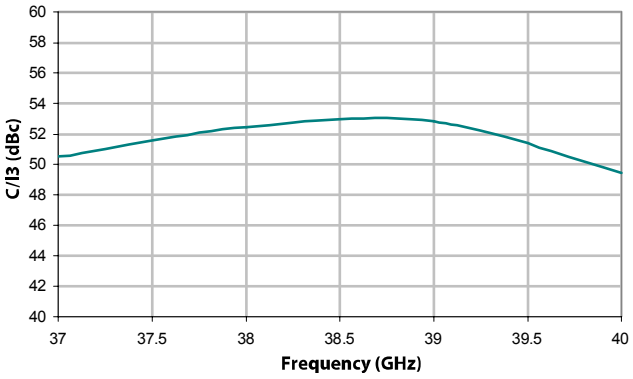
XB1014-QT: Reverse Isolation (S12)
Vd = 4V, Id1 = Id2 = 62.5 mA, Id3 = 125 mA



XB1014-QT: OIP3 vs Freq
Pscl=+5dBm; Vd1,2,3=4.0V, Id1=Id2=62.5mA, Id3=125mA

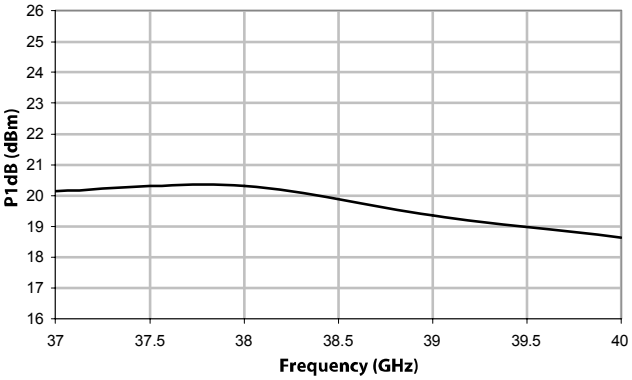


XB1014-QT: C/I3 vs Freq
Pscl=+5dBm; Vd1,2,3=4.0V, Id1=Id2=62.5mA, Id3=125mA

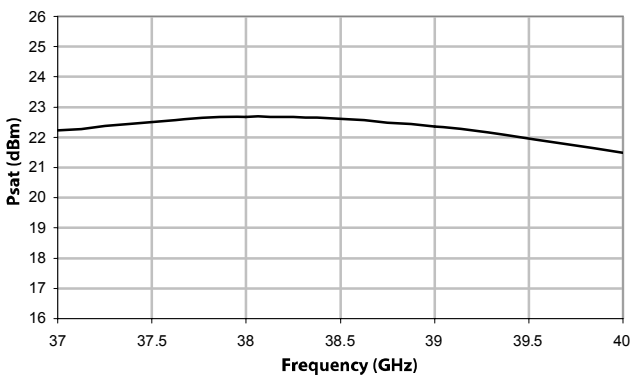


Typical Performance Curves (cont.)

XB1014-QT: P1dB vs Freq
Vd1,2,3=4.0V, Id1=Id2=62.5mA, Id3=125mA

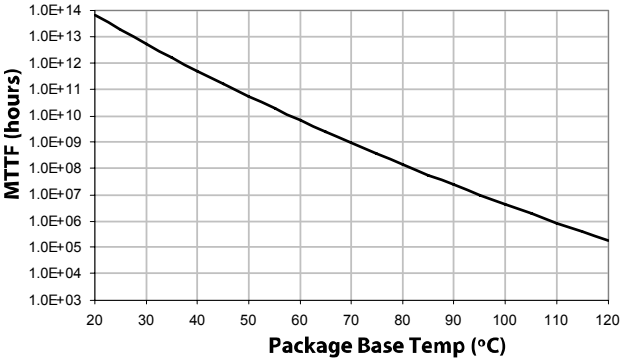


XB1014-QT: Psat vs Freq
Vd1,2,3=4.0V, Id1=Id2=62.5mA, Id3=125mA

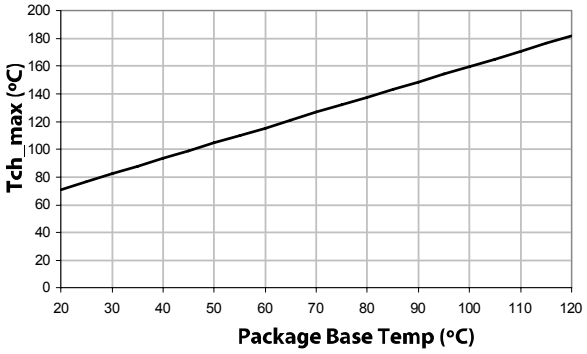


MTTF

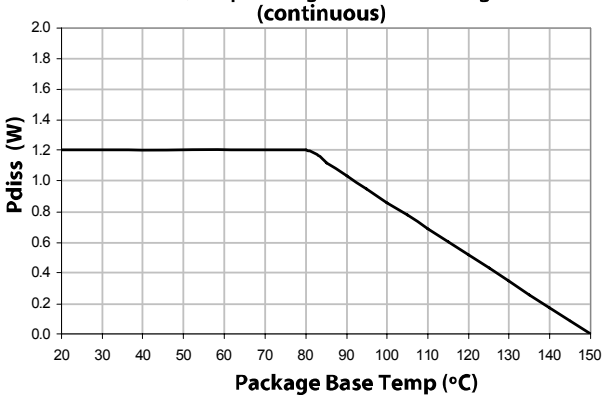
XB1014-QT: MTTF hours vs. Package Base Temperature
Vd1,2,3=4V; Id1=Id2=62.5mA, Id3=125mA



XB1014-QT: Tch (max) vs. Package Base Temperature
Vd1,2,3=4V; Id1=Id2=62.5mA, Id3=125mA



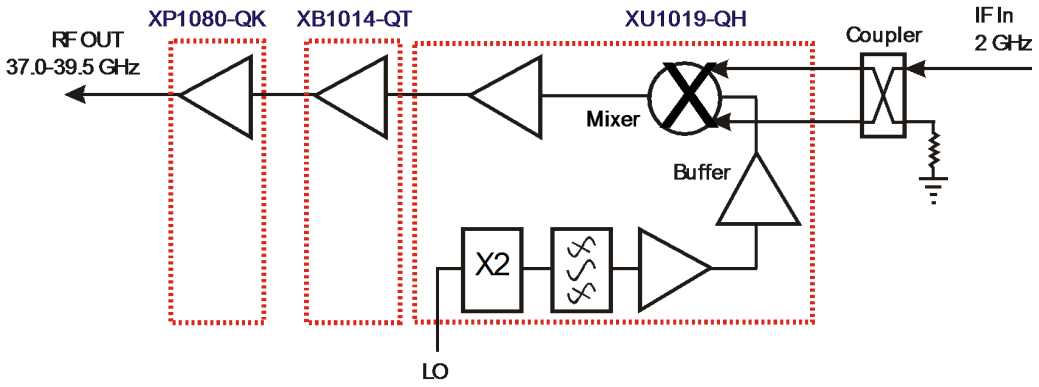
XB1014-QT: Operating Power De-rating Curve
(continuous)



App Note [1] Biasing - It is recommended to bias the amplifier with Vd=4.0 V and IdTOTAL=250 mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.3 V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

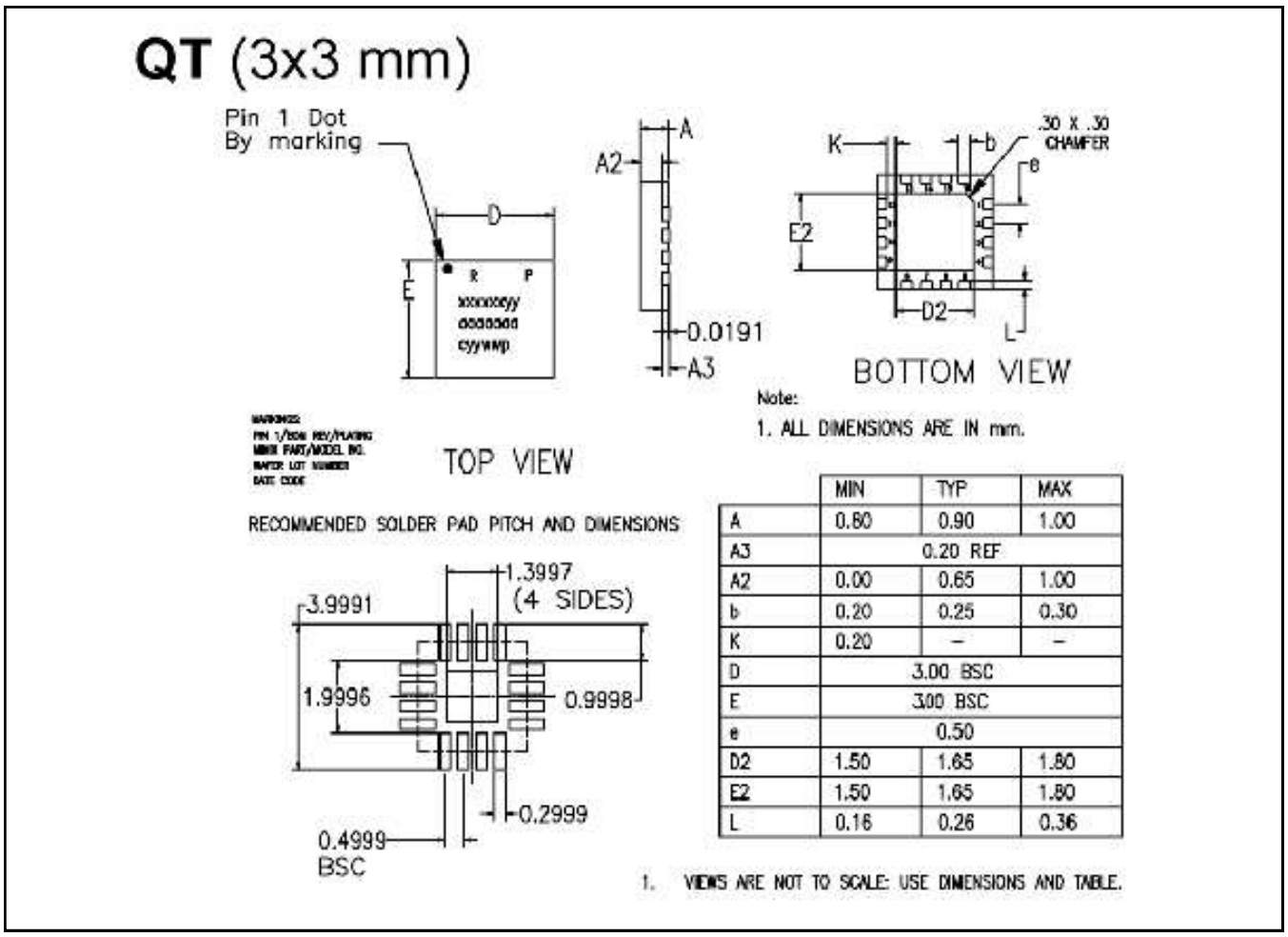
App Note [2] Bias Arrangement - Each DC pin (Vd and Vg) needs to have DC bypass capacitance (100pF/10nF/1uF) as close to the package as possible.

Typical Application



MMIC-based 37.0-40.0 GHz Transmitter Block Diagram

Lead-Free 3 mm 16-Lead PQFN†



	MIN	TYP	MAX
A	0.80	0.90	1.00
A3		0.20 REF	
A2	0.00	0.65	1.00
b	0.20	0.25	0.30
K	0.20	–	–
D		3.00 BSC	
E		3.00 BSC	
e		0.50	
D2	1.50	1.65	1.80
E2	1.50	1.65	1.80
L	0.16	0.26	0.36

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.