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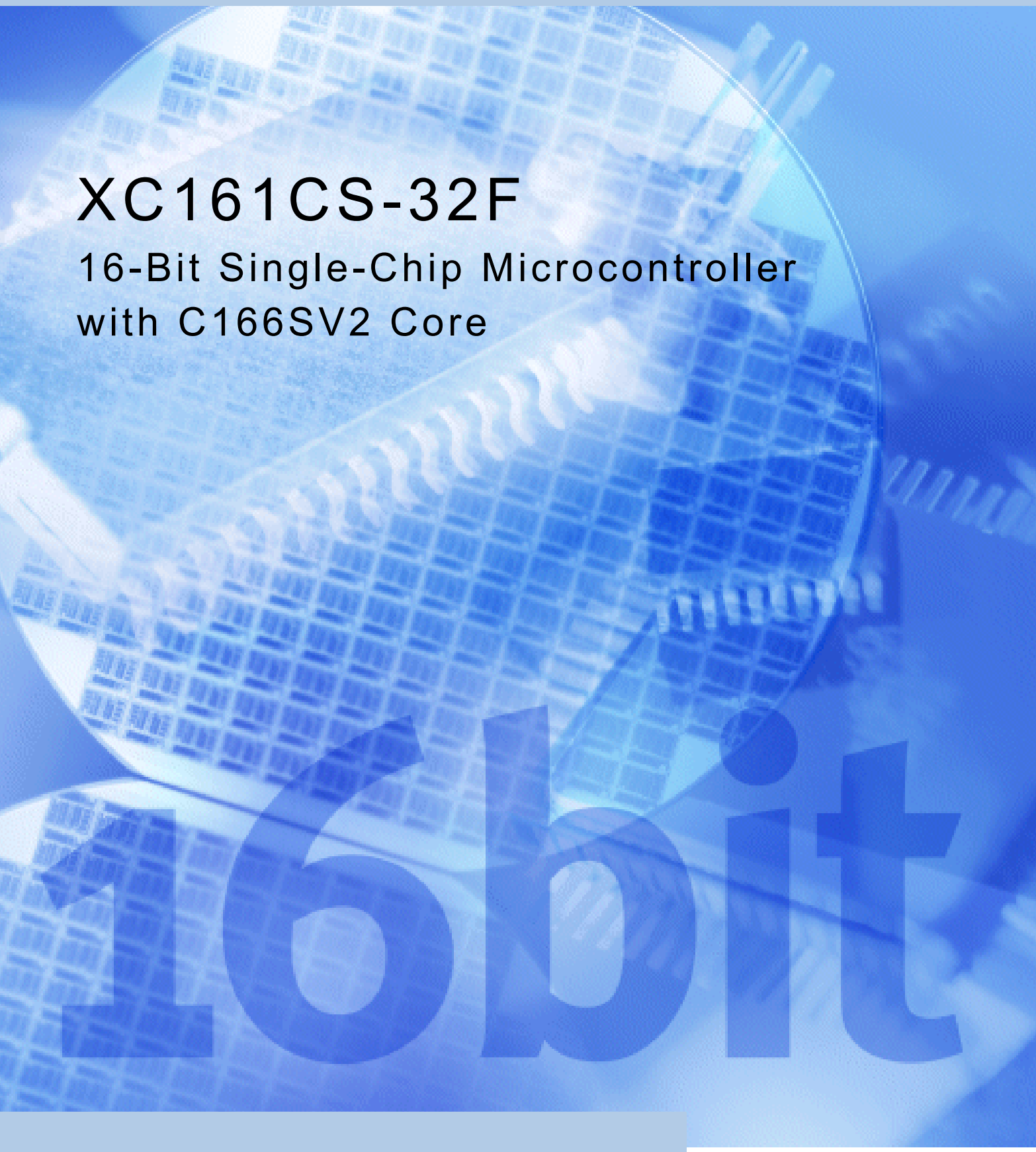
Data Sheet, V1.2, Aug. 2006

XC161CS-32F

16-Bit Single-Chip Microcontroller with C166SV2 Core



Microcontrollers

Never stop thinking

Edition 2006-08

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XC161CS-32F

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers

Never stop thinking

XC161
Revision History: V1.2, 2006-08

Previous Version(s):
V1.1, 2005-06
V1.0, 2004-11

Page	Subjects (major changes since last revision)
12	Description of the $\overline{\text{TRST}}$ signal modified.
17	Footnote added about pins XTAL1/XTAL3 belonging to V_{DDI} power domain.
21	Emulation Program SRAM (EPSRAM) introduced in the memory map.
50	Instructions Set Summary improved.
57	Footnote added about amplitude at XTAL1 pin.
82	Green package added.
82	Thermal Resistance: R_{THA} replaced by $R_{\Theta JC}$ and $R_{\Theta JL}$ because R_{THA} strongly depends on the external system (PCB, environment). P_{DISS} removed, because no static parameter, but derived from thermal resistance.

We Listen to Your Comments
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mcdocu.comments@infineon.com

Table of Contents

1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 × 16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with 73 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 4 Kbytes On-Chip Data SRAM (DSRAM)
  - 6 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 256 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 12-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55 µs or 2.15 µs)
  - Two 16-Channel General Purpose Capture/Compare Units (32 Input/Output Pins)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip TwinCAN Interface (Rev. 2.0B active) with 32 Message Objects (Full CAN/Basic CAN) on Two CAN Nodes, and Gateway Functionality
  - IIC Bus Interface (10-bit addressing, 400 kbit/s) with 3 Channels (multiplexed)
  - On-Chip Real Time Clock, Driven by Dedicated Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog

- Up to 12 Mbytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses
  - Selectable Address Bus Width
  - 16-Bit or 8-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Up to 99 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Debug Support via JTAG Interface
- 144-Pin Green TQFP Package, 0.5 mm (19.7 mil) pitch (RoHS compliant)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC161 please refer to your responsible sales representative or your local distributor.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

This document describes several derivatives of the XC161 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC161** throughout this document.

Table 1 XC161 Derivative Synopsis

Derivative[1]	Temp. Range	Program Memory	On-Chip RAM	Interfaces
Standard Devices[2]				
SAK-XC161CS-32F40F SAK-XC161CS-32F20F	-40 °C to 125 °C	256 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 6 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1, IIC
SAF-XC161CS-32F40F SAF-XC161CS-32F20F	-40 °C to 85 °C			
Grade A Devices[2]				
SAK-XC161CS-32F40F SAK-XC161CS-32F20F	-40 °C to 125 °C	256 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 6 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1, IIC
SAF-XC161CS-32F40F SAF-XC161CS-32F20F	-40 °C to 85 °C			

1) This Data Sheet is valid for devices starting with and including design step BB.

2) The Flash speed grading indicates the access time to the on-chip Flash module. According to this access time Flash waitstates must be selected (bitfield WSFLASH in register IMBCTRL) according to the intended operating frequency. For more details, please refer to **Section 4.4.2**.
Grade A devices are identified by “Grade A” in the fourth line of the chip marking.

2 General Device Information

2.1 Introduction

The XC161 derivatives are high-performance members of the Infineon XC166 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 40 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program Flash, program RAM, and data RAM.

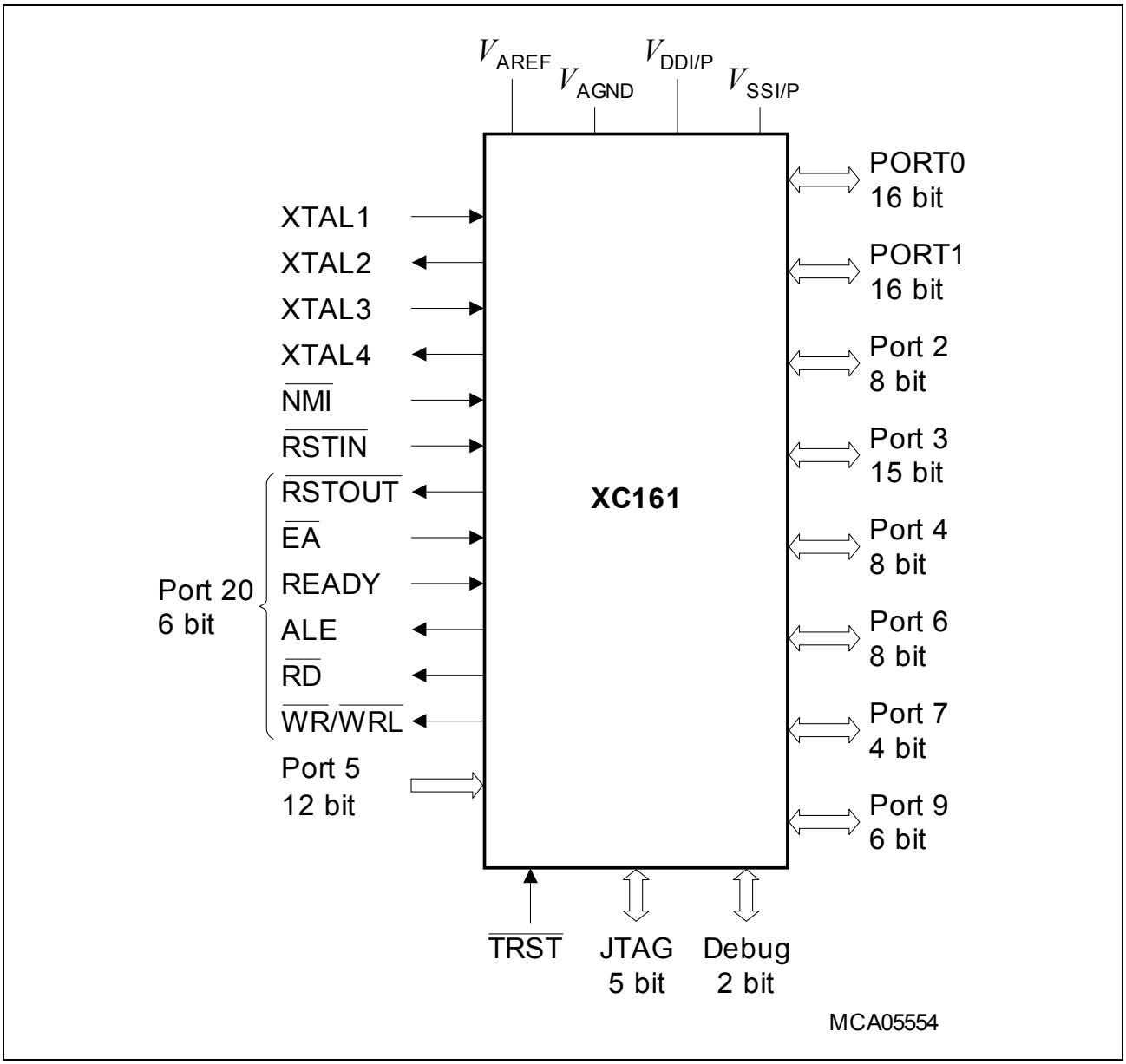

Figure 1 Logic Symbol

2.2 Pin Configuration and Definition

The pins of the XC161 are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN interface lines assigned to them.

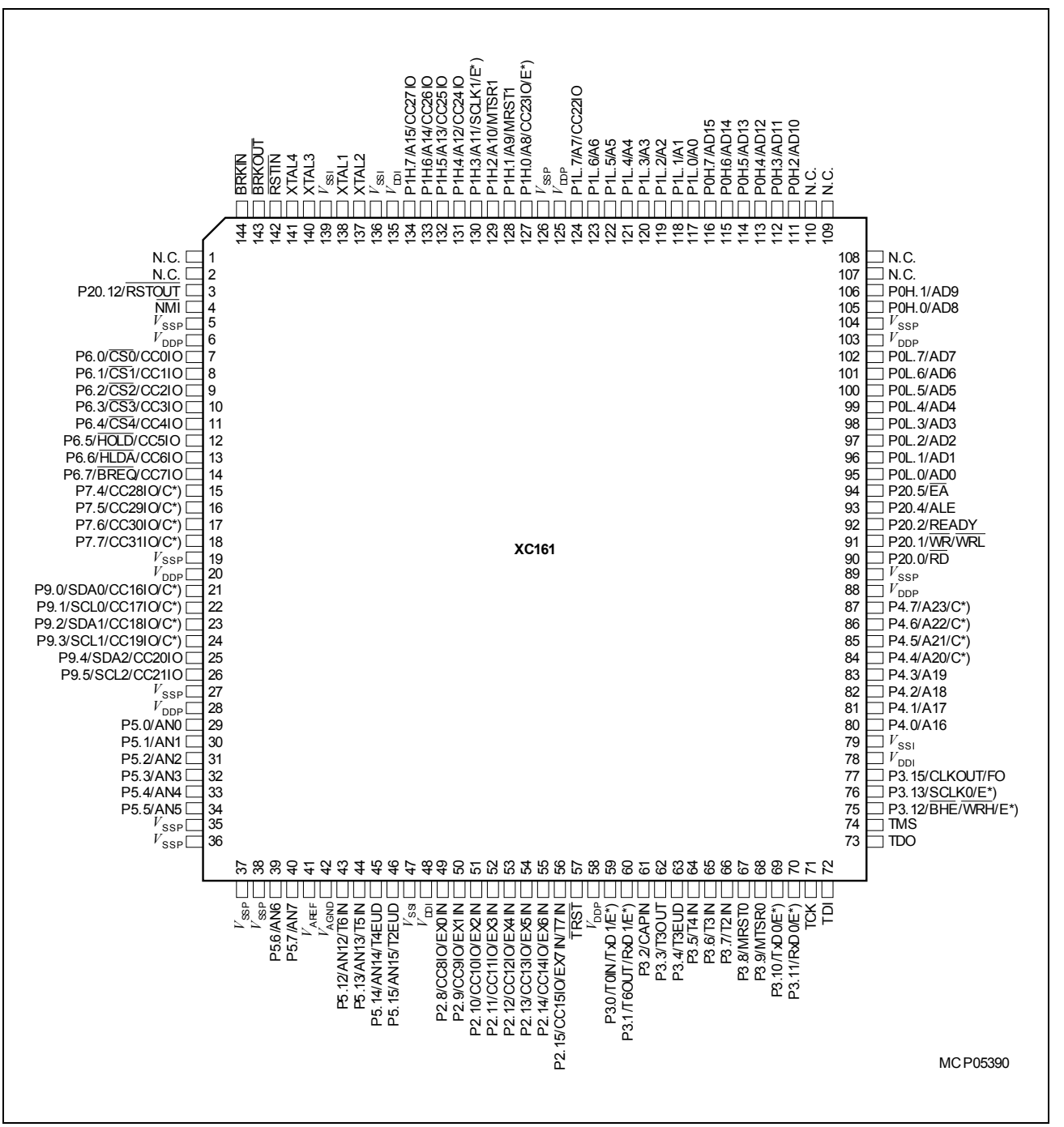

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions

Sym-bol	Pin Num.	Input Outp.	Function
P20.12	3	IO	For details, please refer to the description of **P20**.
NMI	4	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the XC161 into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 6 is selectable (standard or special). The Port 6 pins also serve for alternate functions:
P6.0	7	O	CS0 Chip Select 0 Output,
		I/O	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P6.1	8	O	CS1 Chip Select 1 Output,
		I/O	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P6.2	9	O	CS2 Chip Select 2 Output,
		I/O	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P6.3	10	O	CS3 Chip Select 3 Output,
		I/O	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P6.4	11	O	CS4 Chip Select 4 Output,
		I/O	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P6.5	12	I	HOLD External Master Hold Request Input,
		I/O	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P6.6	13	O/I	HLDA Hold Acknowledge Output (master mode) or Input (slave mode),
		I/O	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P6.7	14	O	BREQ Bus Request Output,
		I/O	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is a 4-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 7 is selectable (standard or special). Port 7 pins provide inputs/outputs for CAPCOM2 and serial interface lines.[1)]
P7.4	15	I/O I I	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp., CAN2_RxD CAN Node 2 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin B)
P7.5	16	I/O O I	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp., CAN2_TxD CAN Node 2 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin B)
P7.6	17	I/O I I	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp., CAN1_RxD CAN Node 1 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin A)
P7.7	18	I/O O I	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp., CAN1_TxD CAN Node 1 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function		
P9		IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:[1)]		
P9.0	21	I/O I I/O	CC16IO CAN2_RxD SDA0	CAPCOM2: CC16 Capture Inp./Compare Outp., CAN Node 2 Receive Data Input, IIC Bus Data Line 0	
P9.1	22	I/O O I/O	CC17IO CAN2_TxD SCL0	CAPCOM2: CC17 Capture Inp./Compare Outp., CAN Node 2 Transmit Data Output, IIC Bus Clock Line 0	
P9.2	23	I/O I I/O	CC18IO CAN1_RxD SDA1	CAPCOM2: CC18 Capture Inp./Compare Outp., CAN Node 1 Receive Data Input, IIC Bus Data Line 1	
P9.3	24	I/O O I/O	CC19IO CAN1_TxD SCL1	CAPCOM2: CC19 Capture Inp./Compare Outp., CAN Node 1 Transmit Data Output, IIC Bus Clock Line 1	
P9.4	25	I/O I/O	CC20IO SDA2	CAPCOM2: CC20 Capture Inp./Compare Outp., IIC Bus Data Line 2	
P9.5	26	I/O I/O	CC21IO SCL2	CAPCOM2: CC21 Capture Inp./Compare Outp., IIC Bus Clock Line 2	
P5		I	Port 5 is a 12-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:		
P5.0	29	I	AN0		
P5.1	30	I	AN1		
P5.2	31	I	AN2		
P5.3	32	I	AN3		
P5.4	33	I	AN4		
P5.5	34	I	AN5		
P5.6	39	I	AN6		
P5.7	40	I	AN7		
P5.12	43	I	AN12,	T6IN	GPT2 Timer T6 Count/Gate Input
P5.13	44	I	AN13,	T5IN	GPT2 Timer T5 Count/Gate Input
P5.14	45	I	AN14,	T4EUD	GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	46	I	AN15,	T2EUD	GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P2		IO	Port 2 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 2 is selectable (standard or special). The following Port 2 pins also serve for alternate functions:
P2.8	49	I/O I	CC8IO CAPCOM1: CC8 Capture Inp./Compare Output, EX0IN Fast External Interrupt 0 Input (default pin)
P2.9	50	I/O I	CC9IO CAPCOM1: CC9 Capture Inp./Compare Output, EX1IN Fast External Interrupt 1 Input (default pin)
P2.10	51	I/O I	CC10IO CAPCOM1: CC10 Capture Inp./Compare Outp., EX2IN Fast External Interrupt 2 Input (default pin)
P2.11	52	I/O I	CC11IO CAPCOM1: CC11 Capture Inp./Compare Outp., EX3IN Fast External Interrupt 3 Input (default pin)
P2.12	53	I/O I	CC12IO CAPCOM1: CC12 Capture Inp./Compare Outp., EX4IN Fast External Interrupt 4 Input (default pin)
P2.13	54	I/O I	CC13IO CAPCOM1: CC13 Capture Inp./Compare Outp., EX5IN Fast External Interrupt 5 Input (default pin)
P2.14	55	I/O I	CC14IO CAPCOM1: CC14 Capture Inp./Compare Outp., EX6IN Fast External Interrupt 6 Input (default pin)
P2.15	56	I/O I I	CC15IO CAPCOM1: CC15 Capture Inp./Compare Outp., EX7IN Fast External Interrupt 7 Input (default pin), T7IN CAPCOM2: Timer T7 Count Input
$\overline{\text{TRST}}$	57	I	$\overline{\text{T}}$est-System Reset Input. For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{RSTIN}}$ activates the XC164CM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.0	59	I	T0IN	CAPCOM1 Timer T0 Count Input,
		O	TxD1	ASC1 Clock/Data Output (Async./Sync),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin B)
P3.1	60	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A)
P3.2	61	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	62	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	63	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	64	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	65	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	66	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	67	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	68	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	69	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	70	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin A)
P3.12	75	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	76	I/O	SCLK0	SSC0 Master Clock Output/Slave Clock Input.,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	77	O	CLKOUT	Master Clock Output,
		O	FOUT	Programmable Frequency Output
TCK	71	I	Debug System: JTAG Clock Input	
TDI	72	I	Debug System: JTAG Data In	
TDO	73	O	Debug System: JTAG Data Out	
TMS	74	I	Debug System: JTAG Test Mode Selection	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P4		IO	Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special). Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:[1)]	
P4.0	80	O	A16	Least Significant Segment Address Line
P4.1	81	O	A17	Segment Address Line
P4.2	82	O	A18	Segment Address Line
P4.3	83	O	A19	Segment Address Line
P4.4	84	O	A20	Segment Address Line,
		I	CAN2_RxD	CAN Node 2 Receive Data Input,
		I	EX5IN	Fast External Interrupt 5 Input (alternate pin B)
P4.5	85	O	A21	Segment Address Line,
		I	CAN1_RxD	CAN Node 1 Receive Data Input,
		I	EX4IN	Fast External Interrupt 4 Input (alternate pin B)
P4.6	86	O	A22	Segment Address Line,
		O	CAN1_TxD	CAN Node 1 Transmit Data Output,
		I	EX5IN	Fast External Interrupt 5 Input (alternate pin A)
P4.7	87	O	A23	Most Significant Segment Address Line,
		I	CAN1_RxD	CAN Node 1 Receive Data Input,
		O	CAN2_TxD	CAN Node 2 Transmit Data Output,
		I	EX4IN	Fast External Interrupt 4 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P20		IO	Port 20 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special). The following Port 20 pins also serve for alternate functions:	
P20.0	90	O	$\overline{RD}$	External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	91	O	$\overline{WR}$/$\overline{WRL}$	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus.
P20.2	92	I	READY	READY Input. When the READY function is enabled, memory cycle time waitstates can be forced via this pin during an external access.
P20.4	93	O	ALE	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	94	I	$\overline{EA}$	External Access Enable pin. **A low-level** at this pin during and after Reset forces the XC161 to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high-level** forces the XC161 to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.12	3	O	$\overline{RSTOUT}$	Internal Reset Indication Output. **Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset. **Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software.
			Note: Port 20 pins may input configuration values (see $\overline{EA}$).	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
PORT0		IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. Each pin can be programmed for input (output driver in high-impedance state) or output. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0 *Note: At the end of an external reset ($\overline{EA}$ = 0) PORT0 also may input configuration values.*
P0L.0 - P0L.7, P0H.0, P0H.1, P0H.2 - P0H.7	95 - 102, 105, 106, 111 - 116		
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions:
P1L.0 - P1L.6	117 - 123	O	(A0-6) Address output only
P1L.7	124	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P1H.0	127	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.,
		I	EX0IN Fast External Interrupt 0 Input (alternate pin B)
P1H.1	128	I/O	MRST1 SSC1 Master-Receive/Slave-Transmit In/Outp.
P1H.2	129	I/O	MTSR1 SSC1 Master-Transmit/Slave-Receive Out/Inp.
P1H.3	130	I/O	SCLK1 SSC1 Master Clock Output/Slave Clock Input,
		I	EX0IN Fast External Interrupt 0 Input (alternate pin A)
P1H.4	131	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	132	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	133	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	134	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	137 138	O I	XTAL2: Output of the main oscillator amplifier circuit XTAL1: Input to the main oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
XTAL3 XTAL4	140 141	I O	XTAL3: Input to the auxiliary (32-kHz) oscillator amplifier XTAL4: Output of the auxiliary (32-kHz) oscillator amplifier circuit To clock the device from an external source, drive XTAL3, while leaving XTAL4 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL3 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
$\overline{\text{RSTIN}}$	142	I	Reset Input with Schmitt-Trigger characteristics. A low-level at this pin while the oscillator is running resets the XC161. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle.* *External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
$\overline{\text{BRK OUT}}$	143	O	Debug System: Break Out
$\overline{\text{BRKIN}}$	144	I	Debug System: Break In
NC	1, 2, 107 - 110	–	No connection. It is recommended not to connect these pins to the PCB.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
V_{AREF}	41	–	Reference voltage for the A/D converter.
V_{AGND}	42	–	Reference ground for the A/D converter.
V_{DDI}	48, 78, 135	–	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{DDP}	6, 20, 28, 58, 88, 103, 125	–	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{SSI}	47, 79, 136, 139	–	**Digital Ground** Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.
V_{SSP}	5, 19, 27, 35, 36, 37, 38, 89, 104, 126	–	

1) The CAN interface lines are assigned to ports P4, P7, and P9 under software control.

3 Functional Description

The architecture of the XC161 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC161.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC161.

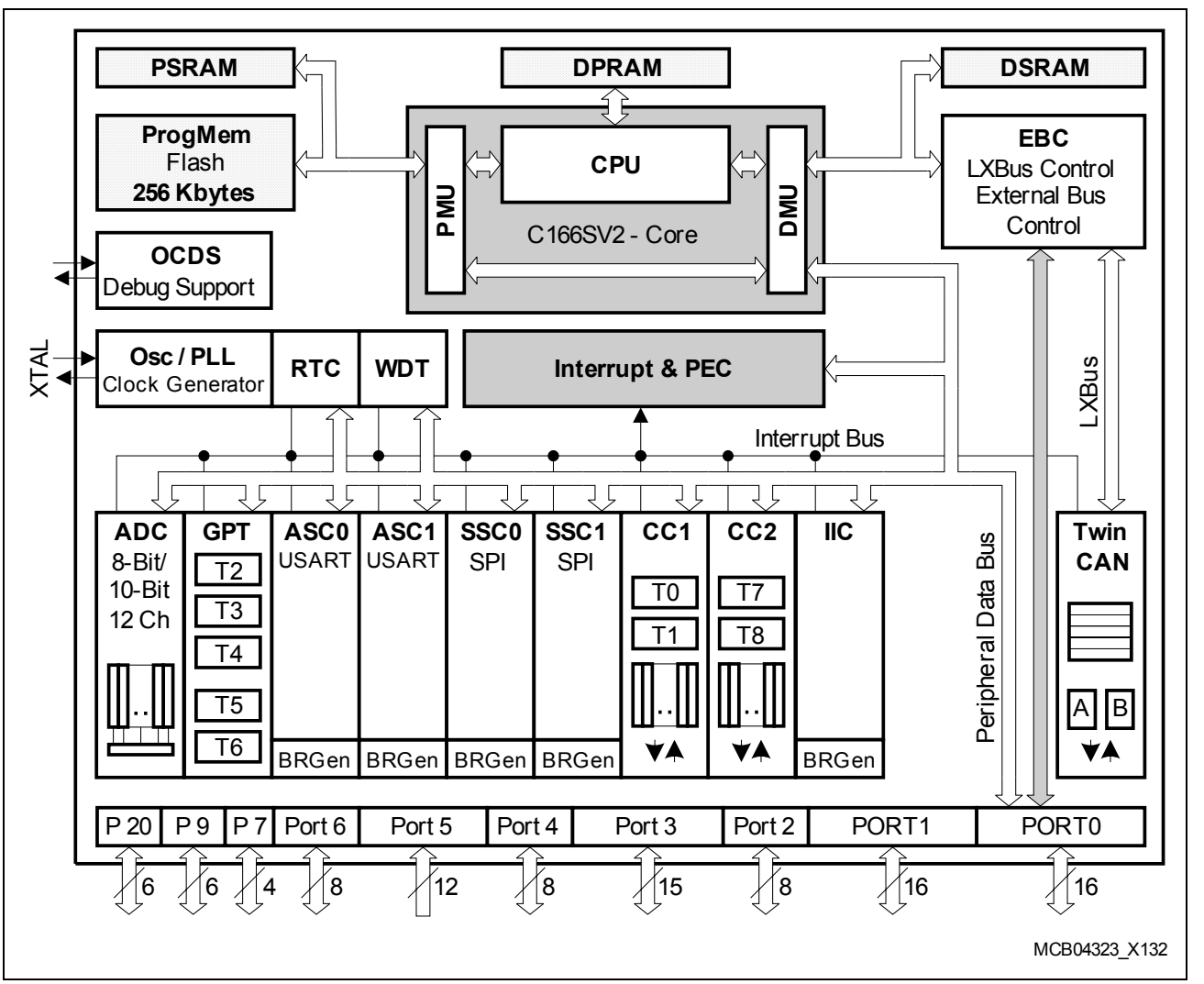

Figure 3 Block Diagram

3.1 Memory Subsystem and Organization

The memory space of the XC161 is configured in a Von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bitaddressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

256 Kbytes of on-chip Flash memory store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors, one 32-Kbyte sector, and three 64-Kbyte sectors. Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
Programming typically takes 2 ms per 128-byte block (5 ms max.), erasing a sector typically takes 200 ms (500 ms max.).

6 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

4 Kbytes of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, and general purpose register banks. A register

1) Each two 8-Kbyte sectors are combined for write-protection purposes.

bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bitaddressable. When used by a GPR, any location in the DPRAM is bitaddressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see **Table 3**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Table 3 XC161 Memory Map[1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
Flash register space	$FF'F000_H$	$FF'FFFF_H$	4 Kbytes	[3)]
Reserved (Access trap)	$FE'0000_H$	$FF'EFFF_H$	< 0.5 Mbytes	Minus Flash registers
Reserved for EPSRAM	$F8'1800_H$	$FD'FFFF_H$	378 Kbytes	–
Emul. Program SRAM[4)]	$F8'0000_H$	$F8'17FF_H$	6 Kbytes	2nd way to PSRAM
Reserved for PSRAM	$E0'1800_H$	$F7'FFFF_H$	< 1.5 Mbytes	Minus PSRAM
Program SRAM	$E0'0000_H$	$E0'17FF_H$	6 Kbytes	Maximum
Reserved for program memory	$C4'0000_H$	$DF'FFFF_H$	< 2 Mbytes	Minus Flash
Program Flash	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	–
Reserved	$BF'0000_H$	$BF'FFFF_H$	64 Kbytes	–
External memory area	$40'0000_H$	$BE'FFFF_H$	< 8 Mbytes	Minus reserved segment
External IO area[5)]	$20'0800_H$	$3F'FFFF_H$	< 2 Mbytes	Minus TwinCAN
TwinCAN registers	$20'0000_H$	$20'07FF_H$	2 Kbytes	–
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
Data RAMs and SFRs	$00'8000_H$	$00'FFFF_H$	32 Kbytes	Partly used
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) Accesses to the shaded areas generate external bus accesses.

2) The areas marked with “<” are slightly smaller than indicated, see column “Notes”.

3) Not defined register locations return a trap code.

4) The Emulation PSRAM (EPSRAM) realizes a 2nd access path to the PSRAM with a different timing.

5) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

- 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
- 16 … 24-bit Addresses, 16-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Access to very slow memories or modules with varying access times is supported via a particular ‘Ready’ function. The active level of the control input signal is selectable.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software. After enabling, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. In Slave Mode pin $\overline{HLDA}$ is switched to input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

The EBC also controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.