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Data Sheet, V2.3, Aug. 2006

# XC164CS-16F/16R
# XC164CS-8F/8R

## 16-Bit Single-Chip Microcontroller with C166SV2 Core


Microcontrollers

Never stop thinking

**Edition 2006-08**

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# XC164CS-16F/16R
# XC164CS-8F/8R

## 16-Bit Single-Chip Microcontroller with C166SV2 Core

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Never stop thinking

**XC164CS**
**Revision History: V2.3, 2006-08**

Previous Version(s):
V2.2, 2006-03
V2.1, 2003-06
V2.0, 2003-01
V1.0, 2002-03

| Page | Subjects (major changes since last revision) |
|---|---|
| 48 | Instructions Set Summary improved. |
| 51 | Footnote added about pin XTAL1 belonging to $V_{DDI}$ power domain. |
| 55 | Footnote added about amplitude at XTAL1 pin. |
| 75 | Green Package added. |
| 74 | Thermal Resistance: $R_{THA}$ replaced by $R_{\Theta JC}$ and $R_{\Theta JL}$ because $R_{THA}$ strongly depends on the external system (PCB, environment). $P_{DISS}$ removed, because no static parameter, but derived from thermal resistance. |

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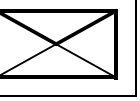

# Table of Contents

# 1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 × 16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with up to 75 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 2/4 Kbytes On-Chip Data SRAM (DSRAM)[1)]
  - 2 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 64/128 Kbytes On-Chip Program Memory (Flash Memory or Mask ROM)[1)]
- On-Chip Peripheral Modules
  - 14-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55 µs or 2.15 µs)
  - Two 16-Channel General Purpose Capture/Compare Units (12 Input/Output Pins)
  - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip TwinCAN Interface (Rev. 2.0B active) with 32 Message Objects (Full CAN/Basic CAN) on Two CAN Nodes, and Gateway Functionality
  - On-Chip Real Time Clock
- Idle, Sleep, and Power Down Modes with Flexible Power Management

1) Depends on the respective derivative. The derivatives are listed in **Table 1**.

- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 12 Mbytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses
  - Selectable Address Bus Width
  - 16-Bit or 8-Bit Data Bus Width
  - Four Programmable Chip-Select Signals
- Up to 79 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Debug Support via JTAG Interface
- 100-Pin Green TQFP Package, 0.5 mm (19.7 mil) pitch (RoHS compliant)

## Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164CS please refer to your responsible sales representative or your local distributor.

*Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.*

This document describes several derivatives of the XC164CS group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164CS** throughout this document.

**Table 1 XC164CS Derivative Synopsis**

| Derivative[1)] | Temp. Range | Program Memory | On-Chip RAM | Interfaces |
|---|---|---|---|---|
| SAK-XC164CS-16F40F, SAK-XC164CS-16F20F | -40 °C to 125 °C | 128 Kbytes Flash | 2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM | ASC0, ASC1, SSC0, SSC1, CAN0, CAN1 |
| SAF-XC164CS-16F40F, SAF-XC164CS-16F20F | -40 °C to 85 °C | | | |
| SAK-XC164CS-8F40F, SAK-XC164CS-8F20F | -40 °C to 125 °C | 64 Kbytes Flash | 2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM | |
| SAF-XC164CS-8F40F, SAF-XC164CS-8F20F | -40 °C to 85 °C | | | |
| SAK-XC164CS-16R40F, SAK-XC164CS-16R20F | -40 °C to 125 °C | 128 Kbytes ROM | 2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM | ASC0, ASC1, SSC0, SSC1, CAN0, CAN1 |
| SAF-XC164CS-16R40F, SAF-XC164CS-16R20F | -40 °C to 85 °C | | | |
| SAK-XC164CS-8R40F, SAK-XC164CS-8R20F | -40 °C to 125 °C | 64 Kbytes ROM | 2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM | |
| SAF-XC164CS-8R40F, SAF-XC164CS-8R20F | -40 °C to 85 °C | | | |

1) This Data Sheet is valid for devices starting with and including design step AD of the Flash version, and design step AA of the ROM version.

# 2 General Device Information

## 2.1 Introduction

The XC164CS derivatives are high-performance members of the Infineon XC166 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 40 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM or Flash, program RAM, and data RAM.

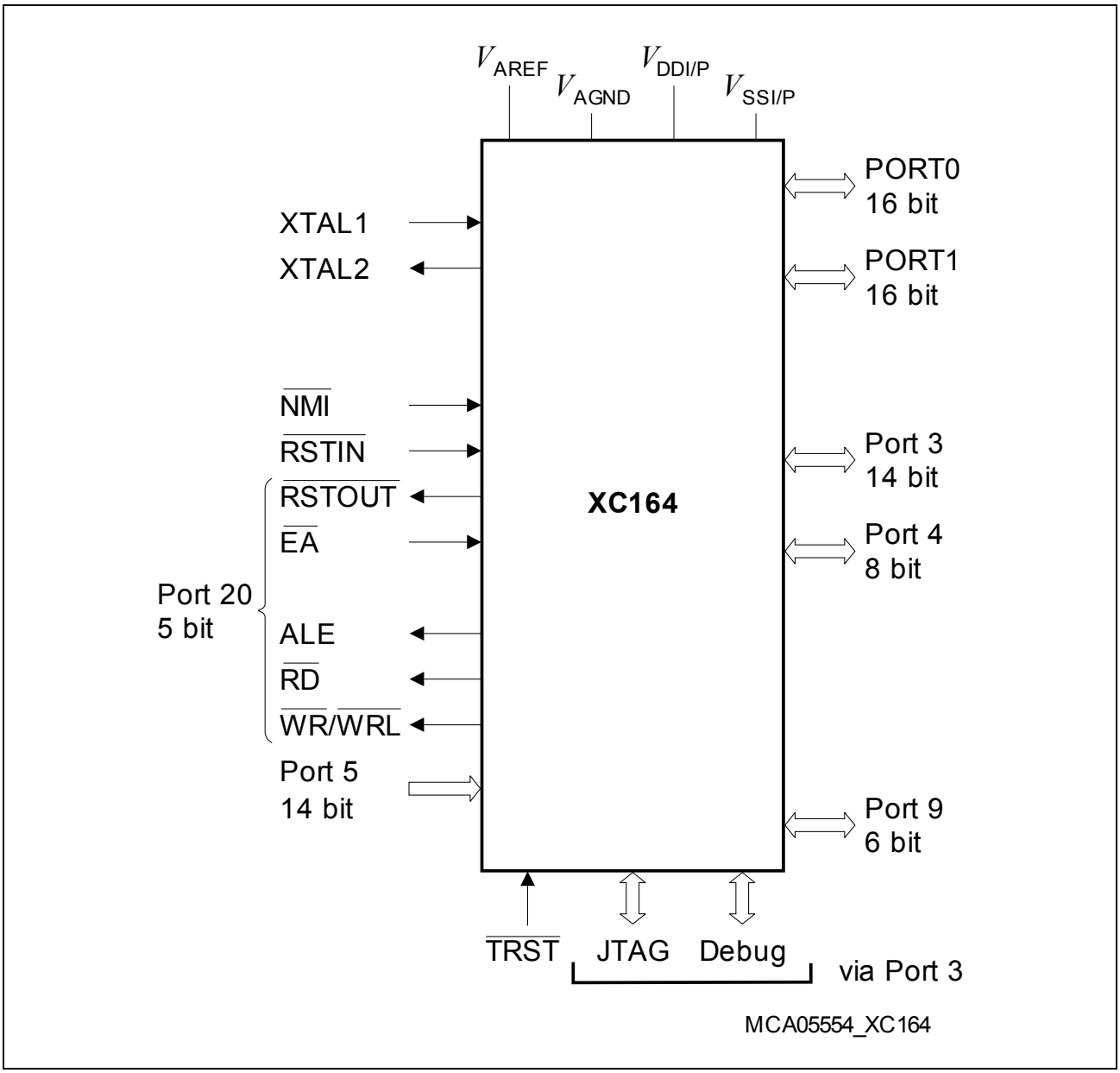


**Figure 1 Logic Symbol**

## 2.2 Pin Configuration and Definition

The pins of the XC164CS are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN interface lines assigned to them.

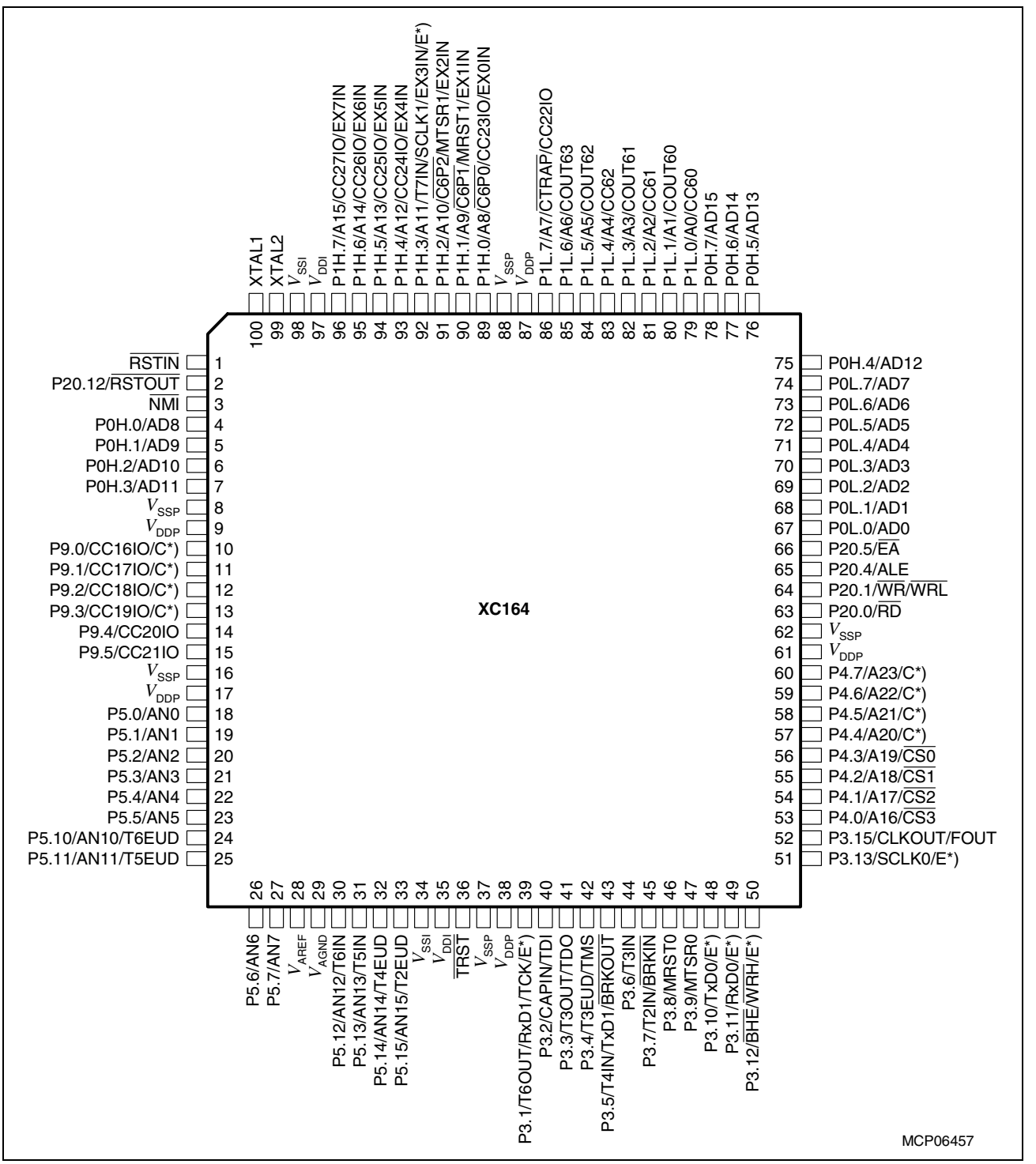


**Figure 2 Pin Configuration** (top view)

**Table 2 Pin Definitions and Functions**

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| $\overline{\text{RSTIN}}$ | 1 | I | Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the XC164CS. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles.<br>*Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.* |
| P20.12 | 2 | IO | For details, please refer to the description of **P20**. |
| $\overline{\text{NMI}}$ | 3 | I | Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the XC164CS into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode.<br>If not used, pin $\overline{\text{NMI}}$ should be pulled high externally. |
| P0H.0-P0H.3 | 4 … 7 | IO | For details, please refer to the description of **PORT0**. |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| **P9** | | IO | Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special).<br>The following Port 9 pins also serve for alternate functions:[1)] |
| P9.0 | 10 | I/O | CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp., |
| | | I | CAN1_RxD CAN Node B Receive Data Input, |
| | | I | EX7IN Fast External Interrupt 7 Input (alternate pin B) |
| P9.1 | 11 | I/O | CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp., |
| | | O | CAN1_TxD CAN Node B Transmit Data Output, |
| | | I | EX6IN Fast External Interrupt 6 Input (alternate pin B) |
| P9.2 | 12 | I/O | CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp. |
| | | I | CAN0_RxD CAN Node A Receive Data Input, |
| | | I | EX7IN Fast External Interrupt 7 Input (alternate pin A) |
| P9.3 | 13 | I/O | CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp., |
| | | O | CAN0_TxD CAN Node A Transmit Data Output, |
| | | I | EX6IN Fast External Interrupt 6 Input (alternate pin A) |
| P9.4 | 14 | I/O | CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp. |
| P9.5 | 15 | I/O | CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp. |
| **P5** | | I | Port 5 is a 14-bit input-only port.<br>The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs: |
| P5.0 | 18 | I | AN0 |
| P5.1 | 19 | I | AN1 |
| P5.2 | 20 | I | AN2 |
| P5.3 | 21 | I | AN3 |
| P5.4 | 22 | I | AN4 |
| P5.5 | 23 | I | AN5 |
| P5.10 | 24 | I | AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp. |
| P5.11 | 25 | I | AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp. |
| P5.6 | 26 | I | AN6 |
| P5.7 | 27 | I | AN7 |
| P5.12 | 30 | I | AN12, T6IN GPT2 Timer T6 Count/Gate Input |
| P5.13 | 31 | I | AN13, T5IN GPT2 Timer T5 Count/Gate Input |
| P5.14 | 32 | I | AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp. |
| P5.15 | 33 | I | AN15, T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl. Inp. |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function | |
|---|---|---|---|---|
| $\overline{\text{TRST}}$ | 36 | I | Test-System Reset Input. A high level at this pin activates the XC164CS's debug system. For normal system operation, pin $\overline{\text{TRST}}$ should be held low. | |
| **P3** | | IO | Port 3 is a 14-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special).<br>The following Port 3 pins also serve for alternate functions: | |
| P3.1 | 39 | O | T6OUT | GPT2 Timer T6 Toggle Latch Output, |
| | | I/O | RxD1 | ASC1 Data Input (Async.) or Inp./Outp. (Sync.), |
| | | I | EX1IN | Fast External Interrupt 1 Input (alternate pin A), |
| | | I | TCK | Debug System: JTAG Clock Input |
| P3.2 | 40 | I | CAPIN | GPT2 Register CAPREL Capture Input, |
| | | I | TDI | Debug System: JTAG Data In |
| P3.3 | 41 | O | T3OUT | GPT1 Timer T3 Toggle Latch Output, |
| | | O | TDO | Debug System: JTAG Data Out |
| P3.4 | 42 | I | T3EUD | GPT1 Timer T3 External Up/Down Control Input |
| | | I | TMS | Debug System: JTAG Test Mode Selection |
| P3.5 | 43 | I | T4IN | GPT1 Timer T4 Count/Gate/Reload/Capture Inp |
| | | O | TxD1 | ASC0 Clock/Data Output (Async./Sync.), |
| | | O | $\overline{\text{BRKOUT}}$ | Debug System: Break Out |
| P3.6 | 44 | I | T3IN | GPT1 Timer T3 Count/Gate Input |
| P3.7 | 45 | I | T2IN | GPT1 Timer T2 Count/Gate/Reload/Capture Inp |
| | | I | $\overline{\text{BRKIN}}$ | Debug System: Break In |
| P3.8 | 46 | I/O | MRST0 | SSC0 Master-Receive/Slave-Transmit In/Out. |
| P3.9 | 47 | I/O | MTSR0 | SSC0 Master-Transmit/Slave-Receive Out/In. |
| P3.10 | 48 | O | TxD0 | ASC0 Clock/Data Output (Async./Sync.), |
| | | I | EX2IN | Fast External Interrupt 2 Input (alternate pin B) |
| P3.11 | 49 | I/O | RxD0 | ASC0 Data Input (Async.) or Inp./Outp. (Sync.), |
| | | I | EX2IN | Fast External Interrupt 2 Input (alternate pin A) |
| P3.12 | 50 | O | $\overline{\text{BHE}}$ | External Memory High Byte Enable Signal, |
| | | O | $\overline{\text{WRH}}$ | External Memory High Byte Write Strobe, |
| | | I | EX3IN | Fast External Interrupt 3 Input (alternate pin B) |
| P3.13 | 51 | I/O | SCLK0 | SSC0 Master Clock Output / Slave Clock Input., |
| | | I | EX3IN | Fast External Interrupt 3 Input (alternate pin A) |
| P3.15 | 52 | O | CLKOUT | System Clock Output (= CPU Clock), |
| | | O | FOUT | Programmable Frequency Output |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| **P4** | | IO | Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special).<br>Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:[1)] |
| P4.0 | 53 | O | $\overline{A16}$ Least Significant Segment Address Line, |
| | | O | $\overline{CS3}$ Chip Select 3 Output |
| P4.1 | 54 | O | $\overline{A17}$ Segment Address Line, |
| | | O | $\overline{CS2}$ Chip Select 2 Output |
| P4.2 | 55 | O | $\overline{A18}$ Segment Address Line, |
| | | O | $\overline{CS1}$ Chip Select 1 Output |
| P4.3 | 56 | O | $\overline{A19}$ Segment Address Line, |
| | | O | $\overline{CS0}$ Chip Select 0 Output |
| P4.4 | 57 | O | A20 Segment Address Line, |
| | | I | CAN1_RxD CAN Node B Receive Data Input, |
| | | I | EX5IN Fast External Interrupt 5 Input (alternate pin B) |
| P4.5 | 58 | O | A21 Segment Address Line, |
| | | I | CAN0_RxD CAN Node A Receive Data Input, |
| | | I | EX4IN Fast External Interrupt 4 Input (alternate pin B) |
| P4.6 | 59 | O | A22 Segment Address Line, |
| | | O | CAN0_TxD CAN Node A Transmit Data Output, |
| | | I | EX5IN Fast External Interrupt 5 Input (alternate pin A) |
| P4.7 | 60 | O | A23 Most Significant Segment Address Line, |
| | | I | CAN0_RxD CAN Node A Receive Data Input, |
| | | O | CAN1_TxD CAN Node B Transmit Data Output, |
| | | I | EX4IN Fast External Interrupt 4 Input (alternate pin A) |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function | |
|---|---|---|---|---|
| **P20** | | IO | Port 20 is a 5-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special).<br>The following Port 20 pins also serve for alternate functions: | |
| P20.0 | 63 | O | $\overline{RD}$ | External Memory Read Strobe, activated for every external instruction or data read access. |
| P20.1 | 64 | O | $\overline{WR}$/$\overline{WRL}$ | External Memory Write Strobe.<br>In $\overline{WR}$-mode this pin is activated for every external data write access.<br>In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. |
| P20.4 | 65 | O | ALE | Address Latch Enable Output.<br>Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. |
| P20.5 | 66 | I | $\overline{EA}$ | External Access Enable pin.<br>**A low level** at this pin during and after Reset forces the XC164CS to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory.<br>**A high level** forces the XC164CS to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'. |
| P20.12 | 2 | O | $\overline{RSTOUT}$ | Internal Reset Indication Output.<br>**Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset.<br>**Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software. |
| | | | *Note: Port 20 pins may input configuration values (see $\overline{EA}$).* | |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| **PORT0** | | IO | PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. Each pin can be programmed for input (output driver in high-impedance state) or output. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. |
| P0L.0-P0L.7 | 67 - 74 | | |
| P0H.0-P0H.3 | 4 - 7 | | |
| P0H.4-P0H.7 | 75 - 78 | | **Demultiplexed bus modes:**<br>8-bit data bus: P0H = I/O, P0L = D7 - D0<br>16-bit data bus: P0H = D15 - D8, P0L = D7 - D0<br>**Multiplexed bus modes:**<br>8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0<br>16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0<br>*Note: At the end of an external reset ($\overline{EA}$ = 0) PORT0 also may input configuration values* |
| **PORT1** | | IO | PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions: |
| P1L.0 | 79 | I/O | CC60 CAPCOM6: Input / Output of Channel 0 |
| P1L.1 | 80 | O | COUT60 CAPCOM6: Output of Channel 0 |
| P1L.2 | 81 | I/O | CC61 CAPCOM6: Input / Output of Channel 1 |
| P1L.3 | 82 | O | COUT61 CAPCOM6: Output of Channel 1 |
| P1L.4 | 83 | I/O | CC62 CAPCOM6: Input / Output of Channel 2 |
| P1L.5 | 84 | O | COUT62 CAPCOM6: Output of Channel 2 |
| P1L.6 | 85 | O | $\overline{COUT63}$ Output of 10-bit Compare Channel |
| P1L.7 | 86 | I | $\overline{CTRAP}$ CAPCOM6: Trap Input<br>$\overline{CTRAP}$ is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled). |
| P1H | … | I/O | CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.<br>… continued … |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| **PORT1** (cont'd) | | IO | … continued … |
| P1H.0 | 89 | I | $\overline{\text{CC6POS0}}$ CAPCOM6: Position 0 Input, |
| | | I | EX0IN Fast External Interrupt 0 Input (default pin), |
| | | I/O | $\overline{\text{CC23IO}}$ CAPCOM2: CC23 Capture Inp./Compare Outp. |
| P1H.1 | 90 | I | $\overline{\text{CC6POS1}}$ CAPCOM6: Position 1 Input, |
| | | I | EX1IN Fast External Interrupt 1 Input (default pin), |
| | | I/O | $\overline{\text{MRST1}}$ SSC1 Master-Receive/Slave-Transmit In/Out. |
| P1H.2 | 91 | I | $\overline{\text{CC6POS2}}$ CAPCOM6: Position 2 Input, |
| | | I | EX2IN Fast External Interrupt 2 Input (default pin), |
| | | I/O | MTSR1 SSC1 Master-Transmit/Slave-Receive Out/Inp. |
| P1H.3 | 92 | I | T7IN CAPCOM2: Timer T7 Count Input, |
| | | I/O | SCLK1 SSC1 Master Clock Output / Slave Clock Input, |
| | | I | EX3IN Fast External Interrupt 3 Input (default pin), |
| | | I | EX0IN Fast External Interrupt 0 Input (alternate pin A) |
| P1H.4 | 93 | I/O | CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp., |
| | | I | EX4IN Fast External Interrupt 4 Input (default pin) |
| P1H.5 | 94 | I/O | CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp., |
| | | I | EX5IN Fast External Interrupt 5 Input (default pin) |
| P1H.6 | 95 | I/O | CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp., |
| | | I | EX6IN Fast External Interrupt 6 Input (default pin) |
| P1H.7 | 96 | I/O | CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp., |
| | | I | EX7IN Fast External Interrupt 7 Input (default pin) |
| $\overline{\text{XTAL2}}$ | 99 | O | XTAL2: Output of the oscillator amplifier circuit |
| XTAL1 | 100 | I | XTAL1: Input to the oscillator amplifier and input to the internal clock generator<br>To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.<br>*Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for $V_{DDI}$.* |
| $V_{AREF}$ | 28 | – | Reference voltage for the A/D converter. |
| $V_{AGND}$ | 29 | – | Reference ground for the A/D converter. |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| $V_{DDI}$ | 35, 97 | – | Digital Core Supply Voltage (On-Chip Modules):<br>+2.5 V during normal operation and idle mode.<br>Please refer to the **Operating Condition Parameters** |
| $V_{DDP}$ | 9, 17, 38, 61, 87 | – | Digital Pad Supply Voltage (Pin Output Drivers):<br>+5 V during normal operation and idle mode.<br>Please refer to the **Operating Condition Parameters** |
| $V_{SSI}$ | 34, 98 | – | **Digital Ground.**<br>Connect decoupling capacitors to adjacent $V_{DD}/V_{SS}$ pin pairs as close as possible to the pins.<br>All $V_{SS}$ pins must be connected to the ground-line or ground-plane. |
| $V_{SSP}$ | 8, 16, 37, 62, 88 | – | |

1) The CAN interface lines are assigned to ports P4 and P9 under software control.

# 3 Functional Description

The architecture of the XC164CS combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164CS.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164CS.

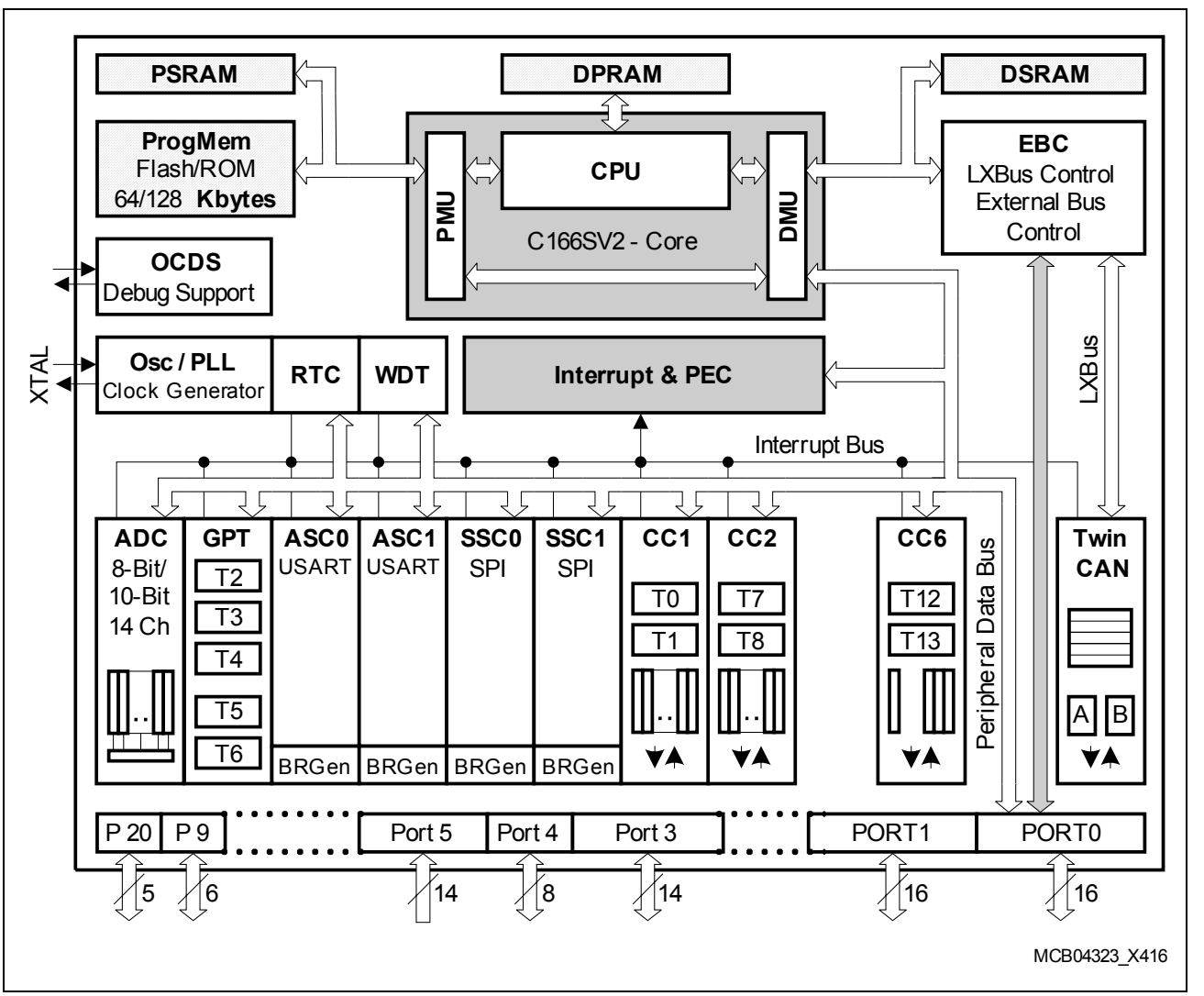


**Figure 3 Block Diagram**

## 3.1 Memory Subsystem and Organization

The memory space of the XC164CS is configured in a Von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bitaddressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory, ROM, and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

**64/128 Kbytes**[1] **of on-chip Flash memory or mask-programmable ROM** store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors, one 32-Kbyte sector, and one 64-Kbyte sector. Each sector can be separately write protected[2], erased and programmed (in blocks of 128 Bytes). The complete Flash or ROM area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
For timing characteristics, please refer to **Section 4.4.2**.

**2 Kbytes of on-chip Program SRAM (PSRAM)** are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

**2/4 Kbytes**[1] **of on-chip Data SRAM (DSRAM)** are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses.

**2 Kbytes of on-chip Dual-Port RAM (DPRAM)** are provided as a storage for user defined variables, for the system stack, and general purpose register banks. A register

1) Depends on the respective derivative. The derivatives are listed in **Table 1**.

2) Each two 8-Kbyte sectors are combined for write-protection purposes.

bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bitaddressable. When used by a GPR, any location in the DPRAM is bitaddressable.

**1024 bytes (2 × 512 bytes)** of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see **Table 3**) of external RAM and/or ROM can be connected to the microcontroller.

**Table 3 XC164CS Memory Map[1)]**

| Address Area | Start Loc. | End Loc. | Area Size[2)] | Notes |
|---|---|---|---|---|
| Flash register space | $FF'F000_H$ | $FF'FFFF_H$ | 4 Kbytes | Flash only[3)] |
| Reserved (Acc. trap) | $F8'0000_H$ | $FF'EFFF_H$ | < 0.5 Mbytes | Minus Flash register space |
| Reserved for PSRAM | $E0'0800_H$ | $F7'FFFF_H$ | < 1.5 Mbytes | Minus PSRAM |
| Program SRAM | $E0'0000_H$ | $E0'07FF_H$ | 2 Kbytes | Maximum |
| Reserved for program memory | $C2'0000_H$ | $DF'FFFF_H$ | < 2 Mbytes | Minus Flash/ROM |
| Program Flash/ROM | $C0'0000_H$ | $C1'FFFF_H$ | 128 Kbytes | [4)] |
| Reserved | $BF'0000_H$ | $BF'FFFF_H$ | 64 Kbytes | – |
| External memory area | $40'0000_H$ | $BE'FFFF_H$ | < 8 Mbytes | Minus reserved segment |
| External IO area[5)] | $20'0800_H$ | $3F'FFFF_H$ | < 2 Mbytes | Minus TwinCAN |
| TwinCAN registers | $20'0000_H$ | $20'07FF_H$ | 2 Kbytes | – |
| External memory area | $01'0000_H$ | $1F'FFFF_H$ | < 2 Mbytes | Minus segment 0 |
| Data RAMs and SFRs | $00'8000_H$ | $00'FFFF_H$ | 32 Kbytes | Partly used[4)] |
| External memory area | $00'0000_H$ | $00'7FFF_H$ | 32 Kbytes | – |

1) Accesses to the shaded areas generate external bus accesses.
2) The areas marked with “<” are slightly smaller than indicated, see column “Notes”.
3) Not defined register locations return a trap code.
4) Depends on the respective derivative. The derivatives are listed in **Table 1**.
5) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

## 3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

- 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
- 16 … 24-bit Addresses, 16-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 4 external $\overline{CS}$ signals (3 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

*Note: The chip select signal of address window 4 is not available on a pin.*

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

The EBC also controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

## 3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.

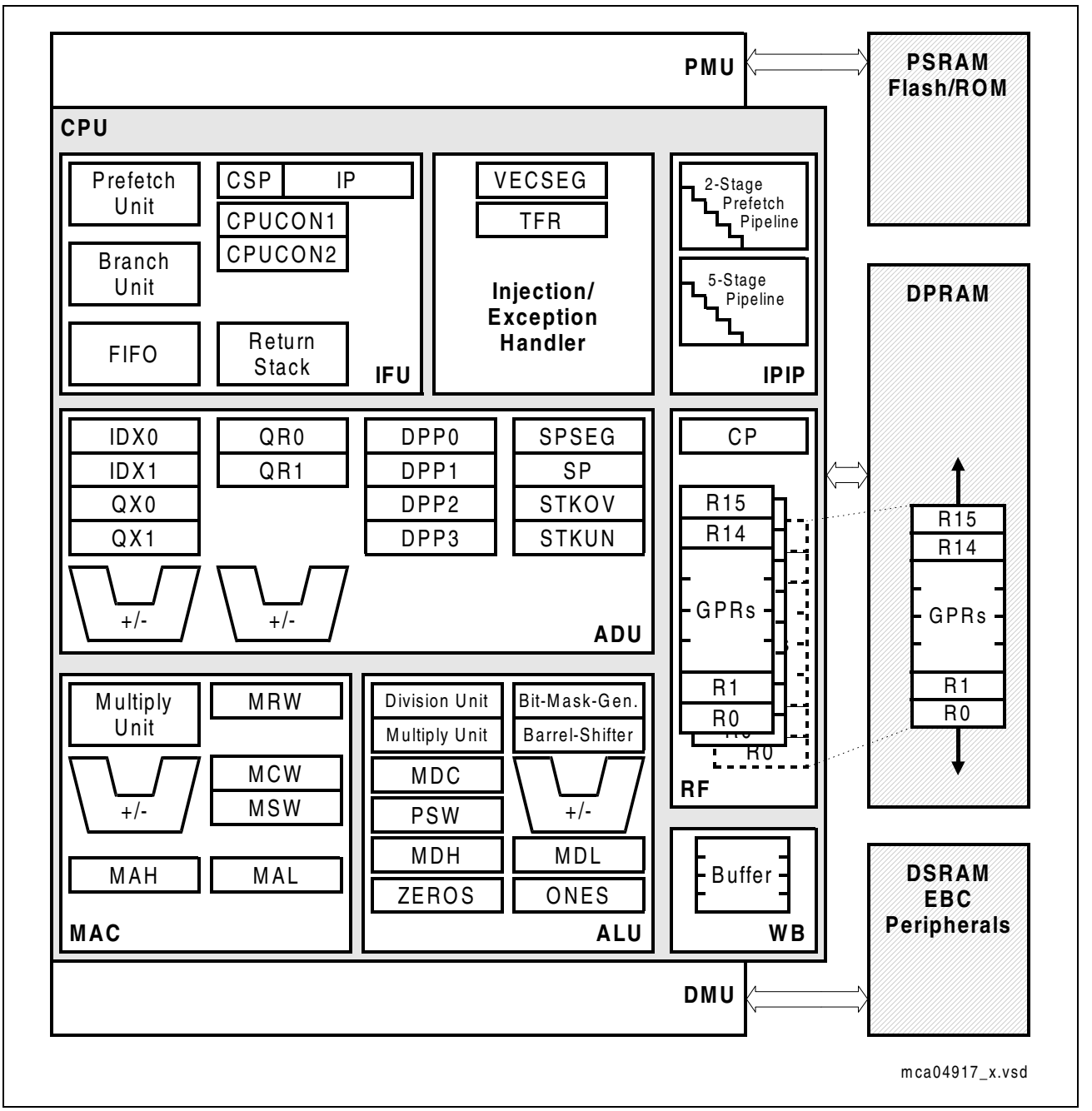


**Figure 4 CPU Block Diagram**

Based on these hardware provisions, most of the XC164CS's instructions can be executed in just one machine cycle which requires 25 ns at 40 MHz CPU clock. For

example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a division algorithm is performed in 18 to 21 CPU cycles, depending on the data and division type. Four cycles are always visible, the rest runs in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 wordwide GPRs each at its disposal. The global register bank is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active global register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164CS instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

## 3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164CS is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164CS supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164CS has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

**Table 4** shows all of the possible XC164CS interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

*Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).*