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16/32-Bit

Architecture

**XC2232N, XC2234N,
XC2236N, XC2238N**

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance

XC2000 Family / Value Line

Data Sheet

V1.5 2013-02

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27	Added AB step marking.
79	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
81	Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”.
82	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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**16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance
XC223xN (XC2000 Family)**

1 Summary of Features

For a quick overview and easy reference, the features of the XC223xN are summarized here.

- High-performance CPU with five-stage pipeline and MPU
 - 12.5 ns instruction cycle @ 80 MHz CPU clock (single-cycle execution)
 - One-cycle 32-bit addition and subtraction with 40-bit result
 - One-cycle multiplication (16 × 16 bit)
 - Background division (32 / 16 bit) in 21 cycles
 - One-cycle multiply-and-accumulate (MAC) instructions
 - Enhanced Boolean bit manipulation facilities
 - Zero-cycle jump execution
 - Additional instructions to support HLL and operating systems
 - Register-based design with multiple variable register banks
 - Fast context switching support with two additional local register banks
 - 16 Mbytes total linear address space for code and data
 - 1,024 Bytes on-chip special function register area (C166 Family compatible)
 - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 96 interrupt nodes
 - Selectable external inputs for interrupt generation and wake-up
 - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
 - 8 Kbytes on-chip stand-by RAM (SBRAM)
 - 2 Kbytes on-chip dual-port RAM (DPRAM)
 - Up to 16 Kbytes on-chip data SRAM (DSRAM)
 - Up to 16 Kbytes on-chip program/data SRAM (PSRAM)
 - Up to 320 Kbytes on-chip program memory (Flash memory)
 - Memory content protection through Error Correction Code (ECC)

Summary of Features

- On-Chip Peripheral Modules
 - Two synchronizable A/D Converters with up to 9 channels, 10-bit resolution, conversion time below 1 μ s, optional data preprocessing (data reduction, range check), broken wire detection
 - 16-channel general purpose capture/compare unit (CC2)
 - Two capture/compare units for flexible PWM signal generation (CCU6x)
 - Multi-functional general purpose timer unit with 5 timers
 - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
 - On-chip MultiCAN interface (Rev. 2.0B active) with up to 256 message objects (Full CAN/Basic CAN) on 6 CAN node
 - On-chip system timer and on-chip real time clock
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable watchdog timer and oscillator watchdog
- Up to 40 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 64-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the temperature range:
 - SAF-...: -40°C to 85°C
 - SAH-...: -40°C to 110°C
 - SAK-...: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC223xN please contact your sales representative or local distributor.

This document describes several derivatives of the XC223xN group:

Basic Device Types are readily available and
Special Device Types are only available on request.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XC223xN** is used for all derivatives throughout this document.

1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XC223xN Basic Device Types

Derivative¹⁾	Flash Memory²⁾	PSRAM DSRAM³⁾	Capt./Comp. Modules⁴⁾	ADC⁵⁾ Chan.	Interfaces⁵⁾
XC2236N-24F40L	192 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 4 Serial Chan.
XC2236N-40F80L	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 4 Serial Chan.
XC2238N-40F80L	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	7 + 2	6 CAN Node, 6 Serial Chan.

1) The 80 MHz type is marked ...80L. The 40 MHz type is marked ...40L.

2) Specific information about the on-chip Flash memory in [Table 3](#).

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Due to bonding limitations in the XC223xN devices only a subset of the CCU61 features can be used. The module has the T12 and T13 timer inputs and no outputs connected. Therefore only CCU61 timers can be triggered from external. This can typically be used for periodic triggering of ADCs.

5) Specific information about the available channels in [Table 5](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC223xN Special Device Types

Derivative¹⁾	Flash Memory²⁾	PSRAM DSRAM³⁾	Capt./Comp. Modules⁴⁾	ADC⁵⁾ Chan.	Interfaces⁵⁾
XC2232N-40FxL	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	7 + 2	3 CAN Nodes, 6 Serial Chan.
XC2232N-24FxL	192 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60/1	7 + 2	3 CAN Nodes, 6 Serial Chan.
XC2232N-8FxL	64 Kbytes	4 Kbytes 4 Kbytes	CC2 CCU60/1	7 + 2	3 CAN Nodes, 6 Serial Chan.
XC2234N-40FxL	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 2 Serial Chan.
XC2234N-24FxL	192 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 2 Serial Chan.
XC2234N-16FxL	128 Kbytes	4 Kbytes 4 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 2 Serial Chan.
XC2236N-40FxL	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 4 Serial Chan.
XC2236N-24FxL	192 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 4 Serial Chan.
XC2236N-16FxL	128 Kbytes	4 Kbytes 4 Kbytes	CC2 CCU60/1	7 + 2	1 CAN Node, 4 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 20, 40, 66 or 80.

2) Specific information about the on-chip Flash memory in [Table 3](#).

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Due to bonding limitations in the XC223xN devices only a subset of the CCU61 features can be used. The module has the T12 and T13 timer inputs and no outputs connected. Therefore only CCU61 timers can be triggered from external. This can typically be used for periodic triggering of ADCs.

5) Specific information about the available channels in [Table 5](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Summary of Features

1.3 Definition of Feature Variants

The XC223xN types are offered with several Flash memory sizes. [Table 3](#) and [Table 4](#) describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range ¹⁾	2nd Range	3rd Range
320 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C4'FFFF _H	n.a.
192 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C1'FFFF _H	C4'0000 _H ... C4'FFFF _H
128 Kbytes	C0'0000 _H ... C0'FFFF _H	C4'0000 _H ... C4'FFFF _H	n.a.
64 Kbytes	C0'0000 _H ... C0'FFFF _H	n.a.	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0 ¹⁾	Flash 1
320	256	64
192	128	64
128	64	64
64	64	-

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XC223xN types are offered with different interface options. [Table 5](#) lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
7 ADC0 channels	CH0, CH2, CH4, CH8, CH10, CH13, CH15
2 ADC1 channels	CH0, CH4
1 CAN node	CAN0 64 message objects
2 CAN nodes	CAN0, CAN1 64 message objects

Table 5 Interface Channel Association (cont'd)

Total Number	Available Channels / Message Objects
3 CAN nodes	CAN0, CAN1, CAN2 64 message objects
6 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4, CAN5 256 message objects
2 serial channels	U0C0, U0C1
4 serial channels	U0C0, U0C1, U1C0, U1C1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

The XC223xN types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.

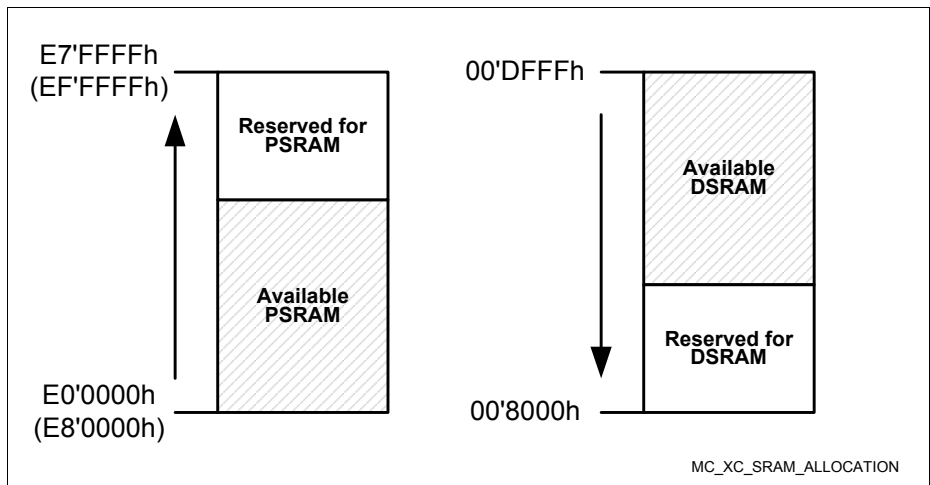


Figure 1 SRAM Allocation

2 General Device Information

The XC223xN series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

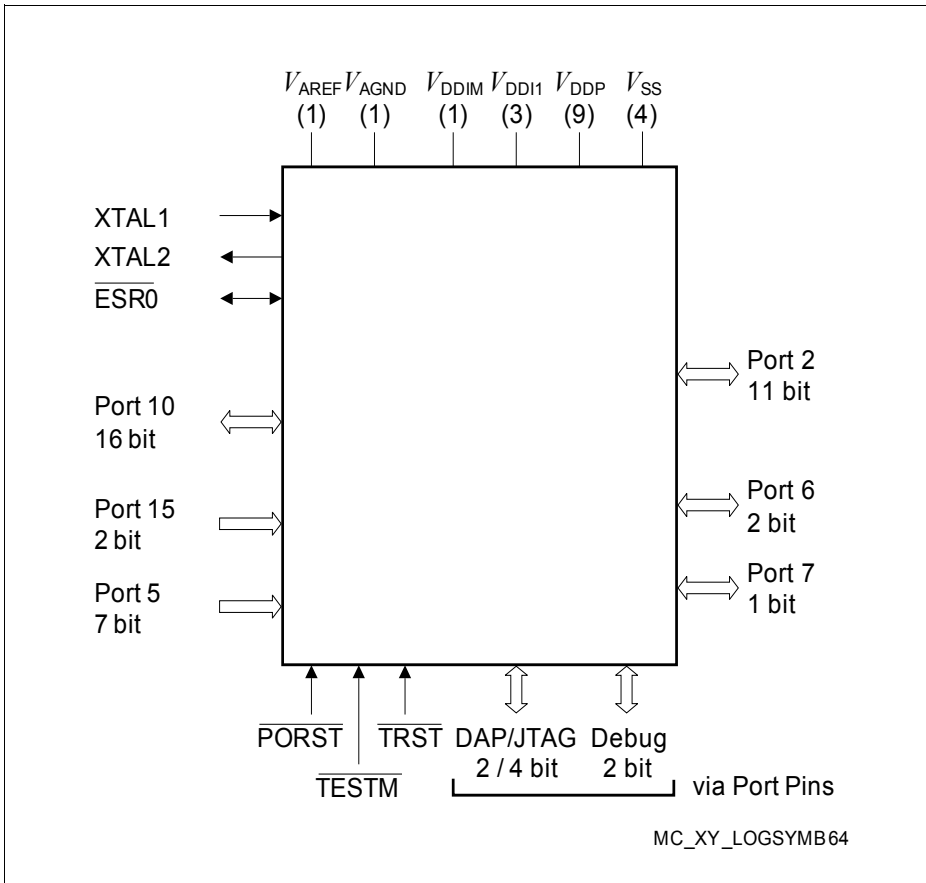


Figure 2 XC223xN Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC223xN are described in detail in [Table 6](#), which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

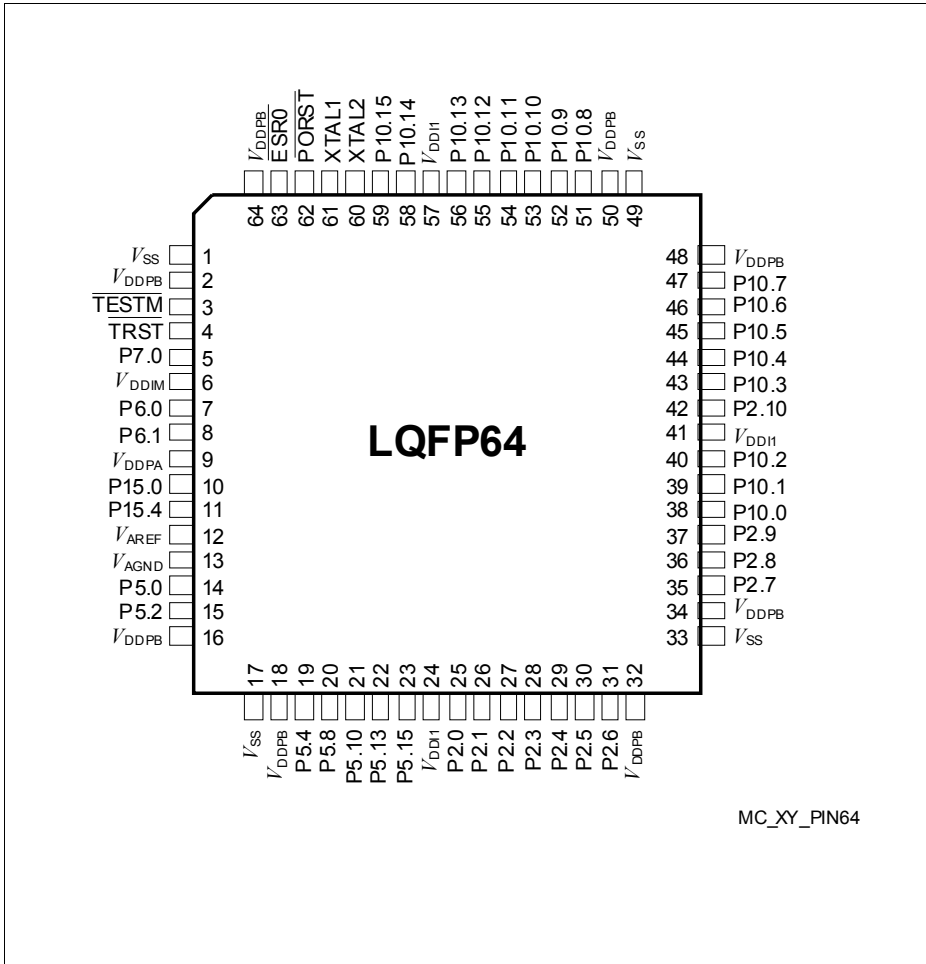


Figure 3 XC223xN Pin Configuration (top view)

Key to Pin Definitions

- **Ctrl.:** The output signal for a port pin is selected by bit field PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bit field PC to 1x00_B, output O1 is selected by 1x01_B, etc. Output signal OH is controlled by hardware.
- **Type:** Indicates the pad type and its power supply domain (A, B, M, 1).
 - St: Standard pad
 - Sp: Special pad e.g. XTALx
 - DP: Double pad - can be used as standard or high speed pad
 - In: Input only pad
 - PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.
4	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC223xN's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.
5	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P6.0	O0 / I	DA/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	DA/A	External Analog MUX Control Output 0 (ADC0)
	TxDC2	O2	DA/A	CAN Node 2 Transmit Data Output
	BRKOUT	O3	DA/A	OCDS Break Signal Output
	ADCx_REQG TyG	I	DA/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	DA/A	USIC1 Channel 1 Shift Data Input
8	P6.1	O0 / I	DA/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	DA/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	DA/A	USIC1 Channel 1 Shift Data Output
	ADCx_REQT RyE	I	DA/A	External Request Trigger Input for ADC0/1
	RxDC2E	I	DA/A	CAN Node 2 Receive Data Input
	ESR1_6	I	DA/A	ESR1 Trigger Input 6
10	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
11	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6INA	I	In/A	GPT12E Timer T6 Count/Gate Input
12	V_{AREF}	-	PS/A	Reference Voltage for A/D Converters ADC0/1
13	V_{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
14	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
15	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
19	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
20	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	ADC1_CH8	I	In/A	Analog Input Channel 8 for ADC1
	CCU6x_T12H RC	I	In/A	External Run Control Input for T12 of CCU60/1
	CCU6x_T13H RC	I	In/A	External Run Control Input for T13 of CCU60/1
	U2C0_DX0F	I	In/A	USIC2 Channel 0 Shift Data Input
21	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	ADC1_CH10	I	In/A	Analog Input Channel 10 for ADC1
	BRKIN_A	I	In/A	OCDS Break Signal Input
	U2C1_DX0F	I	In/A	USIC2 Channel 1 Shift Data Input
	CCU61_T13 HRA	I	In/A	External Run Control Input for T13 of CCU61
22	P5.13	I	In/A	Bit 13 of Port 5, General Purpose Input
	ADC0_CH13	I	In/A	Analog Input Channel 13 for ADC0
23	P5.15	I	In/A	Bit 15 of Port 5, General Purpose Input
	ADC0_CH15	I	In/A	Analog Input Channel 15 for ADC0
	RxDC2F	I	In/A	CAN Node 2 Receive Data Input
25	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output
	TxDC5	O1	St/B	CAN Node 5 Transmit Data Output
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input
	T5INB	I	St/B	GPT12E Timer T5 Count/Gate Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
26	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output
	TxDC0	O1	St/B	CAN Node 0 Transmit Data Output
	RxDC5C	I	St/B	CAN Node 5 Receive Data Input
	T5EUDB	I	St/B	GPT12E Timer T5 External Up/Down Control Input
	ESR1_5	I	St/B	ESR1 Trigger Input 5
27	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output
	TxDC1	O1	St/B	CAN Node 1 Transmit Data Output
	ESR2_5	I	St/B	ESR2 Trigger Input 5
28	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input
29	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.
	ESR1_0	I	St/B	ESR1 Trigger Input 0
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input
	RxDC1A	I	St/B	CAN Node 1 Receive Data Input
30	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input
	ESR1_10	I	St/B	ESR1 Trigger Input 10

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
31	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
	ESR2_6	I	St/B	ESR2 Trigger Input 6
35	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
	ESR2_7	I	St/B	ESR2 Trigger Input 7
36	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output
	CC2_CC21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
37	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_CC22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	CLKIN1	I	St/B	Clock Signal Input 1
	TCK_A	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
38	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_CC60	O2	St/B	CCU60 Channel 0 Output
	CCU60_CC60INA	I	St/B	CCU60 Channel 0 Input
	ESR1_2	I	St/B	ESR1 Trigger Input 2
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input
39	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU60_CC61	O2	St/B	CCU60 Channel 1 Output
	CCU60_CC61INA	I	St/B	CCU60 Channel 1 Input
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
40	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC6 2	O2	St/B	CCU60 Channel 2 Output
	CCU60_CC6 2INA	I	St/B	CCU60 Channel 2 Input
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
42	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_SELO 3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input
43	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output
	CCU60_COU T60	O2	St/B	CCU60 Channel 0 Output
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input
44	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO 3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COU T61	O2	St/B	CCU60 Channel 1 Output
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input
	ESR1_9	I	St/B	ESR1 Trigger Input 9

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
45	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLK OUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COU T62	O2	St/B	CCU60 Channel 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
46	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	U1C0_SELO 0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTR APA	I	St/B	CCU60 Emergency Trap Input
47	P10.7	O0 / I	St/B	Bit 7 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_COU T63	O2	St/B	CCU60 Channel 3 Output
	U0C1_DX0B	I	St/B	USIC0 Channel 1 Shift Data Input
	CCU60_CCP OS0A	I	St/B	CCU60 Position Input 0
	RxDC4C	I	St/B	CAN Node 4 Receive Data Input
	T4INB	I	St/B	GPT12E Timer T4 Count/Gate Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
51	P10.8	O0 / I	St/B	Bit 8 of Port 10, General Purpose Input/Output
	U0C0_MCLK OUT	O1	St/B	USIC0 Channel 0 Master Clock Output
	U0C1_SELO 0	O2	St/B	USIC0 Channel 1 Select/Control 0 Output
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output
	CCU60_CCP OS1A	I	St/B	CCU60 Position Input 1
	U0C0_DX1C	I	St/B	USIC0 Channel 0 Shift Clock Input
	BRKIN_B	I	St/B	OCDS Break Signal Input
	T3EUDB	I	St/B	GPT12E Timer T3 External Up/Down Control Input
52	P10.9	O0 / I	St/B	Bit 9 of Port 10, General Purpose Input/Output
	U0C0_SELO 4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_MCLK OUT	O2	St/B	USIC0 Channel 1 Master Clock Output
	CCU60_CCP OS2A	I	St/B	CCU60 Position Input 2
	TCK_B	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	T3INB	I	St/B	GPT12E Timer T3 Count/Gate Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
53	P10.10	O0 / I	St/B	Bit 10 of Port 10, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	U0C0_DX2C	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX1A	I	St/B	USIC0 Channel 1 Shift Clock Input
	TDI_B	IH	St/B	JTAG Test Data Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
54	P10.11	O0 / I	St/B	Bit 11 of Port 10, General Purpose Input/Output
	U1C0_SCLKOUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	BRKOUT	O2	St/B	OCDS Break Signal Output
	U1C0_DX1D	I	St/B	USIC1 Channel 0 Shift Clock Input
	RxDC2B	I	St/B	CAN Node 2 Receive Data Input
	TMS_B	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
55	P10.12	O0 / I	St/B	Bit 12 of Port 10, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	TDO_B	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U1C0_DX0C	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX1E	I	St/B	USIC1 Channel 0 Shift Clock Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
56	P10.13	O0 / I	St/B	Bit 13 of Port 10, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	U1C0_SELO 3	O3	St/B	USIC1 Channel 0 Select/Control 3 Output
	U1C0_DX0D	I	St/B	USIC1 Channel 0 Shift Data Input
58	P10.14	O0 / I	St/B	Bit 14 of Port 10, General Purpose Input/Output
	U1C0_SELO 1	O1	St/B	USIC1 Channel 0 Select/Control 1 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	ESR2_2	I	St/B	ESR2 Trigger Input 2
	U0C1_DX0C	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC3C	I	St/B	CAN Node 3 Receive Data Input
59	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO 2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input
60	XTAL2	O	Sp/M	Crystal Oscillator Amplifier Output
61	XTAL1	I	Sp/M	Crystal Oscillator Amplifier Input To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .
	ESR2_9	I	St/B	ESR2 Trigger Input 9
62	PORST	I	In/B	Power On Reset Input A low level at this pin resets the XC223xN completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.