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16/32-Bit

Architecture

XC2310S

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance
XC2000 Family / Compact Line

Data Sheet

V1.2 2012-07

Microcontrollers

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Revision History: V1.2 2012-07

Previous Versions: V1.0 2010-12, V1.1 2011-09	
Page	Subjects (major changes since last revision)
49, 50	The value of absolute sum of overload currents parameter in absolute maximum rating parameter and operating conditions tables are switched.
71	Table description on coding of bit field LEVxV is updated.

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Table of Contents

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC2310S (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC2310S are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 15.2 ns instruction cycle @ 66 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 46 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 15.2 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 2 Kbytes on-chip data SRAM (DSRAM)
  - 4 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 64 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC) for Flash memory and through parity for RAMs

- On-Chip Peripheral Modules
  - Synchronizable 12-bit A/D Converter with up to 8 channels, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Capture/compare unit for flexible PWM signal generation (CCU60)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 2 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip system timer and on-chip real time clock
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable window watchdog timer and oscillator watchdog
- Up to 28 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP), Single-Pin DAP (SPD) or JTAG interface
- 38-pin Green TSSOP package, 0.5 mm (10.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range[1]:
  - SAF-…: -40°C to 85°C
  - SAH-…: -40°C to 110°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC2310S please contact your sales representative or local distributor.

This document describes several derivatives of the XC2310S group:

Basic Device Types are readily available and
Special Device Types are only available on request.

1) Not all derivatives are offered in all temperature ranges.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XC2310S** is used for all derivatives throughout this document.

1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XC2310S Basic Device Types

Derivative[1]	Flash Memory[2]	PSRAM DSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
XC2310S-8FxR	64 Kbytes	4 Kbytes 2 Kbytes	CC2 CCU60	8	2 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 40 or 66.
2) Specific information about the on-chip Flash memory in **Table 3**.
3) All derivatives additionally provide 2 Kbytes DPRAM.
4) Specific information about the available channels in **Table 5**.

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC2310S Special Device Types

Derivative[1]	Flash Memory[2]	PSRAM DSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
None					

1) x is a placeholder for available speed grade in MHz. Can be 40 or 66.
2) Specific information about the on-chip Flash memory in **Table 3**.
3) All derivatives additionally provide 2 Kbytes DPRAM.
4) Specific information about the available channels in **Table 5**.

1.3 Definition of Feature Variants

The XC2310S types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
64 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'0FFF_H$	n.a.
32 Kbytes	$C0'0000_H$ … $C0'7FFF_H$	n.a.	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
64	64	n.a.
32	32	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC2310S types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
8 ADC0 channels	CH0, CH2, CH3, CH4, CH8, CH16, CH17, CH19
2 serial channels	U0C0, U0C1

2 General Device Information

The XC2310S series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 66 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

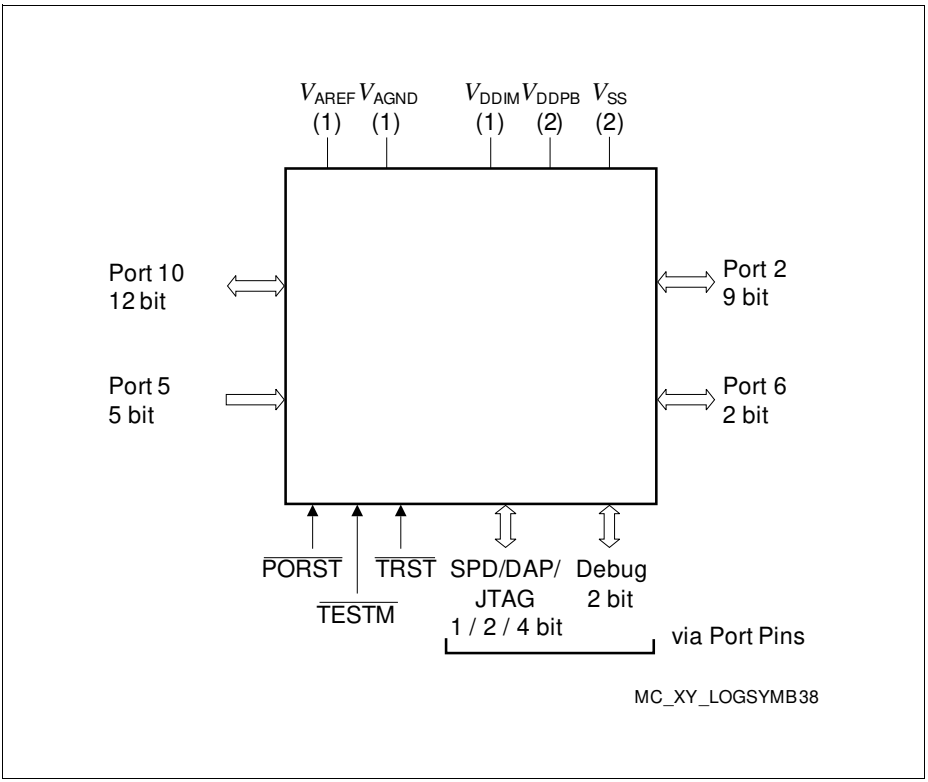

Figure 1 XC2310S Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC2310S are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

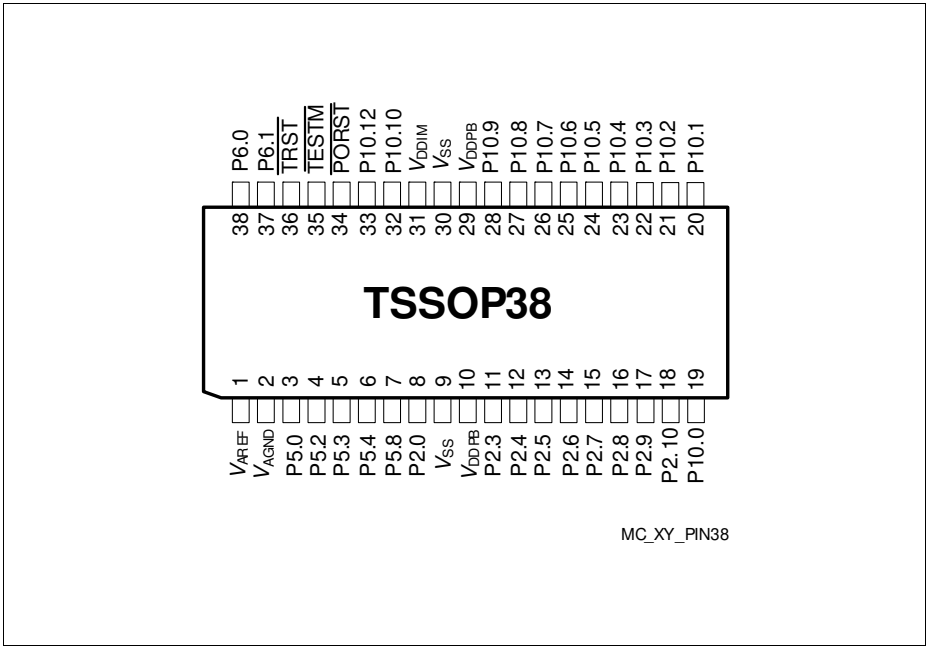

Figure 2 XC2310S Pin Configuration (top view)

Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (B, M).
  – St: Standard pad
  – DA: Digital IO and analog input
  – In: Input only pad
  – PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
35	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
36	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC2310S's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
37	P6.1	O0 / I	DA/B	**Bit 1 of Port 6, General Purpose Input/Output**
	ADC0_CH17	I	DA/B	**Analog Input Channel 17 for ADC0**
	EMUX1	O1	DA/B	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	DA/B	**GPT12E Timer T3 Toggle Latch Output**
	ADC0_REQTRyE	I	DA/B	**External Request Trigger Input for ADC0**
	ESR1_6	I	DA/B	**ESR1 Trigger Input 6**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
38	P6.0	O0 / I	DA/B	**Bit 0 of Port 6, General Purpose Input/Output**
	ADC0_CH16	I	DA/B	**Analog Input Channel 16 for ADC0**
	EMUX0	O1	DA/B	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	DA/B	**OCDS Break Signal Output**
	ADC0_REQGTyG	I	DA/B	**External Request Gate Input for ADC0**
3	P5.0	I	In/B	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/B	**Analog Input Channel 0 for ADC0**
4	P5.2	I	In/B	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/B	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/B	**JTAG Test Data Input**
5	P5.3	I	In/B	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/B	**Analog Input Channel 3 for ADC0**
	T3INA	I	In/B	**GPT12E Timer T3 Count/Gate Input**
6	P5.4	I	In/B	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/B	**Analog Input Channel 4 for ADC0**
	T3EUDA	I	In/B	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/B	**JTAG Test Mode Selection Input**
7	P5.8	I	In/B	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/B	**Analog Input Channel 8 for ADC0**
	CCU60_T12HRC	I	In/B	**External Run Control Input for T12 of CCU60**
	CCU60_T13HRC	I	In/B	**External Run Control Input for T13 of CCU60**
8	P2.0	O0 / I	DA/B	**Bit 0 of Port 2, General Purpose Input/Output**
	ADC0_CH19	I	DA/B	**Analog Input Channel 19 for ADC0**
	T5INB	I	DA/B	**GPT12E Timer T5 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
11	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CC2_CC16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input**
12	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CC2_CC17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
13	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CC2_CC18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	ESR1_10	I	St/B	**ESR1 Trigger Input 10**
14	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_SELO1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_CC19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	CLKIN1	I	St/B	**Clock Signal Input 1**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	ESR2_6	I	St/B	**ESR2 Trigger Input 6**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
15	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_SELO 0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_SELO 1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_CC20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR2_7	I	St/B	**ESR2 Trigger Input 7**
16	P2.8	O0 / I	St/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	St/B	**Programmable Clock Signal Output**
	CC2_CC21	O3 / I	St/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	U0C1_DX1D	I	St/B	**USIC0 Channel 1 Shift Clock Input**
17	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CC2_CC22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	C1	I	St/B	**Configuration Pin 1**
	TCK_A	I	St/B	**DAP0/JTAG Clock Input**
18	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_SELO 3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_CC23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPINA	I	St/B	**GPT12E Register CAPREL Capture Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
19	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
20	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
21	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
22	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
23	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO 3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COU T61	O2	St/B	**CCU60 Channel 1 Output**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**
24	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COU T62	O2	St/B	**CCU60 Channel 2 Output**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
25	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	CCU60_CTR APA	I	St/B	**CCU60 Emergency Trap Input**
26	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COU T63	O2	St/B	**CCU60 Channel 3 Output**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCP OS0A	I	St/B	**CCU60 Position Input 0**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
27	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
	ESR2_11	I	St/B	**ESR2 Trigger Input 11**
28	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_MCLKOUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	CCU60_CCPOS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	I	St/B	**DAP0/JTAG Clock Input**
	T3INB	I	St/B	**GPT12E Timer T3 Count/Gate Input**
32	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	TDI_B	I	St/B	**JTAG Test Data Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
33	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O2	St/B	**USIC0 Channel 0 Shift Data Output**
	TDO_A	OH	St/B	**DAP1/JTAG Test Data Output**
	SPD_0	I/OH	St/B	**SPD Input/Output**
	C0	I	St/B	**Configuration Pin 0**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
34	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XC2310S completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pullup device will hold this pin high when nothing is driving it.
1	V_{AREF}	-	PS/B	**Reference Voltage for A/D Converters ADC0**
2	V_{AGND}	-	PS/B	**Reference Ground for A/D Converters ADC0**
31	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDIM} pins must be connected to each other.
10, 29	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins.
9, 30	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane.

2.2 Identification Registers

The identification registers describe the current version of the XC2310S and of its modules.

Table 7 XC2310S Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820_H	$00'F07E_H$	
SCU_IDCHIP	5001_H	$00'F07C_H$	
SCU_IDMEM	3010_H	$00'F07A_H$	
SCU_IDPROG	1313_H	$00'F078_H$	
JTAG_ID	$001D'7083_H$	---	

3 Functional Description

The architecture of the XC2310S combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC2310S.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC2310S.

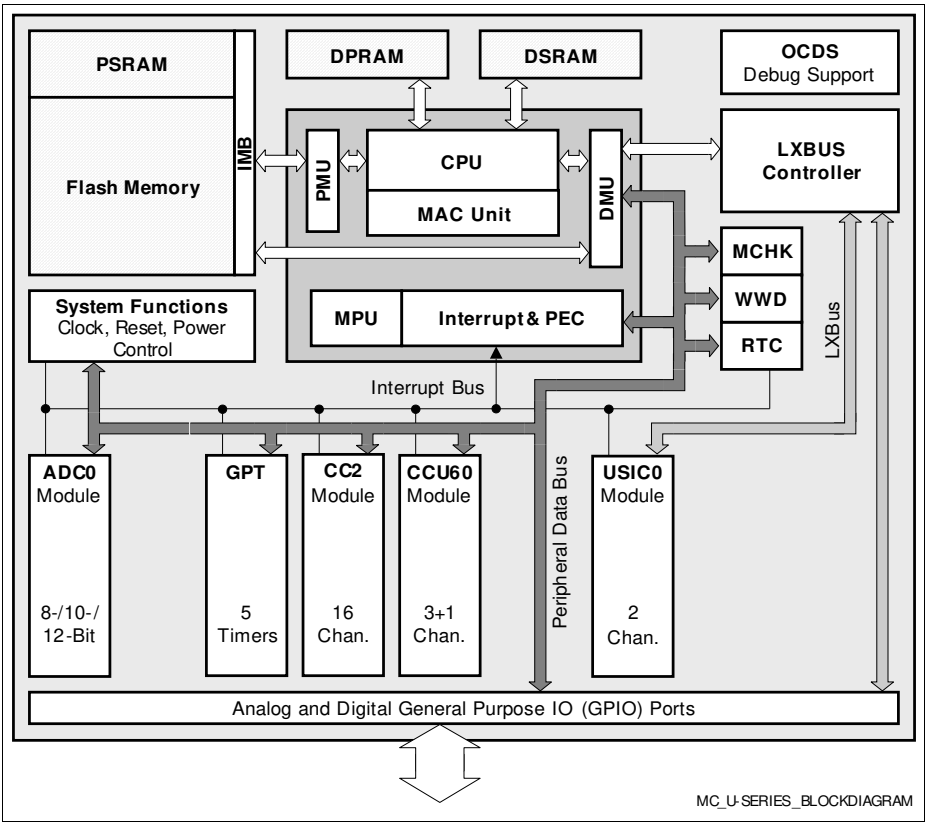

Figure 3 Block Diagram

3.1 Memory Subsystem and Organization

The memory space of the XC2310S is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC2310S **Memory Map** [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	FF'FF00$_H$	FF'FFFF$_H$	256 bytes	
Reserved	F0'0000$_H$	FF'FEFF$_H$	< 1 Mbyte	Minus IMB registers.
Reserved for EPSRAM	E8'1000$_H$	EF'FFFF$_H$	508 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000$_H$	E8'0FFF$_H$	up to 4 Kbytes	With Flash timing.
Reserved for PSRAM	E0'1000$_H$	E7'FFFF$_H$	508 Kbytes	Mirrors PSRAM
PSRAM	E0'0000$_H$	E0'0FFF$_H$	up to 4 Kbytes	Program SRAM.
Reserved for Flash	C1'1000$_H$	DF'FFFF$_H$	1980 Kbytes	
Flash 0	C0'0000$_H$	C1'0FFF$_H$	68 Kbytes[3)]	
External memory area	40'0000$_H$	BF'FFFF$_H$	8 Mbytes	
External IO area[4)]	21'0000$_H$	3F'FFFF$_H$	1984 Kbytes	
Reserved	20'B400$_H$	20'FFFF$_H$	19 Kbytes	
USIC0 alternate regs.	20'B000$_H$	20'B3FF$_H$	1 Kbytes	Accessed via LXBus controller
Reserved	20'4800$_H$	20'AFFF$_H$	26 Kbytes	
USIC0 registers	20'4000$_H$	20'47FF$_H$	2 Kbytes	Accessed via LXBus controller
Reserved	20'0000$_H$	20'3FFF$_H$	16 Kbytes	
External memory area	01'0000$_H$	1F'FFFF$_H$	1984 Kbytes	
SFR area	00'FE00$_H$	00'FFFF$_H$	0.5 Kbytes	
Dual-port RAM (DPRAM)	00'F600$_H$	00'FDFF$_H$	2 Kbytes	
Reserved for DPRAM	00'F200$_H$	00'F5FF$_H$	1 Kbytes	
ESFR area	00'F000$_H$	00'F1FF$_H$	0.5 Kbytes	
XSFR area	00'E000$_H$	00'EFFF$_H$	4 Kbytes	
Data SRAM (DSRAM)	00'D800$_H$	00'DFFF$_H$	2 Kbytes	