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16/32-Bit

Architecture

XC2330D, XC2331D

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance
XC2000 Family / Econo Line

Data Sheet

V1.3 2015-02

Microcontrollers

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V1.3 2015-02

Microcontrollers

XC233[01]D Data Sheet

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Page	Subjects (major changes since last revision)
6	Added SAK-XC2331D-20FxLR to Basic Device Types.
7	Moved SAK-XC2331D-20FxL from Basic Device Types to Special Device Types.
104	Added package type PG-LQFP-64-24.

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16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC233[01]D (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC233[01]D are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle @ 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 64 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 6 Kbytes on-chip data SRAM (DSRAM)
  - 4 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 160 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC) for Flash memory and through parity for RAMs

- On-Chip Peripheral Modules
  - Synchronizable 12-bit A/D Converter with up to 19 channels, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 4 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 32 message objects (Full CAN/Basic CAN) on 2 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable window watchdog timer and oscillator watchdog
- Up to 48 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP), Single-Pin DAP (SPD) or JTAG interface
- 64-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range[1]:
  - SAF-…: -40°C to 85°C
  - SAH-…: -40°C to 110°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC233[01]D please contact your sales representative or local distributor.

This document describes several derivatives of the XC233[01]D group:

Basic Device Types are readily available and
Special Device Types are only available on request.

1) Not all derivatives are offered in all temperature ranges.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XC233[01]D** is used for all derivatives throughout this document.

1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XC233[01]D Basic Device Types

Derivative[1]	Flash Memory[2]	PSRAM DSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
XC2331D-20FxLR	160 Kbytes	4 Kbytes 6 Kbytes	CC2 CCU60/3	19	2 CAN Nodes, 4 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 66 or 80.
2) Specific information about the on-chip Flash memory in **Table 3**.
3) All derivatives additionally provide 2 Kbytes DPRAM.
4) Specific information about the available channels in **Table 5**.

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC233[01]D Special Device Types

Derivative[1]	Flash Memory[2]	PSRAM DSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
XC2330D-12FxL	96 Kbytes	4 Kbytes 6 Kbytes	CC2 CCU60/3	19	4 Serial Chan.
XC2330D-20FxL	160 Kbytes	4 Kbytes 6 Kbytes	CC2 CCU60/3	19	4 Serial Chan.
XC2331D-12FxL	96 Kbytes	4 Kbytes 6 Kbytes	CC2 CCU60/3	19	2 CAN Nodes, 4 Serial Chan.
XC2331D-20FxL	160 Kbytes	4 Kbytes 6 Kbytes	CC2 CCU60/3	19	2 CAN Nodes, 4 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 66 or 80.

2) Specific information about the on-chip Flash memory in **Table 3**.

3) All derivatives additionally provide 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 5**.

1.3 Definition of Feature Variants

The XC233[01]D types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
160 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C2'0FFF_H$	$C4'0000_H$ … $C4'7FFF_H$
96 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'0FFF_H$	$C4'0000_H$ … $C4'7FFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
160	128	32
96	64	32

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC233[01]D types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
19 ADC0 channels	CH[11:0], CH13, CH[20:15]
2 CAN nodes	CAN0, CAN1 32 message objects
4 serial channels	U0C0, U0C1, U1C0, U1C1

2 General Device Information

The XC233[01]D series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

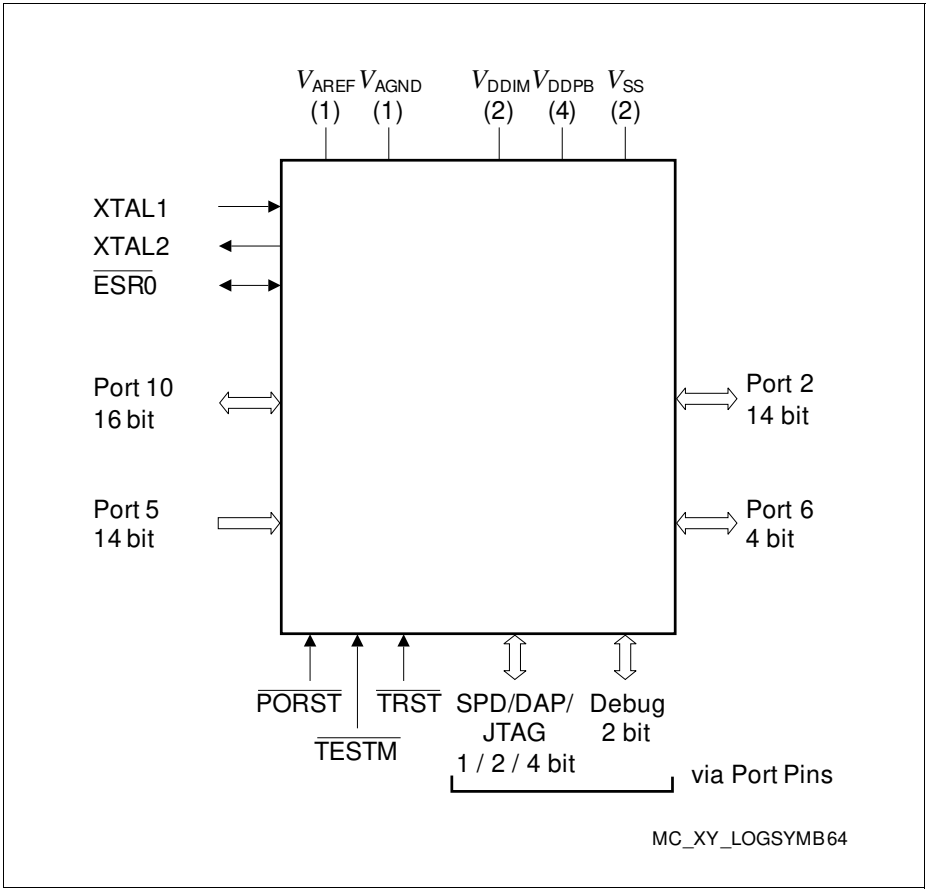

Figure 1 XC233[01]D Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC233[01]D are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

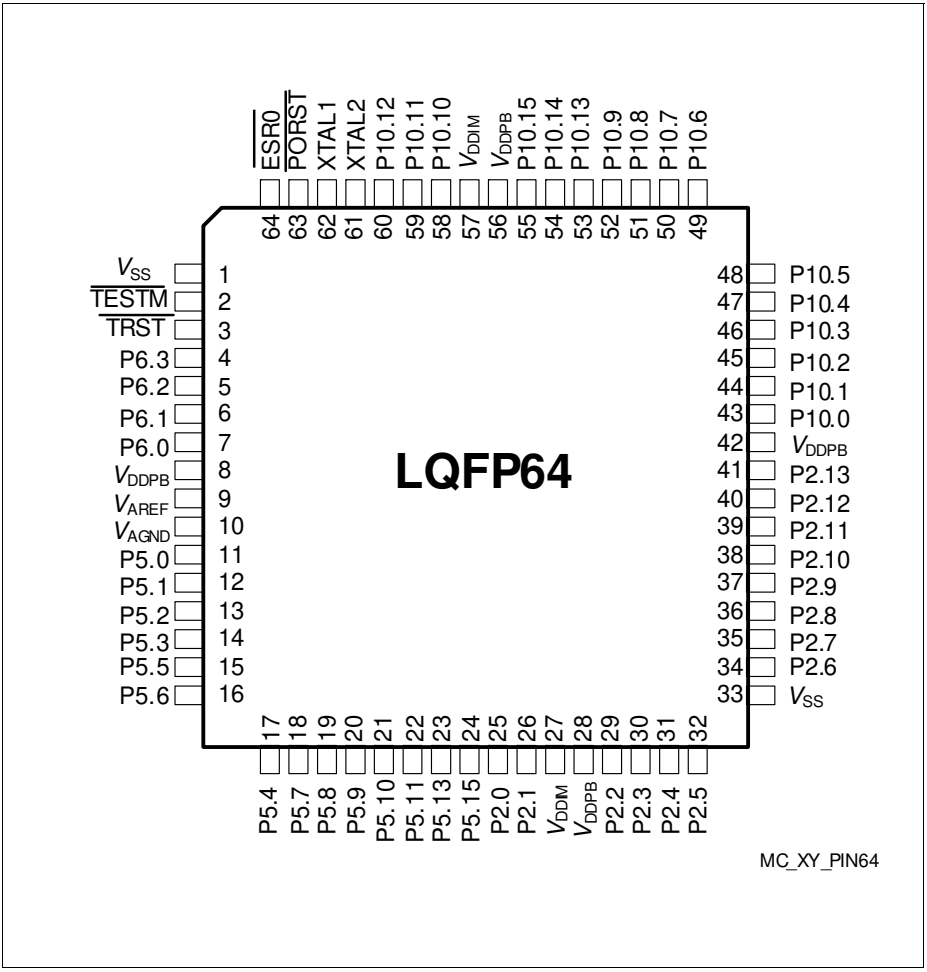

Figure 2 XC233[01]D Pin Configuration (top view)

Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (B, M).
  - St: Standard pad
  - Sp: Special pad e.g. XTALx
  - DA: Digital IO and analog input
  - In: Input only pad
  - PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
2	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
3	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC233[01]D's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
4	P6.3	O0 / I	St/B	**Bit 3 of Port 6, General Purpose Input/Output**
	CCU63_COUT62	O1	St/B	**CCU63 Channel 2 Output**
	T3OUT	O2	St/B	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_SELO0	O3	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C1_DX2D	I	St/B	**USIC1 Channel 1 Shift Control Input**
	ADC0_REQTRyF	I	St/B	**External Request Trigger Input for ADC0/1**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P6.2	O0 / I	DA/B	**Bit 2 of Port 6, General Purpose Input/Output**
	ADC0_CH18	I	DA/B	**Analog Input Channel 18 for ADC0**
	EMUX2	O1	DA/B	**External Analog MUX Control Output 2 (ADC0)**
	T6OUT	O2	DA/B	**GPT12E Timer T6 Toggle Latch Output**
	U1C1_SCLKOUT	O3	DA/B	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1C	I	DA/B	**USIC1 Channel 1 Shift Clock Input**
6	P6.1	O0 / I	DA/B	**Bit 1 of Port 6, General Purpose Input/Output**
	ADC0_CH17	I	DA/B	**Analog Input Channel 17 for ADC0**
	EMUX1	O1	DA/B	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	DA/B	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	DA/B	**USIC1 Channel 1 Shift Data Output**
	ADC0_REQTRyE	I	DA/B	**External Request Trigger Input for ADC0**
	CCU63_CTRAPB	I	DA/B	**CCU63 Emergency Trap Input**
	U1C1_DX0A	I	DA/B	**USIC1 Channel 1 Shift Data Input**
	ESR1_6	I	DA/B	**ESR1 Trigger Input 6**
7	P6.0	O0 / I	DA/B	**Bit 0 of Port 6, General Purpose Input/Output**
	ADC0_CH16	I	DA/B	**Analog Input Channel 16 for ADC0**
	EMUX0	O1	DA/B	**External Analog MUX Control Output 0 (ADC0)**
	CCU63_COUT61	O2	DA/B	**CCU63 Channel 1 Output**
	$\overline{\text{BRKOUT}}$	O3	DA/B	**OCDS Break Signal Output**
	ADC0_REQGTyG	I	DA/B	**External Request Gate Input for ADC0**
	U1C1_DX0E	I	DA/B	**USIC1 Channel 1 Shift Data Input**
11	P5.0	I	In/B	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/B	**Analog Input Channel 0 for ADC0**
12	P5.1	I	In/B	**Bit 1 of Port 5, General Purpose Input**
	ADC0_CH1	I	In/B	**Analog Input Channel 1 for ADC0**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P5.2	I	In/B	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/B	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/B	**JTAG Test Data Input**
14	P5.3	I	In/B	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/B	**Analog Input Channel 3 for ADC0**
	T3INA	I	In/B	**GPT12E Timer T3 Count/Gate Input**
15	P5.5	I	In/B	**Bit 5 of Port 5, General Purpose Input**
	ADC0_CH5	I	In/B	**Analog Input Channel 5 for ADC0**
	CCU60_T12HRB	I	In/B	**External Run Control Input for T12 of CCU60**
16	P5.6	I	In/B	**Bit 6 of Port 5, General Purpose Input**
	ADC0_CH6	I	In/B	**Analog Input Channel 6 for ADC0**
17	P5.4	I	In/B	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/B	**Analog Input Channel 4 for ADC0**
	CCU63_T12HRB	I	In/B	**External Run Control Input for T12 of CCU63**
	T3EUDA	I	In/B	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/B	**JTAG Test Mode Selection Input**
18	P5.7	I	In/B	**Bit 7 of Port 5, General Purpose Input**
	ADC0_CH7	I	In/B	**Analog Input Channel 7 for ADC0**
19	P5.8	I	In/B	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/B	**Analog Input Channel 8 for ADC0**
	CCU6x_T12HRC	I	In/B	**External Run Control Input for T12 of CCU60/3**
	CCU6x_T13HRC	I	In/B	**External Run Control Input for T13 of CCU60/3**
20	P5.9	I	In/B	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/B	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/B	**CAPCOM2 Timer T7 Count Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
21	P5.10	I	In/B	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/B	**Analog Input Channel 10 for ADC0**
	$\overline{\text{BRKIN\_A}}$	I	In/B	**OCDS Break Signal Input**
22	P5.11	I	In/B	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/B	**Analog Input Channel 11 for ADC0**
23	P5.13	I	In/B	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/B	**Analog Input Channel 13 for ADC0**
	CCU63_T13HRF	I	In/B	**External Run Control Input for T13 of CCU63**
	ERU_0B1	I	In/B	**External Request Unit Channel 0 Input B1**
24	P5.15	I	In/B	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/B	**Analog Input Channel 15 for ADC0**
25	P2.0	O0 / I	DA/B	**Bit 0 of Port 2, General Purpose Input/Output**
	CCU63_CC60	O2	DA/B	**CCU63 Channel 0 Output**
	RxDC0C	I	DA/B	**CAN Node 0 Receive Data Input**
	CCU63_CC60INB	I	DA/B	**CCU63 Channel 0 Input**
	ADC0_CH19	I	DA/B	**Analog Input Channel 19 for ADC0**
	T5INB	I	DA/B	**GPT12E Timer T5 Count/Gate Input**
26	P2.1	O0 / I	DA/B	**Bit 1 of Port 2, General Purpose Input/Output**
	TxDC0	O1	DA/B	**CAN Node 0 Transmit Data Output**
	CCU63_CC61	O2	DA/B	**CCU63 Channel 1 Output**
	CCU63_CC61INB	I	DA/B	**CCU63 Channel 1 Input**
	ADC0_CH20	I	DA/B	**Analog Input Channel 20 for ADC0**
	T5EUDB	I	DA/B	**GPT12E Timer T5 External Up/Down Control Input**
	ESR1_5	I	DA/B	**ESR1 Trigger Input 5**
	ERU_0A0	I	DA/B	**External Request Unit Channel 0 Input A0**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
29	P2.2	O0 / I	St/B	**Bit 2 of Port 2, General Purpose Input/Output**
	TxDC1	O1	St/B	**CAN Node 1 Transmit Data Output**
	CCU63_CC62	O2	St/B	**CCU63 Channel 2 Output**
	CCU63_CC62INB	I	St/B	**CCU63 Channel 2 Input**
	ESR2_5	I	St/B	**ESR2 Trigger Input 5**
	ERU_1A0	I	St/B	**External Request Unit Channel 1 Input A0**
30	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU63_COUT63	O2	St/B	**CCU63 Channel 3 Output**
	CC2_CC16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC0A	I	St/B	**CAN Node 0 Receive Data Input**
31	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
32	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	ESR1_10	I	St/B	**ESR1 Trigger Input 10**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
34	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_SELO 0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_SELO 1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_CC19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	CLKIN1	I	St/B	**Clock Signal Input 1**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**
	ESR2_6	I	St/B	**ESR2 Trigger Input 6**
35	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_SELO 0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_SELO 1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_CC20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR2_7	I	St/B	**ESR2 Trigger Input 7**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
	U1C0_DX0A	I	St/B	**USIC1 Channel 0 Shift Data Input**
36	P2.8	O0 / I	St/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	St/B	**Programmable Clock Signal Output**
	CC2_CC21	O3 / I	St/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	U0C1_DX1D	I	St/B	**USIC0 Channel 1 Shift Clock Input**
37	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_CC22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	C1	I	St/B	**Configuration Pin 1**
	TCK_A	I	St/B	**DAP0/JTAG Clock Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
38	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_SELO 3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_CC23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPINA	I	St/B	**GPT12E Register CAPREL Capture Input**
39	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_SELO 2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_SELO 2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
40	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_SELO 4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_SELO 3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	U1C1_SCLK OUT	O3	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
41,	P2.13	O0 / I	St/B	**Bit 13 of Port 2, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	CCU63_COU T60	O2	St/B	**CCU63 Channel 0 Output**
	U1C1_DX0B	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
44	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
45	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
46	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1D	I	St/B	**CAN Node 1 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO 3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COU T61	O2	St/B	**CCU60 Channel 1 Output**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**
48	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COU T62	O2	St/B	**CCU60 Channel 2 Output**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
49	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U1C0_DOUT	O2	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_SELO 0	O3	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX2D	I	St/B	**USIC1 Channel 0 Shift Control Input**
	CCU6x_CTR APA	I	St/B	**CCU60/CCU63 Emergency Trap Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
50	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	CCU63_COUT61	O3	St/B	**CCU63 Channel 1 Output**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCPOS0A	I	St/B	**CCU60 Position Input 0**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**
51	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U1C0_SCLKOUT	O3	St/B	**USIC1 Channel 0 Shift Clock Output**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	ESR2_11	I	St/B	**ESR2 Trigger Input 11**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
52	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_SELO 4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_MCLK OUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	TxDC1	O3	St/B	**CAN Node 1 Transmit Data Output**
	CCU60_CCP OS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	I	St/B	**DAP0/JTAG Clock Input**
	T3INB	I	St/B	**GPT12E Timer T3 Count/Gate Input**
53	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_SELO 3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
54	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_SELO 1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
55	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_SELO 2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**