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**IMPORTANT NOTE:** *Page, figure, and table numbers begin at 1 for each module, and each module has its own Revision History at the end. Use the PDF "Bookmarks" pane for easy navigation in this volume.*



**Summary of Virtex-II™ Features**

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- Differential Signaling
  - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
  - Bus LVDS I/O
  - Lightning Data Transport (LDT) I/O with current driver buffers
  - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
  - Built-in DDR input and output registers
- Proprietary high-performance SelectLink Technology
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V<sub>CCINT</sub>) Core Power Supply, Dedicated 3.3V V<sub>CCAUX</sub> Auxiliary and V<sub>CCO</sub> I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging ([www.xilinx.com/pbfree](http://www.xilinx.com/pbfree))
- 100% Factory Tested

Table 1: Virtex-II Field-Programmable Gate Array Family Members

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads <sup>(1)</sup>
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

**Notes:**

1. See details in [Table 2, "Maximum Number of User I/O Pads"](#).

## General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15  $\mu\text{m}$  / 0.12  $\mu\text{m}$  CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in [Table 1](#), the Virtex-II family comprises 11 members, ranging from 40K to 8M system gates.

## Packaging

Offerings include ball grid array (BGA) packages with 0.80 mm, 1.00 mm, and 1.27 mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

Wire-bond packages CS, FG, and BG are optionally available in Pb-free versions CSG, FGG, and BGG. See [Virtex-II Ordering Examples, page 6](#).

[Table 2](#) shows the maximum number of user I/Os available. The Virtex-II device/package combination table ([Table 6](#) at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: Maximum Number of User I/O Pads

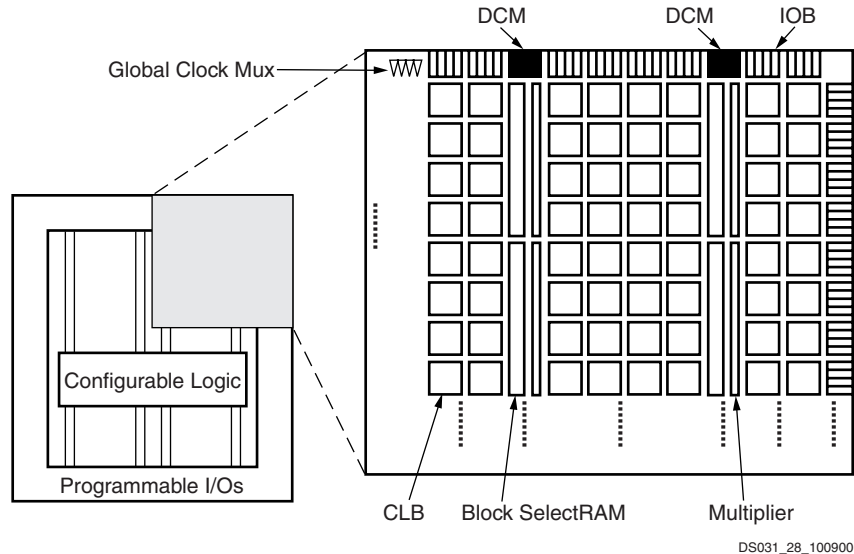
Device	Wire-Bond	Flip-Chip
XC2V40	88	-
XC2V80	120	-
XC2V250	200	-
XC2V500	264	-
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	-	624
XC2V3000	516	720
XC2V4000	-	912
XC2V6000	-	1,104
XC2V8000	-	1,108

## Architecture

### Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in **Figure 1**, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.



**Figure 1: Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during

configuration and can be reloaded to change the functions of the programmable elements.

### Virtex-II Features

This section briefly describes Virtex-II features.

#### Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

- HSTL (Class I, II, III, and IV)
- SSTL (3.3V and 2.5V, Class I and II)
- AGP-2X

The digitally controlled impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element.

The IOB elements also support the following differential signaling I/O standards:

- LVDS
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

### Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

### Block SelectRAM Memory

The block SelectRAM memory resources are 18 Kb of dual-port RAM, programmable from 16K x 1 bit to 512 x 36 bits, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in [Table 3](#).

**Table 3: Dual-Port And Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

A multiplier block is associated with each SelectRAM memory block. The multiplier block is a dedicated 18 x 18-bit multiplier and is optimized for operations based on the block SelectRAM content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

### Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clocking schemes.

Up to 12 DCM blocks are available. To generate de-skewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of 1/256 of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to any M/D ratio of the input clock frequency, where M and D are two integers. For the exact timing parameters, see [Virtex-II Electrical Characteristics](#).

Virtex-II devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each global clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM block is able to drive up to four of the 16 global clock MUX buffers.

### Routing Resources

The IOB, CLB, block SelectRAM, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column as well as massive secondary and local routing resources provide fast interconnect. Virtex-II buffered interconnects are relatively unaffected by net fanout and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

### Boundary Scan

Boundary scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II devices that complies with IEEE standards 1149.1 — 1993 and 1532. A system mode and a test mode are implemented. In system mode, a Virtex-II device performs its intended mission even while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The Virtex-II Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

### Configuration

Virtex-II devices are configured by loading data into internal configuration memory, using the following five modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration information.

### Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops/latches, distributed

SelectRAM, and block SelectRAM memory resources can be read back. This capability is useful for real-time debugging.

The Integrated Logic Analyzer (ILA) core and software provides a complete solution for accessing and verifying Virtex-II devices.

### Virtex-II Device/Package Combinations and Maximum I/O

Wire-bond and flip-chip packages are available. [Table 4](#) and [Table 5](#) show the maximum possible number of user I/Os in wire-bond and flip-chip packages, respectively. [Table 6](#) shows the number of available user I/Os for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG\_B, PWRDWN\_B, TCK, TDI, TDO, TMS, HSWAP\_EN, DXN, DXP, and RSVD) and VBATT.

*Table 4: Wire-Bond Packages Information*

Package <sup>(1)</sup>	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

**Notes:**

1. Wire-bond packages include FGG $nnn$  Pb-free versions. See [Virtex-II Ordering Examples \(Module 1\)](#).

*Table 5: Flip-Chip Packages Information*

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 6: Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)

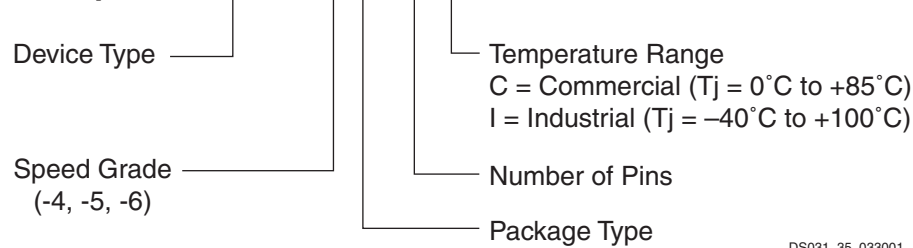
Package <sup>(1,2)</sup>	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144/CSG144	88	92	92	-	-	-	-	-	-	-	-
FG256/FGG256	88	120	172	172	172	-	-	-	-	-	-
FG456/FGG456	-	-	200	264	324	-	-	-	-	-	-
FG676/FGG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575/BGG575	-	-	-	-	328	392	408	-	-	-	-
BG728/BGG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

**Notes:**

1. All devices in a particular package are pinout (footprint) compatible. In addition, the FG456/FGG456 and FG676/FGG676 packages are compatible, as are the FF896 and FF1152 packages.
2. Wire-bond packages CS144, FG256, FG456, FG676, BG575, and BG728 are also available in Pb-free versions CSG144, FGG256, FGG456, FGG676, BGG575, and BGG728. See [Virtex-II Ordering Examples](#) for details on how to order.

## Virtex-II Ordering Examples

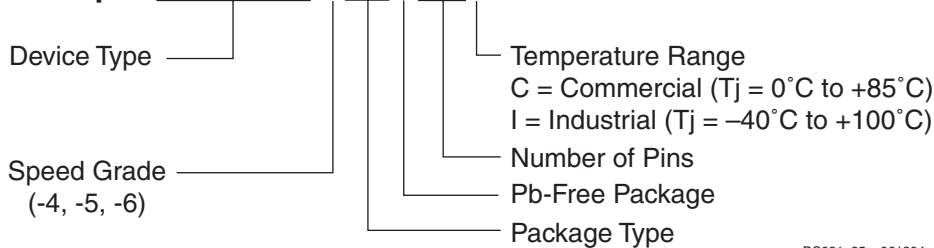
### Example: XC2V1000-5FG456C



DS031\_35\_033001

Figure 2: Virtex-II Ordering Example. Regular Package

### Example: XC2V3000-6BGG728C



DS031\_35a\_061804

Figure 3: Virtex-II Ordering Example. Pb-Free Package



## Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the <a href="#">Virtex-II Performance Characteristics</a> and <a href="#">Virtex-II Switching Characteristics</a> sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard).
04/02/01	1.5	Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	Made minor changes to items listed under <a href="#">Summary of Virtex-II™ Features</a> .
10/02/01	1.7	Minor edits.
07/16/02	1.8	Updated Virtex-II Device/Package Combinations shown in <a href="#">Table 6</a> .
09/26/02	1.9	Updated <a href="#">Table 2</a> and <a href="#">Table 6</a> to reflect supported Virtex-II Device/Package Combinations.
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See <a href="#">Table 13</a> , Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/24/04	3.3	Added references to available Pb-free wire-bond packages. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	<i>No changes in Module 1 for this revision.</i>
11/05/07	3.5	Updated copyright notice and legal disclaimer.

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## Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

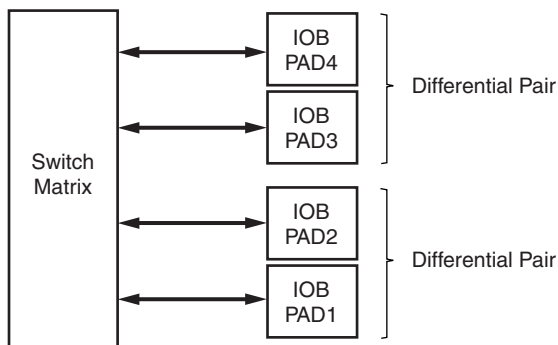
- [Virtex-II Platform FPGAs: Introduction and Overview \(Module 1\)](#)
- [Virtex-II Platform FPGAs: Functional Description \(Module 2\)](#)
- [Virtex-II Platform FPGAs: DC and Switching Characteristics \(Module 3\)](#)
- [Virtex-II Platform FPGAs: Pinout Information \(Module 4\)](#)

## Detailed Description

### Input/Output Blocks (IOBs)

Virtex-II™ I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in [Figure 1](#).

IOB blocks are designed for high performances I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.



DS031\_30\_101600

Figure 1: Virtex-II Input/Output Tile

Note: Differential I/Os must use the same clock.

### Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage ( $V_{CCINT} = 1.5V$ ), output driver supply voltage ( $V_{CCO}$ ) is dependent on the I/O standard (see [Table 1](#) and [Table 2](#)). An auxiliary supply voltage ( $V_{CCAUX} = 3.3V$ ) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see [DC Input and Output Levels](#) in Module 3.

All of the user IOBs have fixed-clamp diodes to  $V_{CCO}$  and to ground. As outputs, these IOBs are not compatible or compliant with 5V I/O standards. As inputs, these IOBs are not normally 5V tolerant, but can be used with 5V I/O standards when external current-limiting resistors are used. For more details, see the “5V Tolerant I/Os” Tech Topic at [www.xilinx.com](http://www.xilinx.com).

[Table 3](#) lists supported I/O standards with Digitally Controlled Impedance. See [Digitally Controlled Impedance \(DCI\)](#), page 8.

Table 1: Supported Single-Ended I/O Standards

IOSTANDARD Attribute	Output $V_{CCO}$	Input $V_{CCO}$	Input $V_{REF}$	Board Termination Voltage ( $V_{TT}$ )
LVTTTL	3.3	3.3	N/R <sup>(3)</sup>	N/R
LVCOS33	3.3	3.3	N/R	N/R
LVCOS25	2.5	2.5	N/R	N/R
LVCOS18	1.8	1.8	N/R	N/R
LVCOS15	1.5	1.5	N/R	N/R
PCI33_3	3.3	3.3	N/R	N/R
PCI66_3	3.3	3.3	N/R	N/R
PCI-X	3.3	3.3	N/R	N/R
GTL	Note (1)	Note (1)	0.8	1.2
GTL P	Note (1)	Note (1)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III_18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL18_I <sup>(2)</sup>	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL3_I	3.3	N/R	1.5	1.5
SSTL3_II	3.3	N/R	1.5	1.5
AGP-2X/AGP	3.3	N/R	1.32	N/R

#### Notes:

- $V_{CCO}$  of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. Example: If the pin High level is 1.5V, connect  $V_{CCO}$  to 1.5V.
- SSTL18\_I is not a JEDEC-supported standard.
- N/R = no requirement.

Table 2: Supported Differential Signal I/O Standards

I/O Standard	Output V <sub>CCO</sub>	Input V <sub>CCO</sub>	Input V <sub>REF</sub>	Output V <sub>OD</sub>
LVPECL_33	3.3	N/R <sup>(1)</sup>	N/R	0.490 - 1.220
LDT_25	2.5	N/R	N/R	0.500 - 0.700
LVDS_33	3.3	N/R	N/R	0.250 - 0.400
LVDS_25	2.5	N/R	N/R	0.250 - 0.400
LVDSEXT_33	3.3	N/R	N/R	0.440 - 0.820
LVDSEXT_25	2.5	N/R	N/R	0.440 - 0.820
BLVDS_25	2.5	N/R	N/R	0.250 - 0.450
ULVDS_25	2.5	N/R	N/R	0.500 - 0.700

**Notes:**

1. N/R = no requirement.

Table 3: Supported DCI I/O Standards

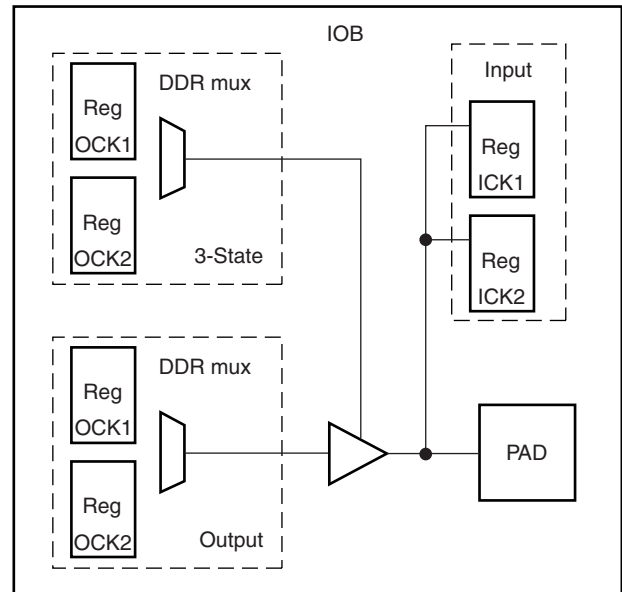
I/O Standard	Output V <sub>CCO</sub>	Input V <sub>CCO</sub>	Input V <sub>REF</sub>	Termination Type
LVDCI_33 <sup>(1)</sup>	3.3	3.3	N/R <sup>(4)</sup>	Series
LVDCI_DV2_33 <sup>(1)</sup>	3.3	3.3	N/R	Series
LVDCI_25 <sup>(1)</sup>	2.5	2.5	N/R	Series
LVDCI_DV2_25 <sup>(1)</sup>	2.5	2.5	N/R	Series
LVDCI_18 <sup>(1)</sup>	1.8	1.8	N/R	Series
LVDCI_DV2_18 <sup>(1)</sup>	1.8	1.8	N/R	Series
LVDCI_15 <sup>(1)</sup>	1.5	1.5	N/R	Series
LVDCI_DV2_15 <sup>(1)</sup>	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTL_P_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL18_I_DCI <sup>(3)</sup>	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split
SSTL2_I_DCI <sup>(2)</sup>	2.5	2.5	1.25	Split
SSTL2_II_DCI <sup>(2)</sup>	2.5	2.5	1.25	Split
SSTL3_I_DCI <sup>(2)</sup>	3.3	3.3	1.5	Split
SSTL3_II_DCI <sup>(2)</sup>	3.3	3.3	1.5	Split
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

**Notes:**

1. LVDCI\_XX and LVDCI\_DV2\_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18\_I is not a JEDEC-supported standard.
4. N/R = no requirement.

**Logic Resources**

IOB blocks include six storage elements, as shown in Figure 2.



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Figure 2: Virtex-II IOB Block

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 3. There are two input, output, and 3-state data signals, each being alternately clocked out.

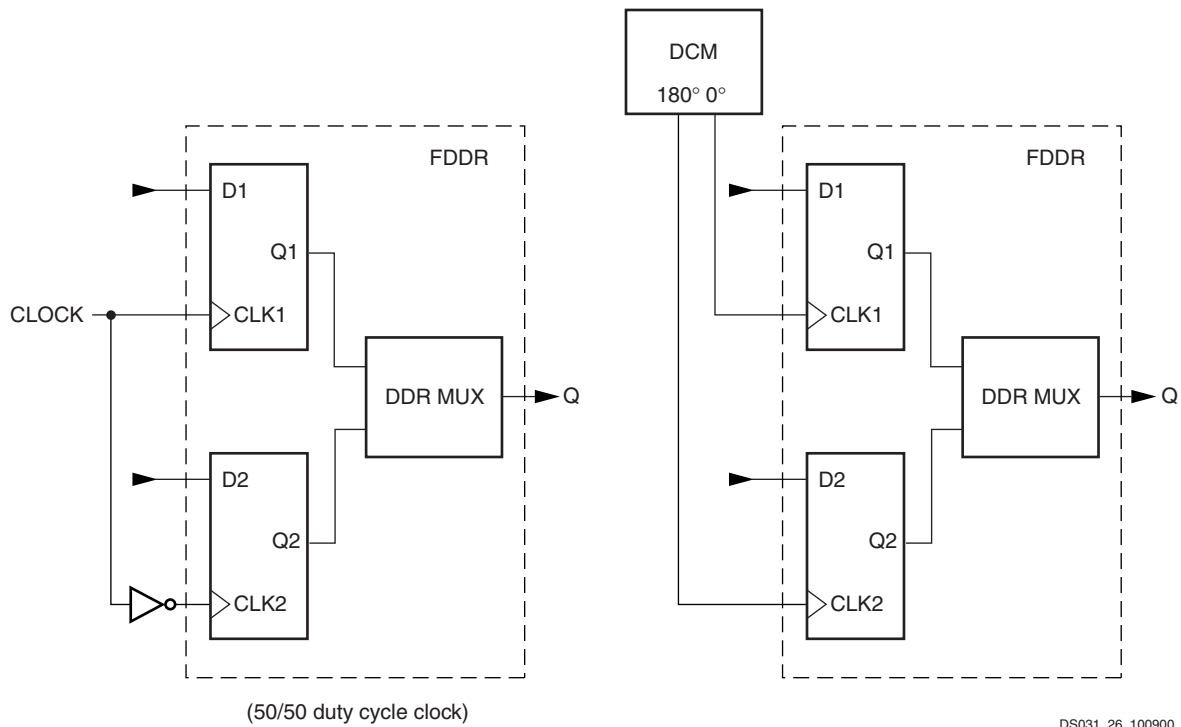


Figure 3: Double Data Rate Registers

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLow attribute. SRHIGH forces a logic “1”. SRLow forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLow attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLow, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.



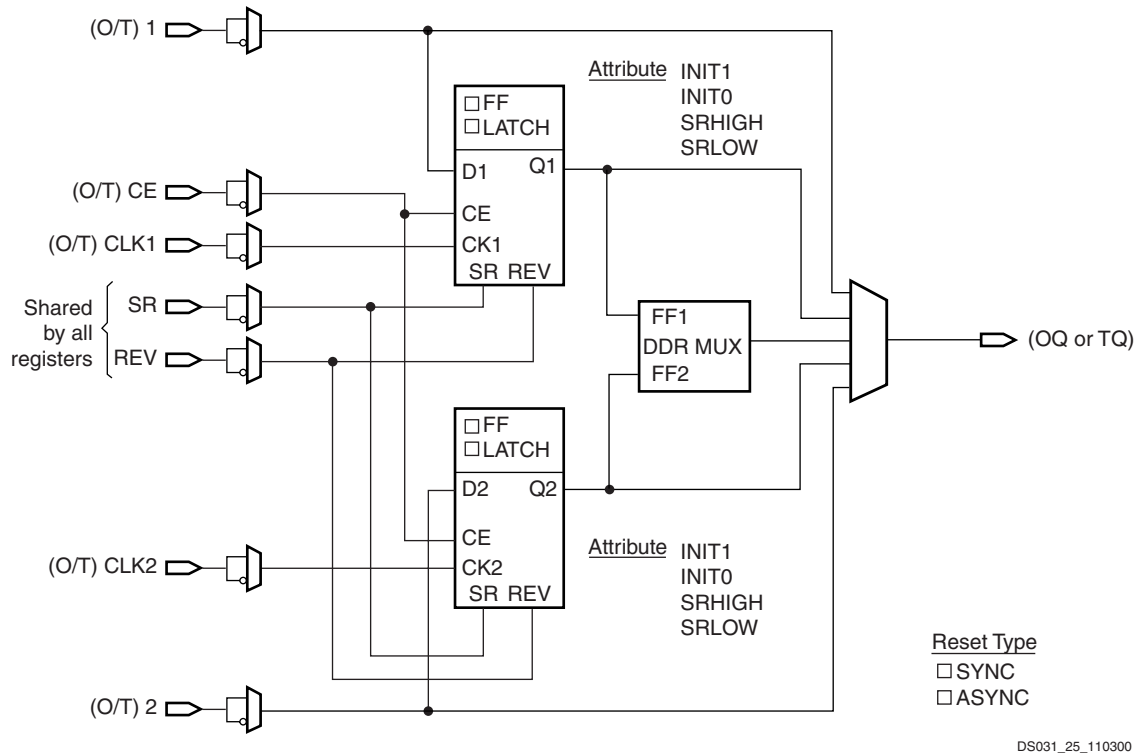


Figure 4: Register / Latch Configuration in an IOB Block

**Input/Output Individual Options**

Each device pad has optional pull-up and pull-down in all SelectI/O-Ultra configurations. Each device pad has optional weak-keeper in LVTTTL, LVCMOS, and PCI SelectI/O-Ultra configurations, as illustrated in Figure 5. Values of the optional pull-up and pull-down resistors are in the range 10 - 60 KΩ, which is the specification for V<sub>CCO</sub> when operating at 3.3V (from 3.0 to 3.6V only). The clamp diode is always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVTTTL sinks and sources current up to 24 mA. The current is programmable for LVTTTL and LVCMOS SelectI/O-Ultra standards (see Table 4). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI\_DV2 standards, drive strength and slew-rate controls are not available.

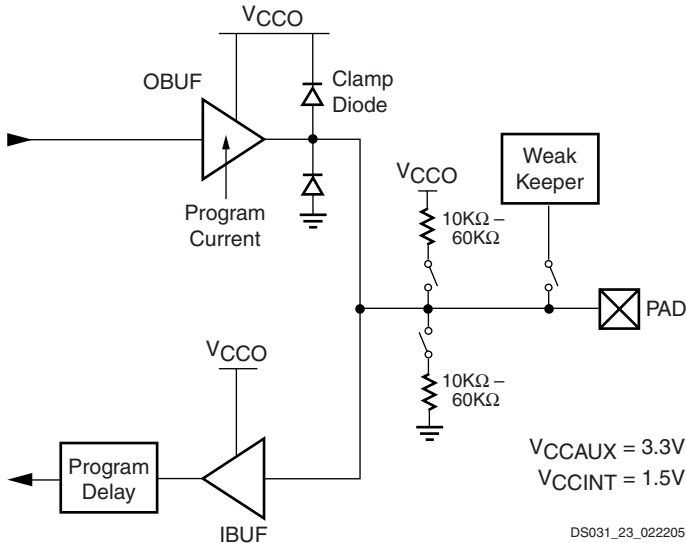


Figure 5: LVTTTL, LVCMOS or PCI SelectI/O-Ultra Standards

Table 4: LVTTTL and LVCMOS Programmable Currents (Sink and Source)

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

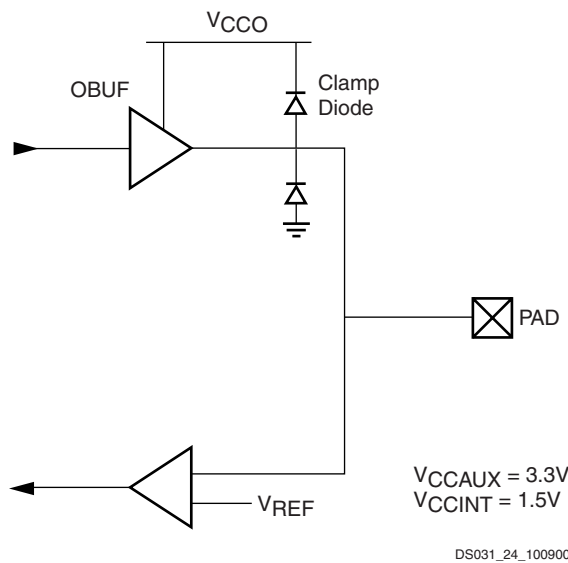


Figure 6: SSTL or HSTL SelectI/O-Ultra Standards

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP\_EN controls the pull-up resistors prior to configuration. By default, HSWAP\_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP\_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

### Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage,  $V_{REF}$ . The need to supply  $V_{REF}$  imposes constraints on which standards can be used in the same bank. See I/O banking description.

### Output Path

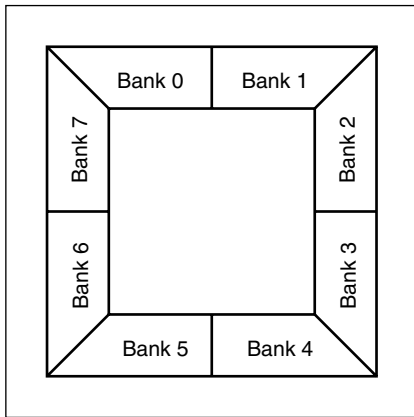
The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied  $V_{CCO}$  voltage. The need to supply  $V_{CCO}$  imposes constraints on which standards can be used in the same bank. See I/O banking description.

### I/O Banking

Some of the I/O standards described above require  $V_{CCO}$  and  $V_{REF}$  voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

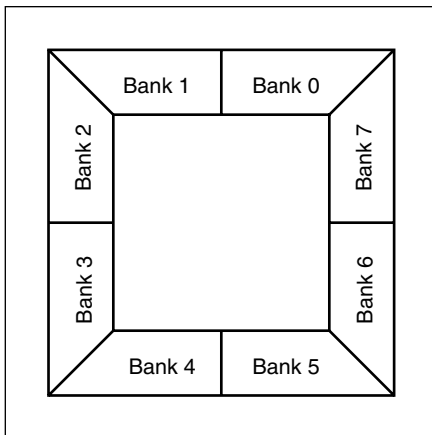
Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple  $V_{CCO}$  pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.



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Figure 7: Virtex-II I/O Banks: Top View for Wire-Bond Packages (CS/CSG, FG/FGG, & BG/BGG)

Some input standards require a user-supplied threshold voltage ( $V_{REF}$ ), and certain user-I/O pins are automatically configured as  $V_{REF}$  inputs. Approximately one in six of the I/O pins in the bank assume this role.



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Figure 8: Virtex-II I/O Banks: Top View for Flip-Chip Packages (FF & BF)

$V_{REF}$  pins within a bank are interconnected internally, and consequently only one  $V_{REF}$  voltage can be used within each bank. However, for correct operation, all  $V_{REF}$  pins in the bank must be connected to the external reference voltage source.

The  $V_{CCO}$  and the  $V_{REF}$  pins for each bank appear in the device pinout tables. Within a given package, the number of  $V_{REF}$  and  $V_{CCO}$  pins can vary depending on the size of device. In larger devices, more I/O pins convert to  $V_{REF}$  pins. Since these are always a superset of the  $V_{REF}$  pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All  $V_{REF}$  pins for the largest device anticipated must be connected to the  $V_{REF}$  voltage and not used for I/O. In smaller

devices, some  $V_{CCO}$  pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to  $V_{CCO}$  to permit migration to a larger device.

**Rules for Combining I/O Standards in the Same Bank**

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output  $V_{CCO}$  requirement can be combined in the same bank.

*Compatible example:*

SSTL2\_I and LVDS\_25\_DCI outputs

*Incompatible example:*

SSTL2\_I (output  $V_{CCO} = 2.5V$ ) and LVCMOS33 (output  $V_{CCO} = 3.3V$ ) outputs

2. **Combining input standards only.** Input standards with the same input  $V_{CCO}$  and input  $V_{REF}$  requirements can be combined in the same bank.

*Compatible example:*

LVCMOS15 and HSTL\_IV inputs

*Incompatible example:*

LVCMOS15 (input  $V_{CCO} = 1.5V$ ) and LVCMOS18 (input  $V_{CCO} = 1.8V$ ) inputs

*Incompatible example:*

HSTL\_I\_DCI\_18 ( $V_{REF} = 0.9V$ ) and HSTL\_IV\_DCI\_18 ( $V_{REF} = 1.1V$ ) inputs

3. **Combining input standards and output standards.** Input standards and output standards with the same input  $V_{CCO}$  and output  $V_{CCO}$  requirement can be combined in the same bank.

*Compatible example:*

LVDS\_25 output and HSTL\_I input

*Incompatible example:*

LVDS\_25 output (output  $V_{CCO} = 2.5V$ ) and HSTL\_I\_DCI\_18 input (input  $V_{CCO} = 1.8V$ )

4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.

5. **Additional rules for combining DCI I/O standards.**

- a. No more than one Single Termination type (input or output) is allowed in the same bank.

*Incompatible example:*

HSTL\_IV\_DCI input and HSTL\_III\_DCI input

- b. No more than one Split Termination type (input or output) is allowed in the same bank.

*Incompatible example:*

HSTL\_I\_DCI input and HSTL\_II\_DCI input

The implementation tools will enforce these design rules.

Table 5 summarizes all standards and voltage supplies.

**Table 5: Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V <sub>CCO</sub>		V <sub>REF</sub>	Termination Type	
	Output	Input	Input	Output	Input
LVDS_33	3.3	N/R	N/R <sup>(1)</sup>	N/R	N/R
LVDS_33			N/R	N/R	N/R
LVPECL_33			N/R	N/R	N/R
SSTL3_I			1.5	N/R	N/R
SSTL3_II			1.5	N/R	N/R
AGP			1.32	N/R	N/R
LVTTTL			N/R	N/R	N/R
LVCOS33		3.3	N/R	N/R	N/R
LVDCI_33			N/R	Series	N/R
LVDCI_DV2_33			N/R	Series	N/R
PCI33_3			N/R	N/R	N/R
PCI66_3			N/R	N/R	N/R
PCIX			N/R	N/R	N/R
SSTL3_I_DCI			1.5	N/R	Split
SSTL3_II_DCI	1.5	Split	Split		
LVDS_25	2.5	N/R	N/R	N/R	N/R
LVDS_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDS_25_DC I			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split

**Table 5: Summary of Voltage Supply Requirements for All Input and Output Standards (Continued)**

I/O Standard	V <sub>CCO</sub>		V <sub>REF</sub>	Termination Type			
	Output	Input	Input	Output	Input		
HSTL_III_18	1.8	N/R	1.1	N/R	N/R		
HSTL_IV_18			1.1	N/R	N/R		
HSTL_I_18			0.9	N/R	N/R		
HSTL_II_18			0.9	N/R	N/R		
SSTL18_I			0.9	N/R	N/R		
SSTL18_II			0.9	N/R	N/R		
LVCOS18			N/R	N/R	N/R		
LVDCI_18		1.8	N/R	Series	N/R		
LVDCI_DV2_18			N/R	Series	N/R		
HSTL_III_DCI_18			1.1	N/R	Single		
HSTL_IV_DCI_18			1.1	Single	Single		
HSTL_I_DCI_18			0.9	N/R	Split		
HSTL_II_DCI_18			0.9	Split	Split		
SSTL18_I_DCI			0.9	N/R	Split		
SSTL18_II_DCI	0.9	Split	Split				
HSTL_III	1.5	N/R	0.9	N/R	N/R		
HSTL_IV			0.9	N/R	N/R		
HSTL_I			0.75	N/R	N/R		
HSTL_II			0.75	N/R	N/R		
LVCOS15		1.5	N/R	N/R	N/R		
LVDCI_15			N/R	Series	N/R		
LVDCI_DV2_15			N/R	Series	N/R		
GTL_DCI			1	Single	Single		
HSTL_III_DCI			0.9	N/R	Single		
HSTL_IV_DCI			0.9	Single	Single		
HSTL_I_DCI			0.75	N/R	Split		
HSTL_II_DCI			0.75	Split	Split		
GTL_DCI			1.2	1.2	0.8	Single	Single
GTL			N/R	N/R	1	N/R	N/R
GTL	0.8	N/R			N/R		

**Notes:**

1. N/R = no requirement.



### Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 9.

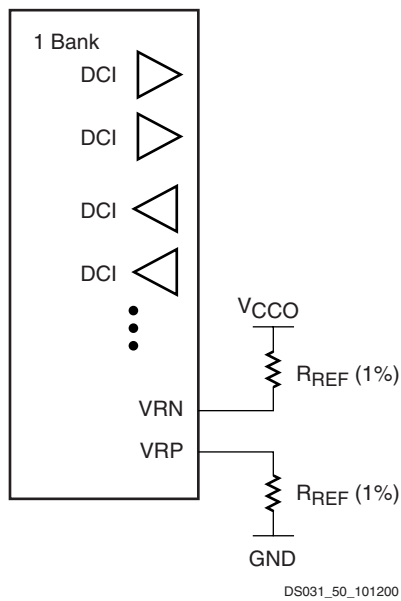


Figure 9: DCI in a Virtex-II Bank

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25Ω to 100Ω). For all series and parallel terminations listed in Table 6 and Table 7, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

### Controlled Impedance Drivers (Series Term.)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance ( $Z_0$ ). Virtex-II input buffers also support LVDCI and LVDCI\_DV2 I/O standards.

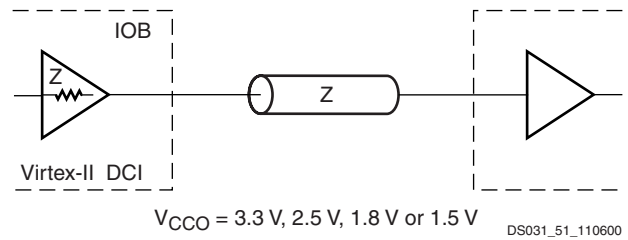


Figure 10: Internal Series Termination

Table 6: SelectI/O-Ultra Controlled Impedance Buffers

V <sub>CCO</sub>	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

### Controlled Impedance Drivers (Parallel)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 7 and Table 8 list the on-chip parallel terminations available in Virtex-II devices. V<sub>CCO</sub> must be set according to Table 3. Note that there is a V<sub>CCO</sub> requirement for GTL\_DCI and GTLP\_DCI, due to the on-chip termination resistor.

Table 7: SelectI/O-Ultra Buffers With On-Chip Parallel Termination

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI <sup>(1)</sup>
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI <sup>(1)</sup>
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI <sup>(1)</sup>
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI <sup>(1)</sup>
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

**Notes:**

1. SSTL-compatible

Table 8: SelectI/O-Ultra Differential Buffers With On-Chip Termination

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDS_EXT_25	LVDS_EXT_25_DCI

Figure 11 provides examples illustrating the use of the HSTL\_I\_DCI, HSTL\_II\_DCI, HSTL\_III\_DCI, and HSTL\_IV\_DCI I/O standards. For a complete list, see the [Virtex-II Platform FPGA User Guide](#).

	HSTL_I	HSTL_II	HSTL_III	HSTL_IV
Conventional				
DCI Transmit Conventional Receive				
Conventional Transmit DCI Receive				
DCI Transmit DCI Receive				
Bidirectional	N/A		N/A	
Reference Resistor	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$
Recommended $Z_0^{(1)}$	50 $\Omega$	50 $\Omega$	50 $\Omega$	50 $\Omega$

Note:  
1.  $Z_0$  is the recommended PCB trace impedance.

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Figure 11: HSTL DCI Usage Examples

Figure 12 provides examples illustrating the use of the SSTL2\_I\_DCI, SSTL2\_II\_DCI, SSTL3\_I\_DCI, and SSTL3\_II\_DCI I/O standards. For a complete list, see the [Virtex-II Platform FPGA User Guide](#).

	SSTL2_I	SSTL2_II	SSTL3_I	SSTL3_II
Conventional				
DCI Transmit Conventional Receive				
Conventional Transmit DCI Receive				
DCI Transmit DCI Receive				
Bidirectional	N/A		N/A	
Reference Resistor	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$
Recommended $Z_0^{(2)}$	50 Ω	50 Ω	50 Ω	50 Ω

Notes:

1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2.  $Z_0$  is the recommended PCB trace impedance.

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Figure 12: SSTL DCI Usage Examples

Figure 13 provides examples illustrating the use of the LVDS\_DCI and LVDS25\_DCI I/O standards. For a complete list, see the [Virtex-II Platform FPGA User Guide](#).

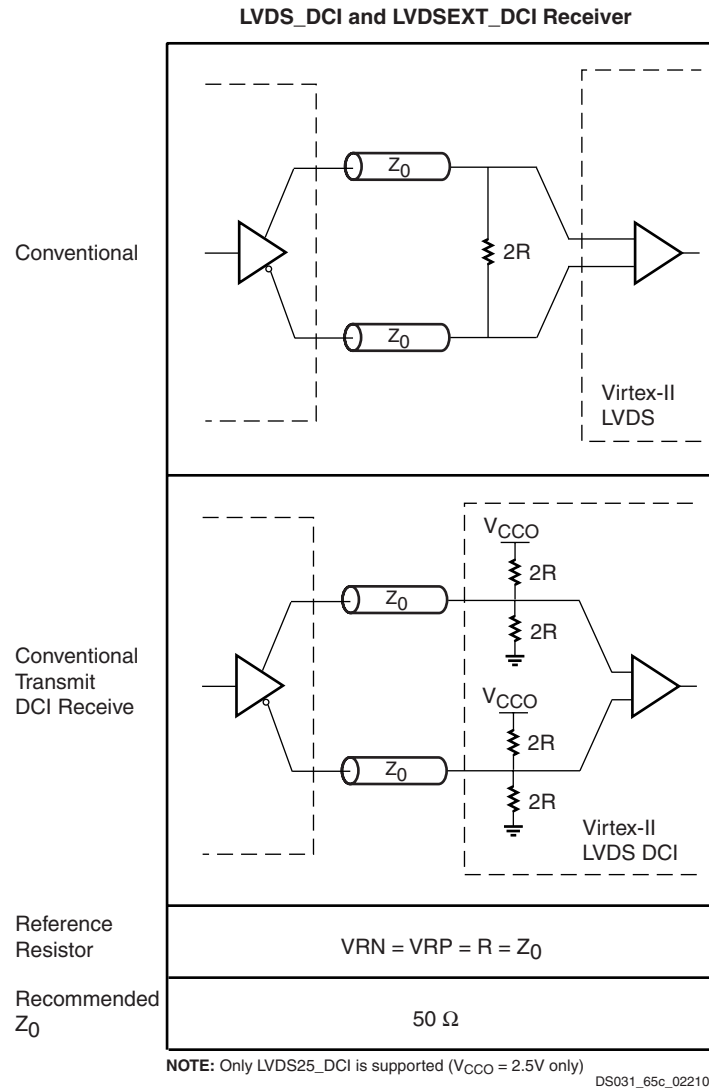


Figure 13: LVDS DCI Usage Examples



## Configurable Logic Blocks (CLBs)

The Virtex-II configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 14. A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

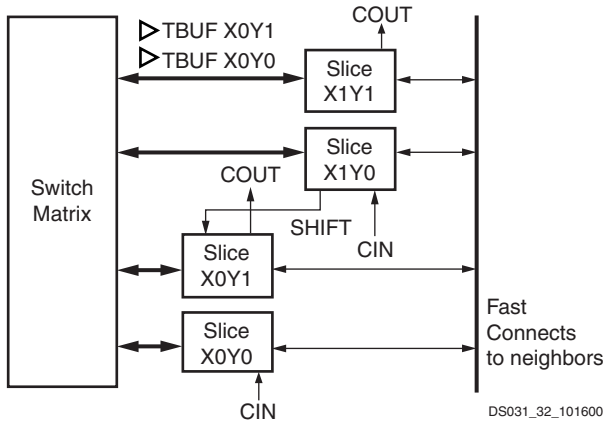


Figure 14: Virtex-II CLB Element

### Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 15, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM memory, or a 16-bit variable-tap shift register element.

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 16 shows a more detailed view of a single slice.

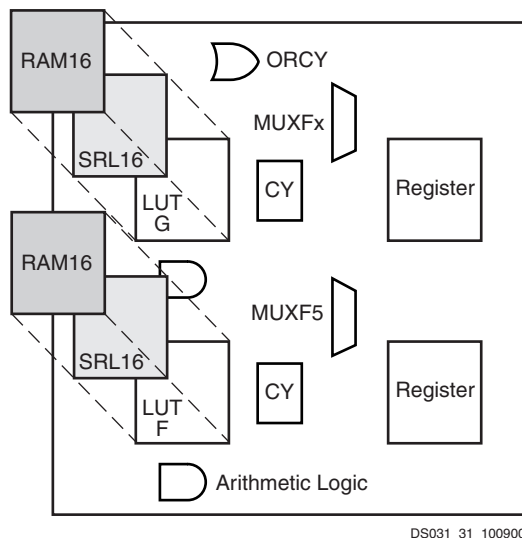


Figure 15: Virtex-II Slice Configuration

## Configurations

### Look-Up Table

Virtex-II function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in Figure 16).

In addition to the basic LUTs, the Virtex-II slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX are either MUXF6, MUXF7 or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexers to map any functions of six, seven, or eight inputs and selected wide logic functions.

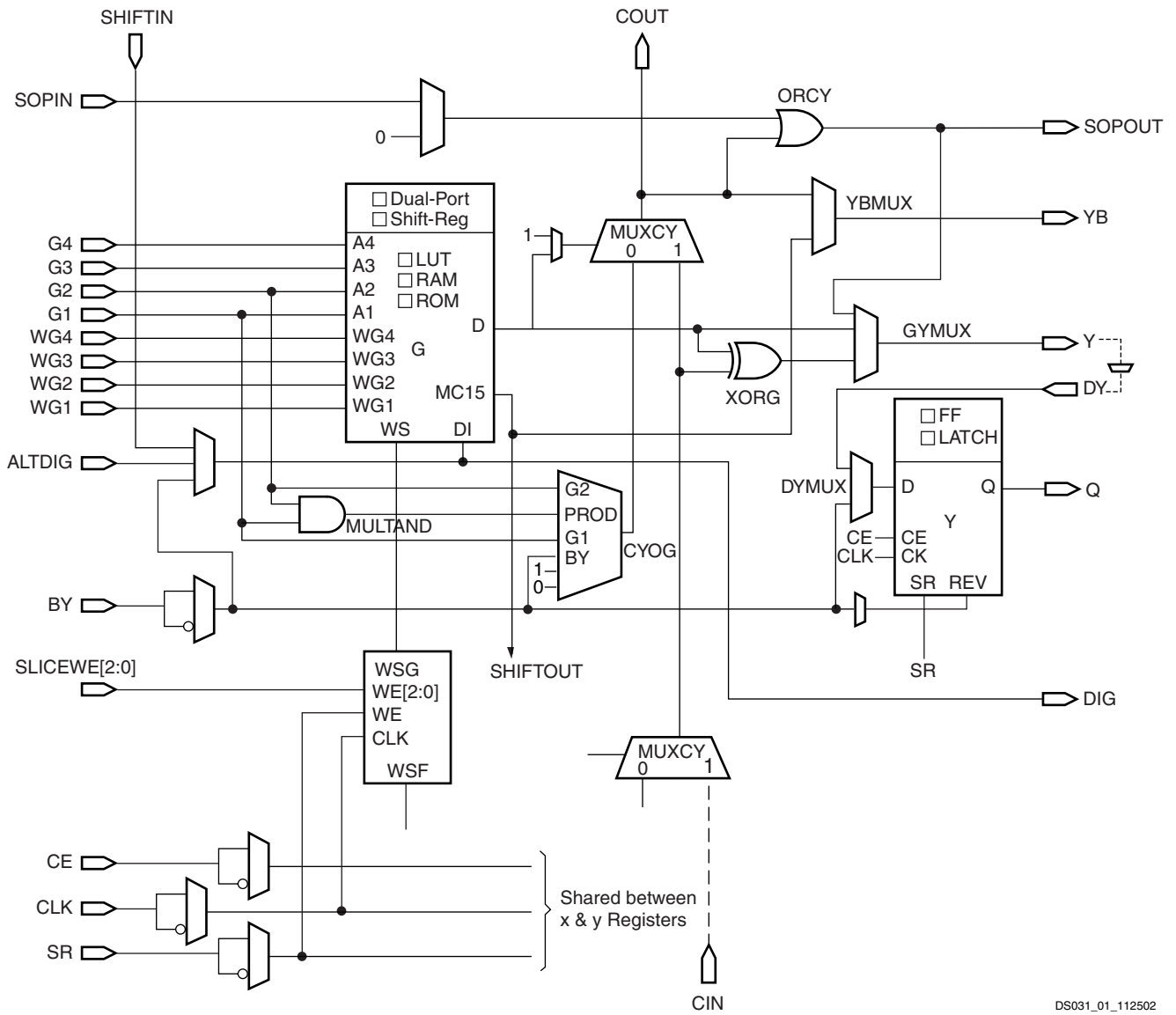
### Register/Latch

The storage elements in a Virtex-II slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic "1" when SR is asserted. SRLOW forces a logic "0". When SR is used, a second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition. (See Figure 17.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1. For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.

The control signals clock (CLK), clock enable (CE) and set/reset (SR) are common to both storage elements in one slice. All of the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.



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Figure 16: Virtex-II Slice (Top Half)

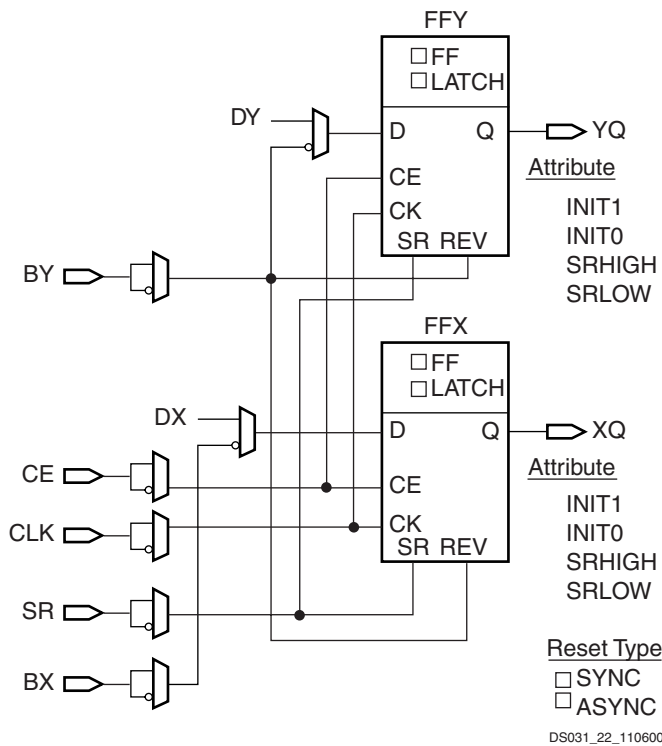


Figure 17: Register / Latch Configuration in a Slice

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

### Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM
- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 9 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 9: Distributed SelectRAM Configurations

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

#### Notes:

1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Figure 18, Figure 19, and Figure 20 illustrate various example configurations.

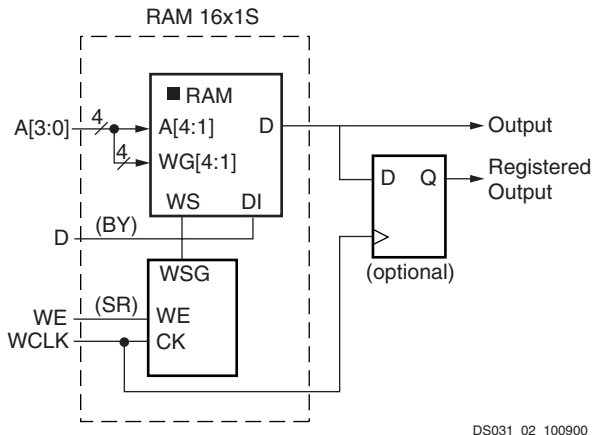


Figure 18: Distributed SelectRAM (RAM16x1S)

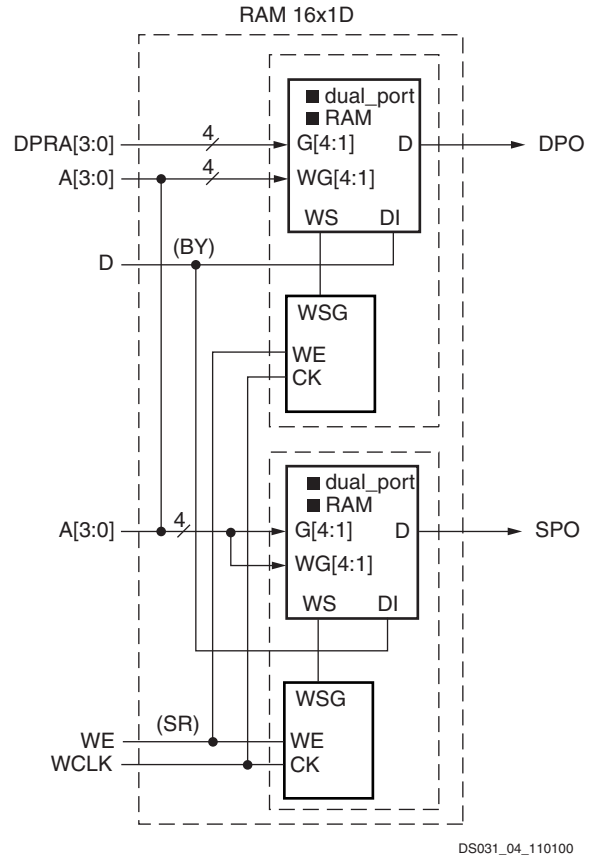


Figure 20: Dual-Port Distributed SelectRAM (RAM16x1D)

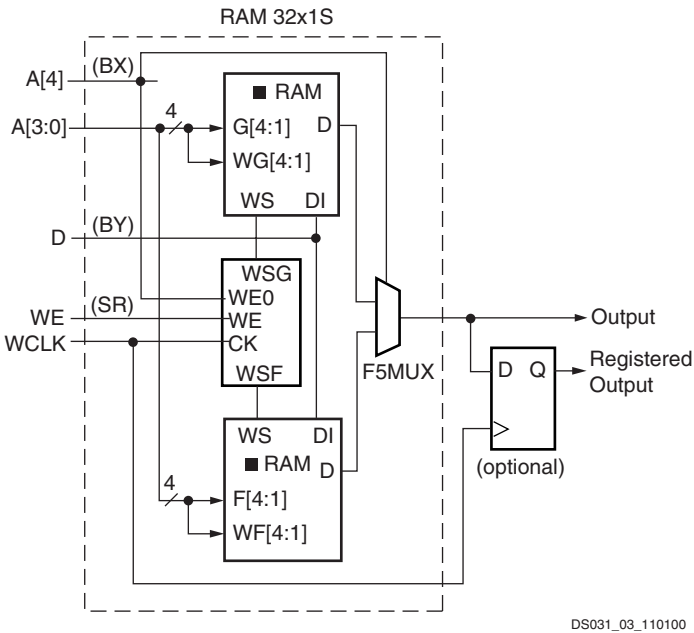


Figure 19: Single-Port Distributed SelectRAM (RAM32x1S)

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 10 shows the number of LUTs occupied by each configuration.

Table 10: ROM Configuration

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

### Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in **Figure 21**. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

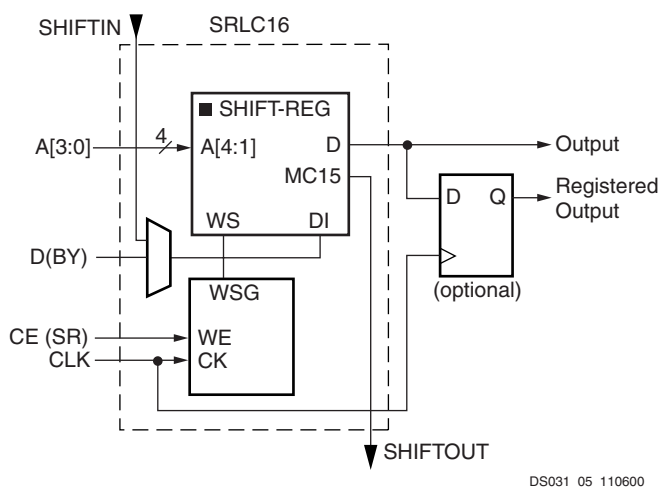


Figure 21: Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See **Figure 22**.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

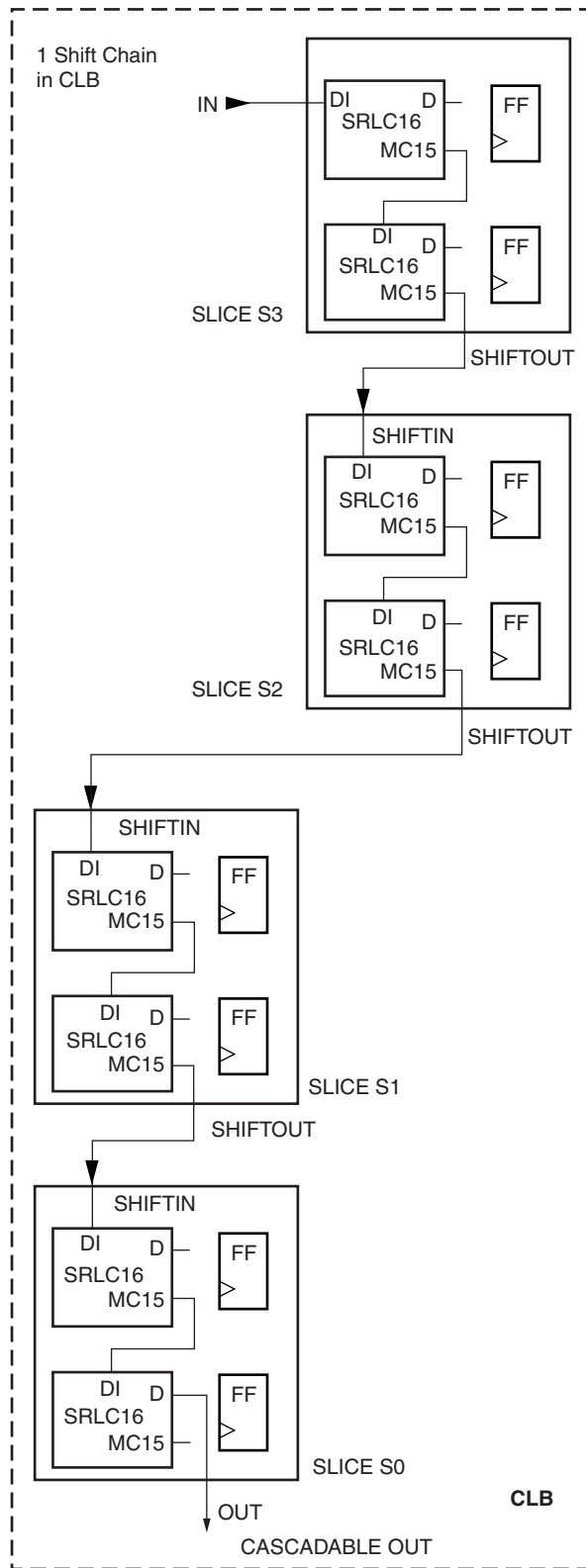


Figure 22: Cascadable Shift Register



**Multiplexers**

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in **Figure 23**. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

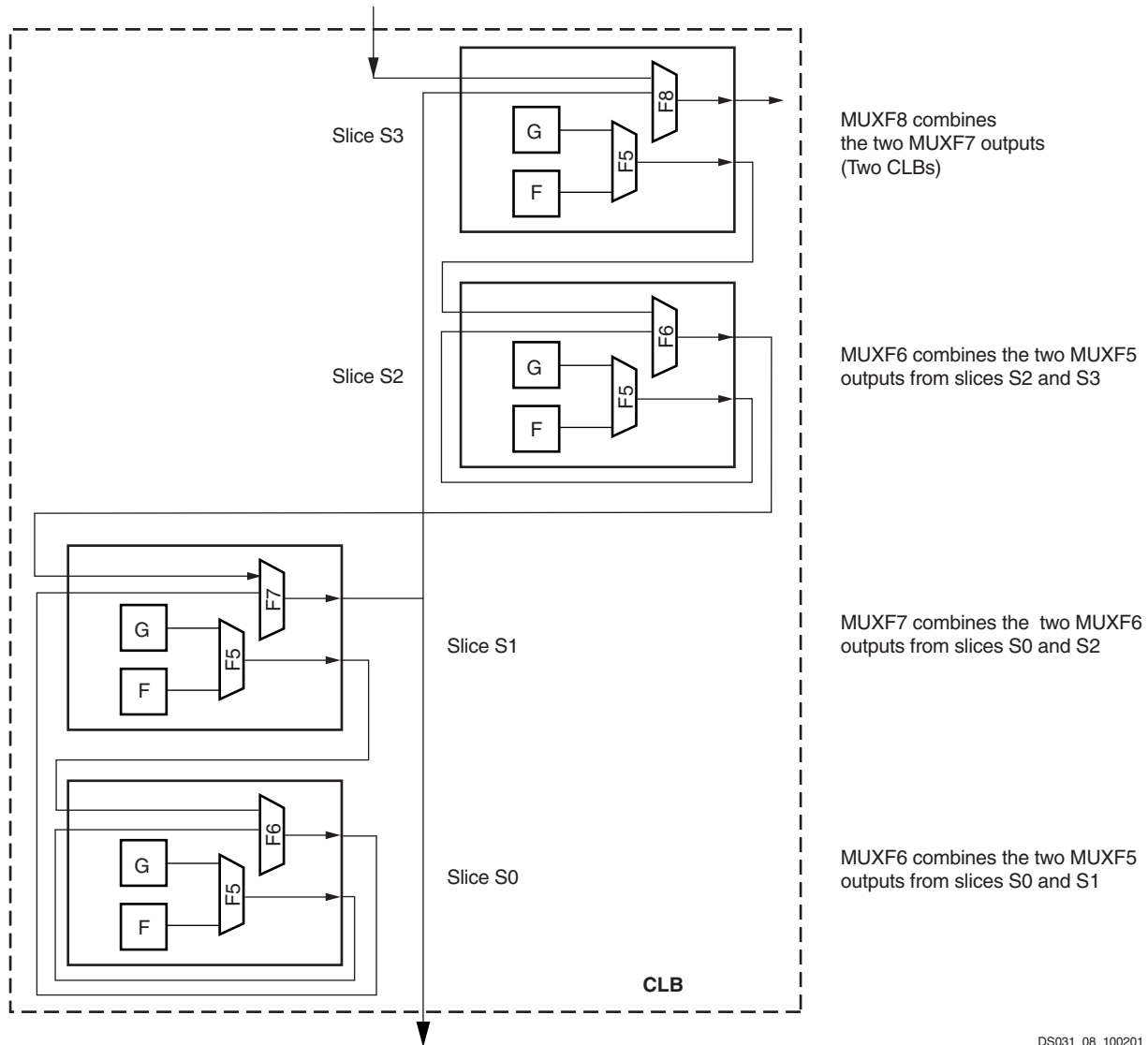


Figure 23: MUXF5 and MUXFX multiplexers

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**Fast Lookahead Carry Logic**

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the **Figure 24**.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also

be used to cascade function generators for implementing wide logic functions.

**Arithmetic Logic**

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT\_AND) gate (shown in **Figure 16**) improves the efficiency of multiplier implementation.