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Spartan-3A FPGA Family: Data Sheet

DS529 August 19, 2010

Product Specification

Module 1: Introduction and Ordering Information

DS529-1 (v2.0) August 19, 2010

- Introduction
- Features
- Architectural and Configuration Overview
- General I/O Capabilities
- Production Status
- Supported Packages and Package Marking
- Ordering Information

Module 2: Spartan-3A FPGA Family: Functional Description

DS529-2 (v2.0) August 19, 2010

The functionality of the Spartan®-3A FPGA family is described in the following documents.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Design Tools and IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
  - Configuration Pins and Behavior
  - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Platform Flash PROM
    - Master SPI Mode using Commodity Serial Flash
    - Master BPI Mode using Commodity Parallel Flash
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA
- UG334: *Spartan-3A/3AN FPGA Starter Kit User Guide*

Module 3: DC and Switching Characteristics

DS529-3 (v2.0) August 19, 2010

- DC Electrical Characteristics
  - Absolute Maximum Ratings
  - Supply Voltage Specifications
  - Recommended Operating Conditions
- Switching Characteristics
  - I/O Timing
  - Configurable Logic Block (CLB) Timing
  - Multiplier Timing
  - Block RAM Timing
  - Digital Clock Manager (DCM) Timing
  - Suspend Mode Timing
  - Device DNA Timing
  - Configuration and JTAG Timing

Module 4: Pinout Descriptions

DS529-4 (v2.0) August 19, 2010

- Pin Descriptions
- Package Overview
- Pinout Tables
- Footprint Diagrams

For more information on the Spartan-3A FPGA family, go to www.xilinx.com/spartan3a

Spartan-3A FPGA	Status
XC3S50A	Production
XC3S200A	Production
XC3S400A	Production
XC3S700A	Production
XC3S1400A	Production

Spartan-3A FPGA Family: Introduction and Ordering Information

DS529-1 (v2.0) August 19, 2010 **Product Specification**

Introduction

The Spartan®-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, I/O-intensive electronic applications. The five-member family offers densities ranging from 50,000 to 1.4 million system gates, as shown in Table 1.

The Spartan-3A FPGAs are part of the Extended Spartan-3A family, which also include the non-volatile Spartan-3AN and the higher density Spartan-3A DSP FPGAs. The Spartan-3A family builds on the success of the earlier Spartan-3E and Spartan-3 FPGA families. New features improve system performance and reduce the cost of configuration. These Spartan-3A family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3A FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3A family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs, and permit field design upgrades.

Features

- Very low cost, high-performance logic solution for high-volume, cost-conscious applications
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 502 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ± 10% compatibility and hot swap compliance
  - 640+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 400 Mb/s
  - Fully compliant 32-/64-bit, 33/66 MHz PCI® technology support
- Abundant, flexible logic resources
  - Densities up to 25,344 logic cells, including optional shift register or distributed RAM support
  - Efficient wide multiplexers, wide logic
  - Fast look-ahead carry logic
  - Enhanced 18 x 18 multipliers with optional pipeline
  - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
  - Up to 576 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 BPI parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
  - Unique Device DNA identifier for design authentication
  - Load multiple bitstreams under FPGA control
  - Post-configuration CRC checking
- Complete Xilinx ISE® and WebPACK™ development system software support plus Spartan-3A Starter Kit
- MicroBlaze™ and PicoBlaze™ embedded processors
- Low-cost QFP and BGA packaging, Pb-free options
  - Common footprints support easy density migration
  - Compatible with select Spartan-3AN nonvolatile FPGAs
  - Compatible with higher density Spartan-3A DSP FPGAs
- XA Automotive version available

Table 1: **Summary of Spartan-3A FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	CLBs	Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1,472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2,816	11,264	176K	576K	32	8	502	227

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

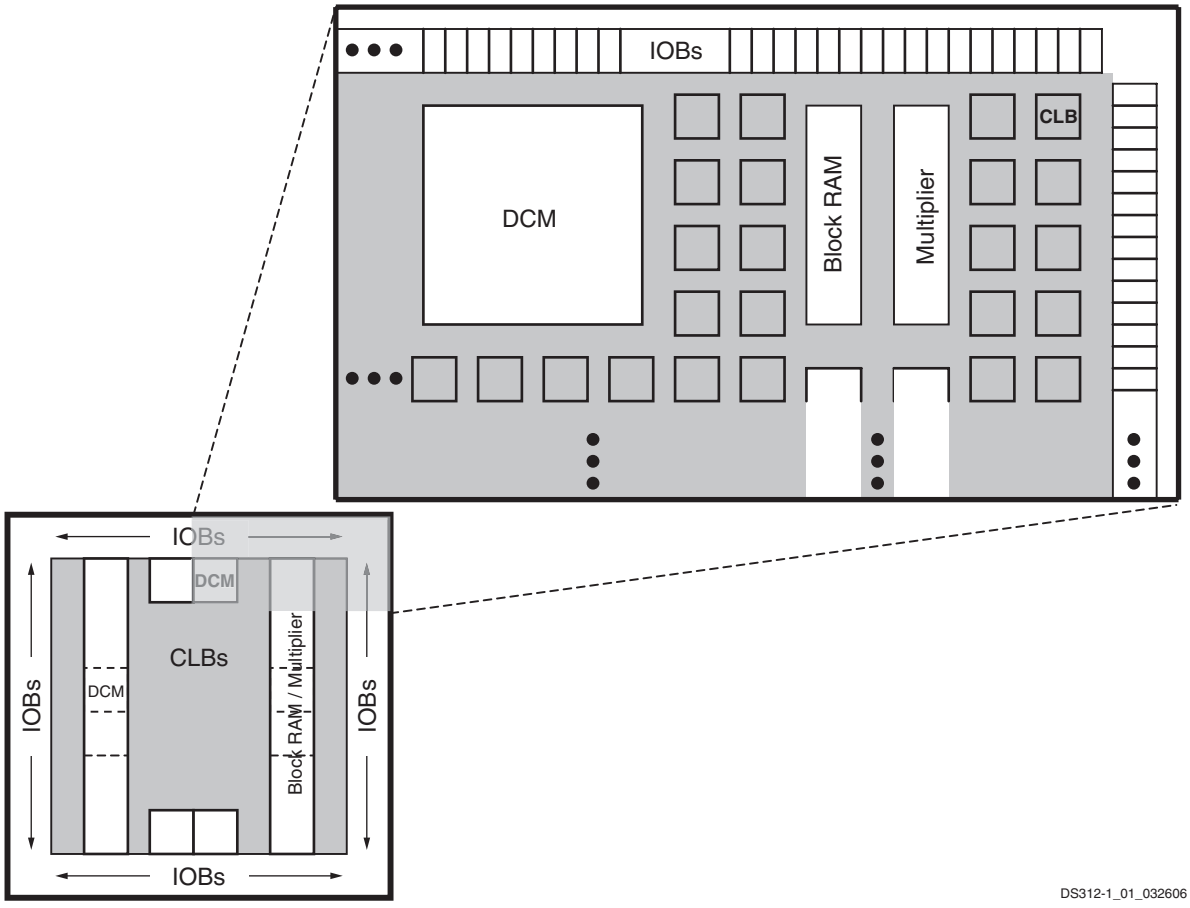
Architectural Overview

The Spartan-3A family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50A, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50A has DCMs only at the top, while the XC3S700A and XC3S1400A add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3A family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3S700A and XC3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50A has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: **Spartan-3A FPGA Architecture**

Configuration

Spartan-3A FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a BPI parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The Spartan-3A FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

Spartan-3A FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3A FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQ100 VQG100		TQ144 TQG144		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484		FG676 FGG676	
Body Size (mm)	14 x 14(2)		20 x 20(2)		17 x 17		19 x 19		21 x 21		23 x 23		27 x 27	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50A	**68** *(13)*	**60** *(24)*	**108** *(7)*	**50** *(24)*	**144** *(32)*	**64** *(32)*	-	-	-	-	-	-	-	-
XC3S200A	**68** *(13)*	**60** *(24)*	-	-	**195** *(35)*	**90** *(50)*	**248** *(56)*	**112** *(64)*	-	-	-	-	-	-
XC3S400A	-	-	-	-	**195** *(35)*	**90** *(50)*	**251** *(59)*	**112** *(64)*	**311** *(63)*	**142** *(78)*	-	-	-	-
XC3S700A	-	-	-	-	**161** *(13)*	**74** *(36)*	-	-	**311** *(63)*	**142** *(78)*	**372** *(84)*	**165** *(93)*	-	-
XC3S1400A	-	-	-	-	**161** *(13)*	**74** *(36)*	-	-	-	-	**375** *(87)*	**165** *(93)*	**502** *(94)*	**227** *(131)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.
2. The footprints for the VQ/TQ packages are larger than the package body. See the Package Drawings for details.

Production Status

Table 3 indicates the production status of each Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **Spartan-3A FPGA Production Status (Production Speed File)**

Temperature Range		Commercial (C)		Industrial
Speed Grade		Standard (–4)	High-Performance (–5)	Standard (–4)
Part Number	XC3S50A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S200A	**Production** (v1.35)	**Production** (v1.35)	**Production** (v1.35)
	XC3S400A	**Production** (v1.36)	**Production** (v1.36)	**Production** (v1.36)
	XC3S700A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)
	XC3S1400A	**Production** (v1.34)	**Production** (v1.35)	**Production** (v1.34)

Package Marking

Figure 2 provides a top marking example for Spartan-3A FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

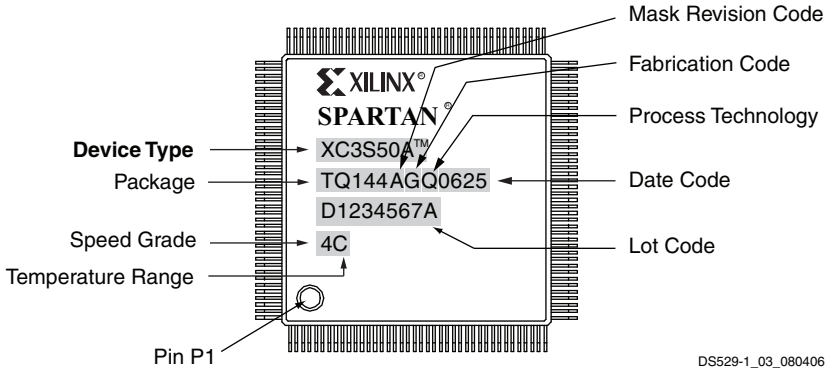


Figure 2: **Spartan-3A QFP Package Marking Example**

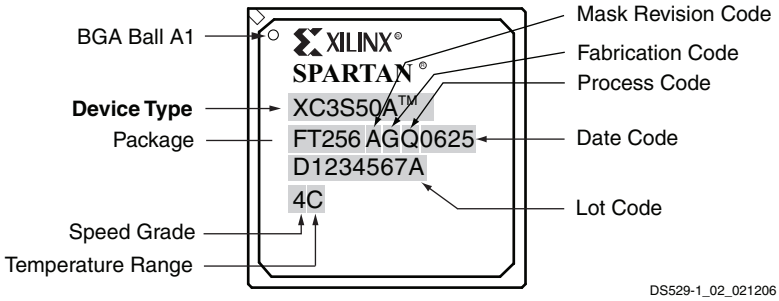
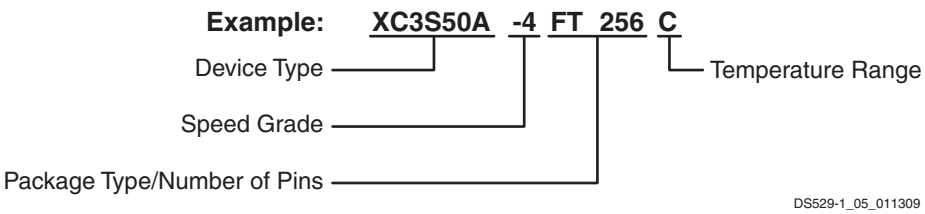


Figure 3: **Spartan-3A BGA Package Marking Example**

Ordering Information

Spartan-3A FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a ‘G’ character in the ordering code.



Device	Speed Grade		Package Type / Number of Pins[1]		Temperature Range (T_J)	
XC3S50A	–4	Standard Performance	VQ100/ VQG100	100-pin Very Thin Quad Flat Pack (VQFP)	C	Commercial (0°C to 85°C)
XC3S200A	–5	High Performance (Commercial only)	TQ144/ TQG144	144-pin Thin Quad Flat Pack (TQFP)	I	Industrial (–40°C to 100°C)
XC3S400A			FT256/ FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)		
XC3S700A			FG320/ FGG320	320-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S1400A			FG400/ FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)		
			FG484/ FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)		
			FG676 FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)		

Notes:

1. See Table 2 for specific device/package combinations.
2. See DS681 for the XA Automotive Spartan-3A FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status. Updated maximum differential I/O count for XC3S50A in Table 1. Updated differential input-only pin counts in Table 2.
03/16/07	1.2	Minor formatting updates.
04/23/07	1.3	Added "Production Status" section.
05/08/07	1.4	Updated XC3S400A to Production.
07/10/07	1.4.1	Minor updates.
04/15/08	1.6	Added VQ100 for XC3S50A and XC3S200A and extended FT256 to XC3S700A and XC3S1400A Added reference to SCD 4103 for 750 Mbps performance.
05/28/08	1.7	Added reference to XA Automotive version.
03/06/09	1.8	Simplified Ordering Information. Added references to Extended Spartan-3A Family. Removed reference to SCD 4103.
08/19/10	2.0	Updated Table 2 to clarify TQ/VQ size.

Spartan-3A FPGA Design Documentation

The functionality of the Spartan®-3A FPGA Family is described in the following documents. The topics covered in each guide is listed below.

- **DS706: Extended Spartan-3A Family Overview**
  www.xilinx.com/support/documentation/data_sheets/ds706.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA

For application examples, see the Spartan-3A FPGA application notes.

- **Spartan-3A FPGA Application Notes**
  www.xilinx.com/support/documentation/spartan-3a_application_notes.htm

For specific hardware examples, please see the Spartan-3A FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3A/3AN FPGA Starter Kit Board Page**
  www.xilinx.com/s3astarter
- **UG334: Spartan-3A/3AN FPGA Starter Kit User Guide**
  www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf

For information on the XA Automotive version of the Spartan-3A family, see the following data sheet.

- XA Spartan-3A Automotive FPGA Family Data Sheet
  www.xilinx.com/support/documentation/data_sheets/ds681.pdf

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

- Sign Up for Alerts
  www.xilinx.com/support/answers/18683.htm

Related Product Families

The Spartan-3AN nonvolatile FPGA family is architecturally identical to the Spartan-3A FPGA family, except that it has in-system flash memory and is offered in select pin-compatible package options.

- **DS557: Spartan-3AN Family Data Sheet**
  www.xilinx.com/support/documentation/data_sheets/ds557.pdf

The compatible Spartan-3A DSP FPGA family replaces the 18-bit multiplier with the DSP48A block, while also increasing the block RAM capability and quantity. The two members of the Spartan-3A DSP FPGA family extend the Spartan-3A density range up to 37,440 and 53,712 logic cells.

- **DS610: Spartan-3A DSP FPGA Family Data Sheet**
  www.xilinx.com/support/documentation/data_sheets/ds610.pdf
- **UG431: XtremeDSP DSP48A for Spartan-3A DSP FPGAs**
  www.xilinx.com/support/documentation/user_guides/ug431.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/05/06	1.0	Initial release.
02/02/07	1.1	Promoted to Preliminary status.
03/16/07	1.2	Added cross-reference to nonvolatile Spartan-3AN FPGA family.
04/23/07	1.3	Added cross-reference to compatible Spartan-3A DSP family.
07/10/07	1.4	Updated Starter Kit reference to new UG334.
04/15/08	1.6	Updated trademarks.
05/28/08	1.7	Added reference to XA Automotive version.
03/06/09	1.8	Added link to DS706 on Extended Spartan-3A family.
08/19/10	2.0	Updated link to sign up for Alerts.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Power Supply Specifications

Table 5: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	1.0	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	1.0	2.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see UG331 chapter "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: **Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

General Recommended Operating Conditions

Table 8: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage(2)	V_{CCAUX} = 2.5		2.25	2.50	2.75	V
		V_{CCAUX} = 3.3		3.00	3.30	3.60	V
V_{IN}	Input voltage(3)	PCI IOSTANDARD		–0.5	–	V_{CCO}+0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_#(4)	–0.5	–	4.10	V
T_{IN}	Input signal transition time(5)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 11 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 13 lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See XAPP459, “Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins.”
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

General DC Characteristics for I/O Pins

Table 9: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**(1)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L(2)	Leakage current at User I/O, input-only, dual-purpose, and dedicated pins, FPGA powered	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested		–10	–	+10	µA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		–10	–	+10	µA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add I_{HS} + I_{RPU}			µA
I_{RPU}(3)	Current through pull-up resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = GND	V_{CCO} or V_{CCAUX} = 3.0V to 3.6V	–151	–315	–710	µA
			V_{CCO} or V_{CCAUX} = 2.3V to 2.7V	–82	–182	–437	µA
			V_{CCO} = 1.7V to 1.9V	–36	–88	–226	µA
			V_{CCO} = 1.4V to 1.6V	–22	–56	–148	µA
			V_{CCO} = 1.14V to 1.26V	–11	–31	–83	µA
R_{PU}(3)	Equivalent pull-up resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPU} per Note 3)	V_{IN} = GND	V_{CCO} = 3.0V to 3.6V	5.1	11.4	23.9	kΩ
			V_{CCO} = 2.3V to 2.7V	6.2	14.8	33.1	kΩ
			V_{CCO} = 1.7V to 1.9V	8.4	21.6	52.6	kΩ
			V_{CCO} = 1.4V to 1.6V	10.8	28.4	74.0	kΩ
			V_{CCO} = 1.14V to 1.26V	15.3	41.1	119.4	kΩ
I_{RPD}(3)	Current through pull-down resistor at User I/O, dual-purpose, input-only, and dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = V_{CCO}	V_{CCAUX} = 3.0V to 3.6V	167	346	659	µA
			V_{CCAUX} = 2.25V to 2.75V	100	225	457	µA
R_{PD}(3)	Equivalent pull-down resistor value at User I/O, dual-purpose, input-only, and dedicated pins (based on I_{RPD} per Note 3)	V_{CCAUX} = 3.0V to 3.6V	V_{IN} = 3.0V to 3.6V	5.5	10.4	20.8	kΩ
			V_{IN} = 2.3V to 2.7V	4.1	7.8	15.7	kΩ
			V_{IN} = 1.7V to 1.9V	3.0	5.7	11.1	kΩ
			V_{IN} = 1.4V to 1.6V	2.7	5.1	9.6	kΩ
			V_{IN} = 1.14V to 1.26V	2.4	4.5	8.1	kΩ
		V_{CCAUX} = 2.25V to 2.75V	V_{IN} = 3.0V to 3.6V	7.9	16.0	35.0	kΩ
			V_{IN} = 2.3V to 2.7V	5.9	12.0	26.3	kΩ
			V_{IN} = 1.7V to 1.9V	4.2	8.5	18.6	kΩ
			V_{IN} = 1.4V to 1.6V	3.6	7.2	15.7	kΩ
			V_{IN} = 1.14V to 1.26V	3.0	6.0	12.5	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		–10	–	+10	µA
C_{IN}	Input capacitance	–		–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{CCO} = 3.3V ± 10%	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		V_{CCO} = 2.5V ± 10%	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See "Parasitic Leakage" in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO} / I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	Commercial Maximum(2)	Industrial Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50A	2	20	30	mA
		XC3S200A	7	50	70	mA
		XC3S400A	10	85	125	mA
		XC3S700A	13	120	185	mA
		XC3S1400A	24	220	310	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50A	0.2	2	3	mA
		XC3S200A	0.2	2	3	mA
		XC3S400A	0.3	3	4	mA
		XC3S700A	0.3	3	4	mA
		XC3S1400A	0.3	3	4	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50A	3	8	10	mA
		XC3S200A	5	12	15	mA
		XC3S400A	5	18	24	mA
		XC3S700A	6	28	34	mA
		XC3S1400A	10	50	58	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. For more accurate estimates for a specific design, use the Xilinx XPower tools. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Single-Ended I/O Standards

Table 11: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.6				0.8	2.0
LVCMOS25(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3(6)	3.0	3.3	3.6				0.3 • V_{CCO}	0.5 • V_{CCO}
PCI66_3(6)	3.0	3.3	3.6				0.3 • V_{CCO}	0.5 • V_{CCO}
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III	1.4	1.5	1.6	–	0.9	-	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	V_{REF} – 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38	V_{REF} – 0.150	V_{REF} + 0.150
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38	V_{REF} – 0.150	V_{REF} + 0.150
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	V_{REF} – 0.2	V_{REF} + 0.2
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	V_{REF} – 0.2	V_{REF} + 0.2

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs when V_{CCAUX} = 3.3V range and for PCI I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 8.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS25 or LVCMOS33 standard depending on V_{CCAUX}. The dual-purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24(4)	24	–24		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16(4)	16	–16		
	24(4)	24	–24		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12(4)	12	–12		
	16(4)	16	–16		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8(4)	8	–8		
	12(4)	12	–12		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4(4)	4	–4		
	6(4)	6	–6		

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards *(Continued)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
PCI33_3(5)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(5)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I(4)	8	–8	0.4	V_{CCO} - 0.4
HSTL_III(4)	24	–8	0.4	V_{CCO} - 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} - 0.4
HSTL_II_18(4)	16	–16	0.4	V_{CCO} - 0.4
HSTL_III_18	24	–8	0.4	V_{CCO} - 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(4)	13.4	–13.4	V_{TT} – 0.603	V_{TT} + 0.603
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(4)	16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 11.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} — the output current condition under which V_{OL} is tested
   I_{OH} — the output current condition under which V_{OH} is tested
   V_{OL} — the output voltage that indicates a Low logic level
   V_{OH} — the output voltage that indicates a High logic level
   V_{CCO} — the supply voltage for output drivers
   V_{TT} — the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for the Fast, Slow, and QUIETIO slew attributes.
4. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
5. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Differential I/O Standards

Differential Input Pairs

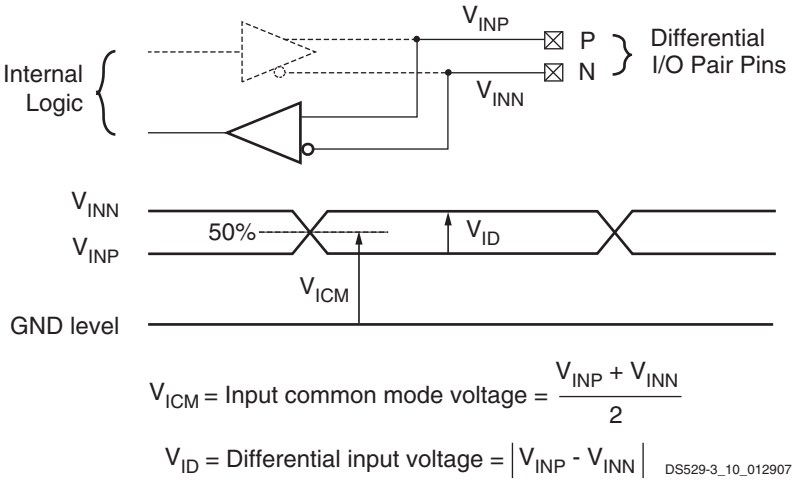


Figure 4: **Differential Input Voltages**

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(1)			V_{ID}			V_{ICM}(2)		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25(3)	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33(3)	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25(4)	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25(3)	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33(3)	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25(5)	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33(5)	Inputs Only			100	800	1000	0.3	1.2	2.8(6)
RSDS_25(3)	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33(3)	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33(3, 4, 7)	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25(3)	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33(3)	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18(8)	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II(8)	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II(8)	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O," page 20.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX}=3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID} / 2)$
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \leq V_{ICM} \leq (V_{CCAUX} - 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have V_{CCAUX} at either 2.5V or 3.3V. Define your V_{CCAUX} level using the CONFIG VCCAUX constraint.

Differential Output Pairs

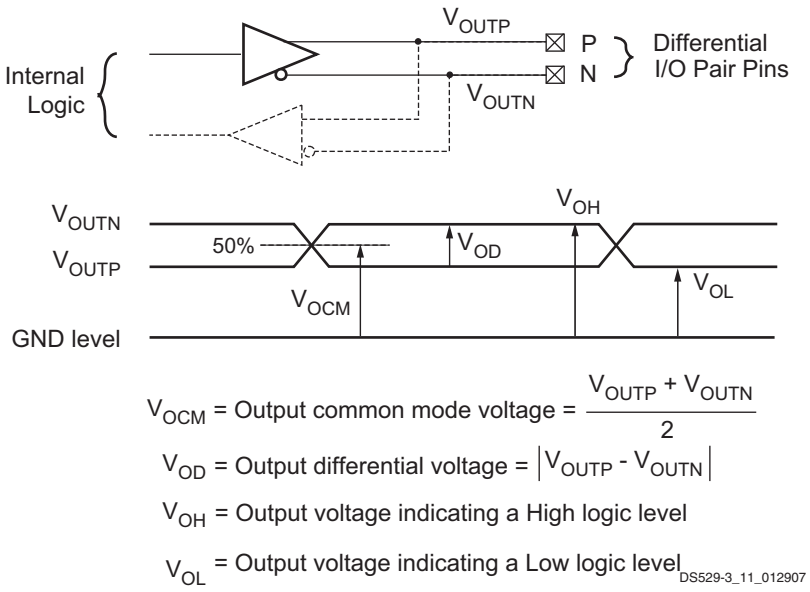


Figure 5: **Differential Output Voltages**

Table 14: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.603	V_{TT} – 0.603
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
2. See "External Termination Requirements for Differential I/O," page 20.
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

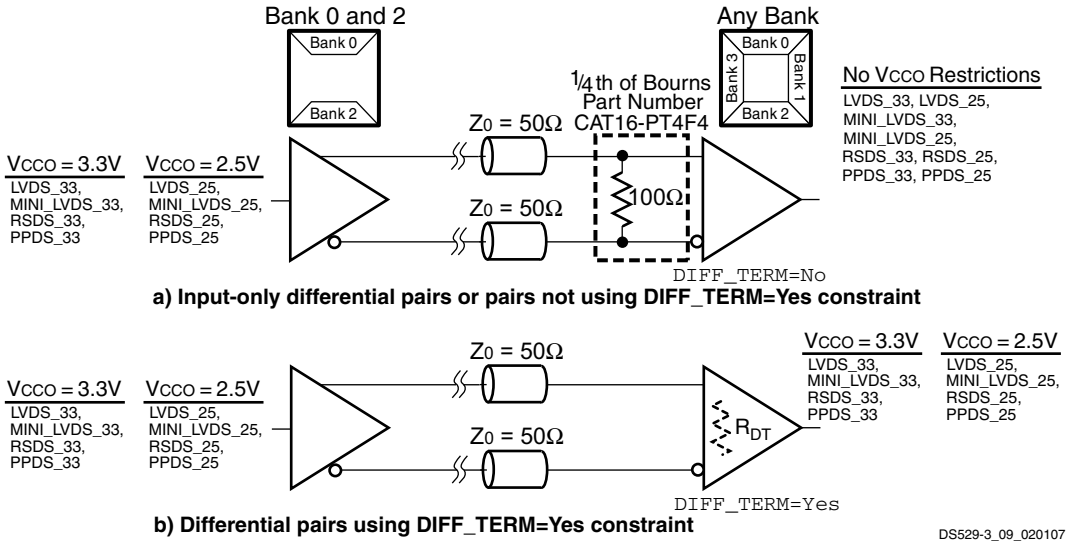


Figure 6: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

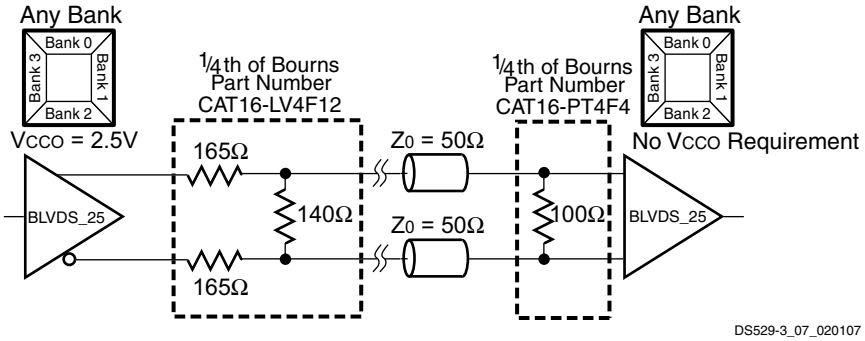


Figure 7: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

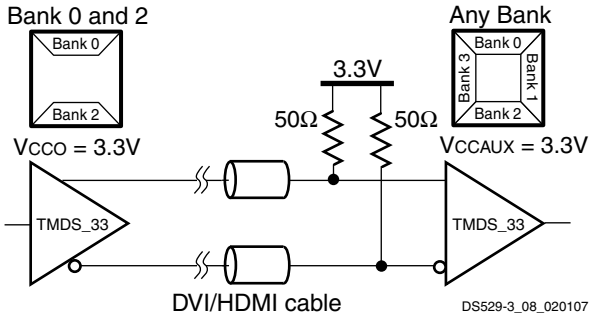


Figure 8: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Read Endurance

Table 15: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All Spartan-3A FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 16. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGA designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A FPGA speed files (v1.41), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 16. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 16: **Spartan-3A v1.41 Speed Grade Designation**

Device	Advance	Preliminary	Production
XC3S50A			-4, -5
XC3S200A			-4, -5
XC3S400A			-4, -5
XC3S700A			-4, -5
XC3S1400A			-4, -5

Table 17 provides the recent history of the Spartan-3A FPGA speed files.

Table 17: **Spartan-3A Speed File Version History**

Version	ISE Release	Description
1.41	ISE 10.1.03	Updated Automotive output delays
1.40	ISE 10.1.02	Updated Automotive input delays.
1.39	ISE 10.1.01	Added Automotive parts.
1.38	ISE 9.2.03i	Added Absolute Minimum values.
1.37	ISE 9.2.01i	Updated pin-to-pin setup and hold times (Table 19), TMDS output adjustment (Table 26) multiplier setup/hold times (Table 34), and block RAM clock width (Table 35).
1.36	ISE 9.2i; previously available via Answer Record AR24992	XC3S400A, all speed grades and all temperature grades, upgraded to Production
1.35	Answer Record AR24992	XC3S50A, XC3S200A, XC3S700A, XC3S1400A, all speed grades and all temperature grades, upgraded to Production.
1.34	ISE 9.1.03i	XC3S700A and XC3S1400A -4 speed grade upgraded to Production. Updated pin-to-pin timing numbers.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 18: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	XC3S50A	3.18	3.42	ns
			XC3S200A	3.21	3.27	ns
			XC3S400A	2.97	3.33	ns
			XC3S700A	3.39	3.50	ns
			XC3S1400A	3.51	3.99	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	XC3S50A	4.59	5.02	ns
			XC3S200A	4.88	5.24	ns
			XC3S400A	4.68	5.12	ns
			XC3S700A	4.97	5.34	ns
			XC3S1400A	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 23. If the latter is true, *add* the appropriate Output adjustment from Table 26.
3. DCM output jitter is included in all measurements.

Pin-to-Pin Setup and Hold Times

Table 19: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50A	2.45	2.68	ns
			XC3S200A	2.59	2.84	ns
			XC3S400A	2.38	2.68	ns
			XC3S700A	2.38	2.57	ns
			XC3S1400A	1.91	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	XC3S50A	2.55	2.76	ns
			XC3S200A	2.32	2.76	ns
			XC3S400A	2.21	2.60	ns
			XC3S700A	2.28	2.63	ns
			XC3S1400A	2.33	2.41	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50A	-0.36	-0.36	ns
			XC3S200A	-0.52	-0.52	ns
			XC3S400A	-0.33	-0.29	ns
			XC3S700A	-0.17	-0.12	ns
			XC3S1400A	-0.07	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	XC3S50A	-0.63	-0.58	ns
			XC3S200A	-0.56	-0.56	ns
			XC3S400A	-0.42	-0.42	ns
			XC3S700A	-0.80	-0.75	ns
			XC3S1400A	-0.69	-0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 23. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 23. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 20: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2)	0	XC3S50A	1.56	1.58	ns
				XC3S200A	1.71	1.81	ns
				XC3S400A	1.30	1.51	ns
				XC3S700A	1.34	1.51	ns
				XC3S1400A	1.36	1.74	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XC3S50A	2.16	2.18	ns
			2		3.10	3.12	ns
			3		3.51	3.76	ns
			4		4.04	4.32	ns
			5		3.88	4.24	ns
			6		4.72	5.09	ns
			7		5.47	5.94	ns
			8		5.97	6.52	ns
			1	XC3S200A	2.05	2.20	ns
			2		2.72	2.93	ns
			3		3.38	3.78	ns
			4		3.88	4.37	ns
			5		3.69	4.20	ns
			6		4.56	5.23	ns
			7		5.34	6.11	ns
			8		5.85	6.71	ns
			1	XC3S400A	1.79	2.02	ns
			2		2.43	2.67	ns
			3		3.02	3.43	ns
			4		3.49	3.96	ns
			5		3.41	3.95	ns
			6		4.20	4.81	ns
			7		4.96	5.66	ns
			8		5.44	6.19	ns

Table 20: **Setup and Hold Times for the IOB Input Path *(Continued)***

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XC3S700A	1.82	1.95	ns
			2		2.62	2.83	ns
			3		3.32	3.72	ns
			4		3.83	4.31	ns
			5		3.69	4.14	ns
			6		4.60	5.19	ns
			7		5.39	6.10	ns
			8		5.92	6.73	ns
			1	XC3S1400A	1.79	2.17	ns
			2		2.55	2.92	ns
			3		3.38	3.76	ns
			4		3.75	4.32	ns
			5		3.81	4.19	ns
			6		4.39	5.09	ns
			7		5.16	5.98	ns
			8		5.69	6.57	ns
Hold Times							
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3)	0	XC3S50A	–0.66	–0.64	ns
				XC3S200A	–0.85	–0.65	ns
				XC3S400A	–0.42	–0.42	ns
				XC3S700A	–0.81	–0.67	ns
				XC3S1400A	–0.71	–0.71	ns
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XC3S50A	–0.88	–0.88	ns
			2		–1.33	–1.33	ns
			3		–2.05	–2.05	ns
			4		–2.43	–2.43	ns
			5		–2.34	–2.34	ns
			6		–2.81	–2.81	ns
			7		–3.03	–3.03	ns
			8		–3.83	–3.57	ns
			1	XC3S200A	–1.51	–1.51	ns
			2		–2.09	–2.09	ns
			3		–2.40	–2.40	ns
			4		–2.68	–2.68	ns
			5		–2.56	–2.56	ns
			6		–2.99	–2.99	ns
			7		–3.29	–3.29	ns
			8		–3.61	–3.61	ns