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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## Introduction

Kintex™-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices can operate at either of two  $V_{CCINT}$  voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at  $V_{CCINT} = 1.0V$ , the speed specification of a -2L device is the same as the -2 speed grade. When operated at  $V_{CCINT} = 0.9V$ , the -2L performance and static and dynamic power is reduced.

Kintex-7 FPGA DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing

characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Kintex-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at [www.xilinx.com/7](http://www.xilinx.com/7).

All specifications are subject to change without notice.

## DC Characteristics

Table 1: Absolute Maximum Ratings (1)

Symbol	Description	Min	Max	Units
<b>FPGA Logic</b>				
$V_{CCINT}$	Internal supply voltage	-0.5	1.1	V
$V_{CCAUX}$	Auxiliary supply voltage	-0.5	2.0	V
$V_{CCBRAM}$	Supply voltage for the block RAM memories	-0.5	1.1	V
$V_{CCO}$	Output drivers supply voltage for 3.3V HR I/O banks	-0.5	3.6	V
	Output drivers supply voltage for 1.8V HP I/O banks	-0.5	2.0	V
$V_{CCAUX\_IO}$	Auxiliary supply voltage	-0.5	2.06	V
$V_{REF}$	Input reference voltage	-0.5	2.0	V
$V_{IN}^{(2)(3)(4)}$	I/O input voltage	-0.5	$V_{CCO} + 0.5$	V
	I/O input voltage for $V_{REF}$ and differential I/O standards.	-0.5	2.625	V
$V_{CCBATT}$	Key memory battery backup supply	-0.5	2.0	V
<b>GTX Transceiver</b>				
$V_{MGTAVCC}$	Analog supply voltage for the GTX transmitter and receiver circuits	-0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTX transmitter and receiver termination circuits	-0.5	1.32	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers	-0.5	1.935	V
$V_{MGTREFCLK}$	GTX transceiver reference clock absolute input voltage	-0.5	1.32	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	-0.5	1.32	V
$V_{IN}$	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.26	V

**Table 1: Absolute Maximum Ratings (1) (Cont'd)**

Symbol	Description	Min	Max	Units
I <sub>DCIN</sub>	DC input current for receiver input pins DC coupled V <sub>MGTAVTT</sub> = 1.2V	–	14	mA
I <sub>DCOUT</sub>	DC output current for transmitter pins DC coupled V <sub>MGTAVTT</sub> = 1.2V	–	14	mA
<b>XADC</b>				
V <sub>CCADC</sub>	XADC supply relative to GNDADC	–0.5	2.0	V
V <sub>REFP</sub>	XADC reference input relative to GNDADC	–0.5	2.0	V
<b>Temperature</b>				
T <sub>STG</sub>	Storage temperature (ambient)	–65	150	°C
T <sub>SOL</sub>	Maximum soldering temperature for Pb/Sn component bodies (6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies (6)	–	+260	°C
T <sub>j</sub>	Maximum junction temperature(6)	–	+125	°C

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to [UG471: 7 Series FPGAs SelectIO Resources User Guide](#).
- The maximum limit applied to DC and AC signals.
- For maximum undershoot and overshoot AC specifications, see [Table 4](#) and [Table 5](#).
- For soldering guidelines and thermal considerations, see [UG475: 7 Series FPGA Packaging and Pinout Specification](#).

**Table 2: Recommended Operating Conditions (1)**

Symbol	Description	Min	Typ	Max	Units
<b>FPGA Logic</b>					
V <sub>CCINT</sub> (2)	Internal supply voltage	0.97	1.00	1.03	V
	For -2L (0.9V) devices: internal supply voltage	0.87	0.90	0.93	V
V <sub>CCBRAM</sub> (2)	Block RAM supply voltage	0.97	1.00	1.03	V
	For -2L (0.9V) devices: block RAM supply voltage	0.87	0.90	1.03	V
V <sub>CCAUX</sub>	Auxiliary supply voltage	1.71	1.80	1.89	V
V <sub>CCO</sub> (3)(4)	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
	Supply voltage for 1.8V HP I/O banks	1.14	–	1.89	V
V <sub>CCAUX_IO</sub>	Auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	Auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
V <sub>IN</sub> (5)	I/O input voltage	–0.20	–	V <sub>CCO</sub> + 0.2	V
	I/O input voltage for V <sub>REF</sub> and differential I/O standards	–0.20	–	2.625	V
I <sub>IN</sub> (6)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V <sub>CCBATT</sub> (7)	Battery voltage	1.0	–	1.89	V
<b>GTX Transceiver</b>					
V <sub>MGTAVCC</sub> (8)	Analog supply voltage for the GTX transceiver QPLL frequency range ≤ 10.3125 GHz(9)(10)	0.97	1.0	1.08	V
	Analog supply voltage for the GTX transceiver QPLL frequency range > 10.3125 GHz	1.02	1.05	1.08	V
V <sub>MGTAVTT</sub> (8)	Analog supply voltage for the GTX transmitter and receiver termination circuits	1.17	1.2	1.23	V
V <sub>MGTVCCAUX</sub> (8)	Auxiliary analog QPLL voltage supply for the transceivers	1.75	1.80	1.85	V

Table 2: Recommended Operating Conditions (1) (Cont'd)

Symbol	Description	Min	Typ	Max	Units
$V_{MGTAVTTRCAL}$ (8)	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
<b>XADC</b>					
$V_{CCADC}$	XADC supply relative to GNDADC	1.71	1.80	1.89	V
$V_{REFP}$	Externally supplied reference voltage	1.20	1.25	1.30	V
<b>Temperature</b>					
$T_j$	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

**Notes:**

1. All voltages are relative to ground.
2.  $V_{CCINT}$  and  $V_{CCBRAM}$  should be connected to the same supply.
3. Configuration data is retained even if  $V_{CCO}$  drops to 0V.
4. Includes  $V_{CCO}$  of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7.  $V_{CCBATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{CCBATT}$  to either ground or  $V_{CCAUX}$ .
8. Each voltage listed requires the filter circuit described in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#).
9. For data rates  $\leq 10.3125$  Gb/s,  $V_{MGTAVCC}$  should be  $1.0V \pm 3\%$  for lower power consumption.
10. For lower power consumption,  $V_{MGTAVCC}$  should be  $1.0V \pm 3\%$  over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ(1)	Max	Units
$V_{DRINT}$	Data retention $V_{CCINT}$ voltage (below which configuration data might be lost)	0.75	–	–	V
$V_{DRI}$	Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost)	1.5	–	–	V
$I_{REF}$	$V_{REF}$ leakage current per pin	–	–	15	$\mu A$
$I_L$	Input or output leakage current per pin (sample-tested)	–	–	15	$\mu A$
$C_{IN}$ (2)	Die input capacitance at the pad	–	–	8	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 3.3V$	90	–	330	$\mu A$
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 2.5V$	68	–	250	$\mu A$
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.8V$	34	–	220	$\mu A$
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.5V$	23	–	150	$\mu A$
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.2V$	12	–	120	$\mu A$
$I_{RPD}$	Pad pull-down (when selected) @ $V_{IN} = 3.3V$	68	–	330	$\mu A$
	Pad pull-down (when selected) @ $V_{IN} = 1.8V$	45	–	180	$\mu A$
$I_{CCADC}$	Analog supply current, analog circuits in powered up state	–	–	25	mA
$I_{BATT}$ (3)	Battery supply current	–	–	150	nA

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ <sup>(1)</sup>	Max	Units
R <sub>IN_TERM</sub> <sup>(4)</sup>	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V<sub>CCO</sub>/2 level.

Table 4: Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks<sup>(1)</sup>

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V <sub>CCO</sub> + 0.40	100	–0.40	100
V <sub>CCO</sub> + 0.45	100	–0.45	61.7
V <sub>CCO</sub> + 0.50	100	–0.50	25.8
V <sub>CCO</sub> + 0.55	100	–0.55	11.0
V <sub>CCO</sub> + 0.60	46.6	–0.60	4.77
V <sub>CCO</sub> + 0.65	21.2	–0.65	2.10
V <sub>CCO</sub> + 0.70	9.75	–0.70	0.94
V <sub>CCO</sub> + 0.75	4.55	–0.75	0.43
V <sub>CCO</sub> + 0.80	2.15	–0.80	0.20
V <sub>CCO</sub> + 0.85	1.02	–0.85	0.09
V <sub>CCO</sub> + 0.90	0.49	–0.90	0.04
V <sub>CCO</sub> + 0.95	0.24	–0.95	0.02

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

Table 5: Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks<sup>(1)(2)</sup>

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V <sub>CCO</sub> + 0.40	100	–0.40	100
V <sub>CCO</sub> + 0.45	100	–0.45	100
V <sub>CCO</sub> + 0.50	100	–0.50	100
V <sub>CCO</sub> + 0.55	100	–0.55	100
V <sub>CCO</sub> + 0.60	50.0	–0.60	50.0
V <sub>CCO</sub> + 0.65	50.0	–0.65	50.0
V <sub>CCO</sub> + 0.70	47.0	–0.70	50.0
V <sub>CCO</sub> + 0.75	21.2	–0.75	50.0

Table 5: Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks<sup>(1)(2)</sup> (Cont'd)

AC Voltage Overshoot	% of UI @-40°C to 100°C	AC Voltage Undershoot	% of UI @-40°C to 100°C
V <sub>CCO</sub> + 0.80	9.71	-0.80	50.0
V <sub>CCO</sub> + 0.85	4.51	-0.85	28.4
V <sub>CCO</sub> + 0.90	2.12	-0.90	12.7
V <sub>CCO</sub> + 0.95	1.01	-0.95	5.79

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μs.

Table 6: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I <sub>CCINTQ</sub>	Quiescent V <sub>CCINT</sub> supply current	XC7K70T	241	241	241	187	mA
		XC7K160T	474	474	474	368	mA
		XC7K325T	810	810	810	629	mA
		XC7K355T	993	993	993	771	mA
		XC7K410T	1080	1080	1080	838	mA
		XC7K420T	1313	1313	1313	1019	mA
		XC7K480T	1313	1313	1313	1019	mA
I <sub>CCOQ</sub>	Quiescent V <sub>CCO</sub> supply current	XC7K70T	1	1	1	1	mA
		XC7K160T	1	1	1	1	mA
		XC7K325T	1	1	1	1	mA
		XC7K355T	1	1	1	1	mA
		XC7K410T	1	1	1	1	mA
		XC7K420T	1	1	1	1	mA
		XC7K480T	1	1	1	1	mA
I <sub>CCAUXQ</sub>	Quiescent V <sub>CCAUX</sub> supply current	XC7K70T	21	21	21	21	mA
		XC7K160T	40	40	40	40	mA
		XC7K325T	68	68	68	68	mA
		XC7K355T	75	75	75	75	mA
		XC7K410T	85	85	85	85	mA
		XC7K420T	99	99	99	99	mA
		XC7K480T	99	99	99	99	mA
I <sub>CCAUX_IOQ</sub>	Quiescent V <sub>CCAUX_IO</sub> supply current	XC7K70T	N/A	N/A	N/A	N/A	mA
		XC7K160T	2	2	2	2	mA
		XC7K325T	2	2	2	2	mA
		XC7K355T	N/A	N/A	N/A	N/A	mA
		XC7K410T	2	2	2	2	mA
		XC7K420T	N/A	N/A	N/A	N/A	mA
		XC7K480T	N/A	N/A	N/A	N/A	mA

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I <sub>CCBRAMQ</sub>	Quiescent V <sub>CCBRAM</sub> supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T<sub>j</sub>) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V<sub>CCINT</sub>, V<sub>CCBRAM</sub>, V<sub>CCAUX</sub>, V<sub>CCAUX\_IO</sub>, and V<sub>CCO</sub> to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V<sub>CCINT</sub> and V<sub>CCBRAM</sub> have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V<sub>CCAUX</sub>, V<sub>CCAUX\_IO</sub>, and V<sub>CCO</sub> have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V<sub>CCO</sub> voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V<sub>CCO</sub> and V<sub>CCAUX</sub> must not exceed 2.625V for longer than T<sub>VCCO2VCCAUX</sub> for each power-on/off cycle to maintain device reliability levels.
- The T<sub>VCCO2VCCAUX</sub> time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V<sub>CCINT</sub>, V<sub>MGTAVCC</sub>, V<sub>MGTAVTT</sub> OR V<sub>MGTAVCC</sub>, V<sub>CCINT</sub>, V<sub>MGTAVTT</sub>. There is no recommended sequencing for V<sub>MGTVCCAUX</sub>. Both V<sub>MGTAVCC</sub> and V<sub>CCINT</sub> can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from V<sub>MGTAVTT</sub> can be higher than specifications during power-up and power-down.

- When V<sub>MGTAVTT</sub> is powered before V<sub>MGTAVCC</sub> and V<sub>MGTAVTT</sub> - V<sub>MGTAVCC</sub> > 150 mV and V<sub>MGTAVCC</sub> < 0.7V, the V<sub>MGTAVTT</sub> current draw can increase by 460 mA per transceiver during V<sub>MGTAVCC</sub> ramp up. The duration of the current draw can be up to 0.3 x T<sub>MGTAVCC</sub> (ramp time from GND to 90% of V<sub>MGTAVCC</sub>). The reverse is true for power-down.
- When V<sub>MGTAVTT</sub> is powered before V<sub>CCINT</sub> and V<sub>MGTAVTT</sub> - V<sub>CCINT</sub> > 150 mV and V<sub>CCINT</sub> < 0.7V, the V<sub>MGTAVTT</sub> current draw can increase by 50 mA per transceiver during V<sub>CCINT</sub> ramp up. The duration of the current draw can be up to 0.3 x T<sub>VCCINT</sub> (ramp time from GND to 90% of V<sub>CCINT</sub>). The reverse is true for power-down.

Table 7 shows the minimum current, in addition to  $I_{CCQ}$ , that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after  $V_{CCINT}$  is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

**Table 7: Power-On Current for Kintex-7 Devices**

Device	$I_{CCINTMIN}$ Typ <sup>(1)</sup>	$I_{CCAUXMIN}$ Typ <sup>(1)</sup>	$I_{CCOMIN}$ Typ <sup>(1)</sup>	$I_{CCAUX_IOMIN}$ Typ <sup>(1)</sup>	$I_{CCBRAMMIN}$ Typ <sup>(1)</sup>	Units
XC7K70T	$I_{CCINTQ} + 450$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAUXXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K160T	$I_{CCINTQ} + 550$	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAUXXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K325T	$I_{CCINTQ} + 600$	$I_{CCAUXQ} + 80$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAUXXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K355T	$I_{CCINTQ} + 1450$	$I_{CCAUXQ} + 109$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAUXXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 81$	mA
XC7K410T	$I_{CCINTQ} + 1500$	$I_{CCAUXQ} + 125$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAUXXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 90$	mA
XC7K420T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAUXXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA
XC7K480T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAUXXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA

**Notes:**

- Typical values are specified at nominal voltage, 25°C.
- Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

**Table 8: Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCINT}$	Ramp time from GND to 90% of $V_{CCINT}$		0.2	50	ms
$T_{VCCO}$	Ramp time from GND to 90% of $V_{CCO}$		0.2	50	ms
$T_{VCCAUX}$	Ramp time from GND to 90% of $V_{CCAUX}$		0.2	50	ms
$T_{VCCAUX_IO}$	Ramp time from GND to 90% of $V_{CCAUX_IO}$		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of $V_{CCBRAM}$		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

**Notes:**

- Based on 240,000 power cycles with nominal  $V_{CCO}$  of 3.3V or 36,500 power cycles with a worst case  $V_{CCO}$  of 3.465V.



## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels (1)(2)

I/O Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_I_12	-0.300	$V_{REF} - 0.080$	$V_{REF} + 0.080$	$V_{CCO} + 0.300$	25% $V_{CCO}$	75% $V_{CCO}$	6.3	-6.3
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% $V_{CCO}$	80% $V_{CCO}$	0.1	-0.1
LVC MOS12	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15, LVDCI_15	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	25% $V_{CCO}$	75% $V_{CCO}$	Note 4	Note 4
LVC MOS18, LVDCI_18	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LVC MOS33	-0.300	0.800	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LV TTL	-0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	-0.300	20% $V_{CCO}$	80% $V_{CCO}$	$V_{CCO} + 0.300$	10% $V_{CCO}$	90% $V_{CCO}$	0.1	-0.1
PCI33_3	-0.500	30% $V_{CCO}$	50% $V_{CCO}$	$V_{CCO} + 0.500$	10% $V_{CCO}$	90% $V_{CCO}$	1.5	-0.5
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	14.25	-14.25
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.0	-13.0
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.9	-8.9
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.0	-13.0
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.9	-8.9
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8	-8
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.4	-13.4

**Notes:**

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see [UG471: 7 Series FPGAs SelectIO Resources User Guide](#).

Table 10: Differential SelectIO DC Input and Output Levels

I/O Standard	V <sub>ICM</sub> <sup>(1)</sup>			V <sub>ID</sub> <sup>(2)</sup>			V <sub>OCM</sub> <sup>(3)</sup>			V <sub>OD</sub> <sup>(4)</sup>		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V <sub>CCAUX</sub>	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V <sub>CCAUX</sub>	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V <sub>CCO</sub> –0.405	V <sub>CCO</sub> –0.300	V <sub>CCO</sub> –0.190	0.400	0.600	0.800

**Notes:**

1. V<sub>ICM</sub> is the input common mode voltage.
2. V<sub>ID</sub> is the input differential voltage (Q –  $\bar{Q}$ ).
3. V<sub>OCM</sub> is the output common mode voltage.
4. V<sub>OD</sub> is the output differential voltage (Q –  $\bar{Q}$ ).
5. V<sub>OD</sub> for BLVDS will vary significantly depending on topology and loading.
6. LVDS\_25 is specified in Table 12.
7. LVDS is specified in Table 13.

Table 11: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	V <sub>ICM</sub> <sup>(1)</sup>			V <sub>ID</sub> <sup>(2)</sup>		V <sub>OL</sub> <sup>(3)</sup>	V <sub>OH</sub> <sup>(4)</sup>	I <sub>OL</sub>	I <sub>OH</sub>
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V <sub>CCO</sub> –0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V <sub>CCO</sub> –0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V <sub>CCO</sub> –0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V <sub>CCO</sub> –0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V <sub>CCO</sub>	80% V <sub>CCO</sub>	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V <sub>CCO</sub>	90% V <sub>CCO</sub>	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V <sub>CCO</sub> /2) – 0.150	(V <sub>CCO</sub> /2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V <sub>CCO</sub> /2) – 0.150	(V <sub>CCO</sub> /2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V <sub>CCO</sub> /2) – 0.150	(V <sub>CCO</sub> /2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V <sub>CCO</sub> /2) – 0.175	(V <sub>CCO</sub> /2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V <sub>CCO</sub> /2) – 0.175	(V <sub>CCO</sub> /2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V <sub>CCO</sub> /2) – 0.470	(V <sub>CCO</sub> /2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V <sub>CCO</sub> /2) – 0.600	(V <sub>CCO</sub> /2) + 0.600	13.4	–13.4

**Notes:**

1. V<sub>ICM</sub> is the input common mode voltage.
2. V<sub>ID</sub> is the input differential voltage (Q –  $\bar{Q}$ ).
3. V<sub>OL</sub> is the single-ended low-output voltage.
4. V<sub>OH</sub> is the single-ended high-output voltage.

## LVDS DC Specifications (LVDS\_25)

The LVDS\_25 standard is available in the HR I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 12: LVDS\_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}$	Supply Voltage		2.375	2.500	2.625	V
$V_{OH}$	Output High Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	–	–	1.675	V
$V_{OL}$	Output Low Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	0.700	–	–	V
$V_{ODIFF}$	Differential Output Voltage (Q – $\bar{Q}$ ), Q = High ( $\bar{Q}$ – Q), $\bar{Q}$ = High	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	247	350	600	mV
$V_{OCM}$	Output Common-Mode Voltage	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.000	1.250	1.425	V
$V_{IDIFF}$	Differential Input Voltage (Q – $\bar{Q}$ ), Q = High ( $\bar{Q}$ – Q), $\bar{Q}$ = High		100	350	600	mV
$V_{ICM}$	Input Common-Mode Voltage		0.300	1.200	1.425	V

## LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}$	Supply Voltage		1.710	1.800	1.890	V
$V_{OH}$	Output High Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	–	–	1.675	V
$V_{OL}$	Output Low Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	0.825	–	–	V
$V_{ODIFF}$	Differential Output Voltage (Q – $\bar{Q}$ ), Q = High ( $\bar{Q}$ – Q), $\bar{Q}$ = High	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	247	350	600	mV
$V_{OCM}$	Output Common-Mode Voltage	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.000	1.250	1.425	V
$V_{IDIFF}$	Differential Input Voltage (Q – $\bar{Q}$ ), Q = High ( $\bar{Q}$ – Q), $\bar{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
$V_{ICM}$	Input Common-Mode Voltage	Differential input voltage = $\pm 350$ mV	0.300	1.200	1.425	V

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in ISE® software 14.3 v1.07 for the -3, -2, -2L(1.0V), -1, and v1.06 for -2L(0.9V) speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 14](#) correlates the current status of each Kintex-7 device on a per speed grade basis.

Table 14: Kintex-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7K70T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K160T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K325T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K355T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K410T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K420T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K480T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 15 lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 15: Kintex-7 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7K70T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K160T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K325T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K355T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K410T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K420T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K480T	ISE 14.2 v1.06			ISE 14.3 v1.06

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 11](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 16: Networking Applications Interface Performances

Description	I/O Bank Type	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s
SDR LVDS receiver (SFI-4.1) <sup>(1)</sup>	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS receiver (SPI-4.2) <sup>(1)</sup>	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s

### Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 17: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)<sup>(1)(2)</sup>

Memory Standard	I/O Bank Type	V <sub>CCAUX_IO</sub>	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
<b>4:1 Memory Controllers</b>							
DDR3	HP	2.0V	1866	1866	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	1066	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	800	800	800	Mb/s
RLDRAM III <sup>(3)</sup>	HP	2.0V	800	667	667	533	MHz
	HP	1.8V	550	500	450	450	MHz
	HR	N/A	N/A				
<b>2:1 Memory Controllers</b>							
DDR3	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+ <sup>(4)</sup>	HP	2.0V	550	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
RLDRAM II	HP	2.0V	533	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
LPDDR2 <sup>(3)</sup>	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s

**Notes:**

1. V<sub>REF</sub> tracking is required. For more information, see [UG586](#), 7 Series FPGAs Memory Interface Solutions User Guide.
2. When using the internal V<sub>REF</sub> the maximum data rate is 800 Mb/s (400 MHz).
3. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)<sup>(1)(2)</sup>

Memory Standard	I/O Bank Type	V <sub>CCAUX_IO</sub> <sup>(3)</sup>	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
<b>4:1 Memory Controllers</b>							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III <sup>(4)</sup>	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
<b>2:1 Memory Controllers</b>							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+ <sup>(5)</sup>	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2 <sup>(4)</sup>	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

**Notes:**

1. V<sub>REF</sub> tracking is required. For more information, see [UG586](#), *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V<sub>REF</sub> the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V<sub>CCAUX\_IO</sub> supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

### IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$  is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$  is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than  $T_{IOTP}$  when the DCITERMDISABLE pin is used. In HR I/O banks, the IN\_TERM termination turn-on time is always faster than  $T_{IOTP}$  when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	$T_{IOPI}$				$T_{IOOP}$				$T_{IOTP}$				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTTL_S4	1.31	1.42	1.64	1.51	5.27	5.63	6.05	4.13	6.03	6.49	7.04	4.64	ns
LVTTTL_S8	1.31	1.42	1.64	1.51	4.45	4.83	5.30	3.86	5.21	5.69	6.29	4.38	ns
LVTTTL_S12	1.31	1.42	1.64	1.51	4.45	4.83	5.29	3.84	5.21	5.69	6.28	4.36	ns
LVTTTL_S16	1.31	1.42	1.64	1.51	3.47	3.88	4.40	3.39	4.23	4.74	5.39	3.91	ns
LVTTTL_S24	1.31	1.42	1.64	1.51	3.58	3.99	4.51	3.61	4.34	4.85	5.50	4.13	ns
LVTTTL_F4	1.31	1.42	1.64	1.51	4.70	4.98	5.29	3.58	5.46	5.84	6.28	4.09	ns
LVTTTL_F8	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.06	4.42	4.92	5.55	3.58	ns
LVTTTL_F12	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.05	4.42	4.92	5.55	3.56	ns
LVTTTL_F16	1.31	1.42	1.64	1.51	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVTTTL_F24	1.31	1.42	1.64	1.51	2.41	2.64	2.89	2.94	3.17	3.50	3.88	3.45	ns
LVDS_25 <sup>(1)</sup>	0.64	0.68	0.80	0.83	1.36	1.47	1.55	1.58	2.12	2.33	2.54	2.09	ns
MINI_LVDS_25	0.68	0.70	0.79	0.83	1.36	1.47	1.55	1.59	2.12	2.33	2.54	2.11	ns
BLVDS_25 <sup>(1)</sup>	0.65	0.69	0.80	0.83	1.83	2.02	2.20	2.16	2.59	2.88	3.19	2.67	ns
RSDS_25 (point to point) <sup>(1)</sup>	0.63	0.68	0.79	0.83	1.36	1.48	1.55	1.59	2.12	2.34	2.54	2.11	ns
PPDS_25 <sup>(1)</sup>	0.65	0.69	0.80	0.83	1.36	1.49	1.58	1.59	2.12	2.35	2.57	2.11	ns
TMDS_33 <sup>(1)</sup>	0.72	0.76	0.86	0.83	1.43	1.54	1.60	1.70	2.19	2.40	2.59	2.22	ns
PCI33_3 <sup>(1)</sup>	1.28	1.41	1.65	1.50	2.71	3.08	3.52	3.42	3.47	3.94	4.51	3.94	ns
HSUL_12	0.63	0.64	0.71	0.79	2.06	2.31	2.59	2.13	2.82	3.17	3.58	2.64	ns
DIFF_HSUL_12	0.58	0.61	0.70	0.81	1.83	2.04	2.26	1.92	2.59	2.90	3.25	2.44	ns
HSTL_I_S	0.61	0.64	0.73	0.79	1.55	1.69	1.80	1.91	2.31	2.55	2.79	2.42	ns
HSTL_II_S	0.61	0.64	0.73	0.78	1.21	1.34	1.43	1.70	1.97	2.20	2.42	2.22	ns
HSTL_I_18_S	0.64	0.67	0.76	0.79	1.28	1.39	1.45	1.58	2.04	2.25	2.44	2.09	ns
HSTL_II_18_S	0.64	0.67	0.76	0.79	1.18	1.31	1.40	1.69	1.94	2.17	2.39	2.20	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.78	1.42	1.54	1.61	1.84	2.18	2.40	2.60	2.36	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.79	1.15	1.24	1.27	1.78	1.91	2.10	2.26	2.30	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	0.79	1.27	1.38	1.43	1.67	2.03	2.24	2.42	2.19	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	0.81	1.14	1.23	1.26	1.72	1.90	2.09	2.25	2.23	ns



**Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)**

I/O Standard	T <sub>IOP1</sub>				T <sub>IOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_I_F	0.61	0.64	0.73	0.79	1.10	1.19	1.23	1.41	1.86	2.05	2.22	1.92	ns
HSTL_II_F	0.61	0.64	0.73	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
HSTL_I_18_F	0.64	0.67	0.76	0.79	1.05	1.18	1.28	1.44	1.81	2.04	2.27	1.95	ns
HSTL_II_18_F	0.64	0.67	0.76	0.79	1.03	1.14	1.23	1.42	1.79	2.00	2.22	1.94	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	0.78	1.09	1.18	1.22	1.48	1.85	2.04	2.21	2.00	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	0.79	1.02	1.11	1.14	1.48	1.78	1.97	2.13	2.00	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	0.79	1.08	1.17	1.21	1.48	1.84	2.03	2.20	2.00	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	0.81	1.01	1.10	1.13	1.48	1.77	1.96	2.12	2.00	ns
LVC MOS33_S4	1.31	1.40	1.60	1.54	5.23	5.61	6.09	4.13	5.99	6.47	7.08	4.64	ns
LVC MOS33_S8	1.31	1.40	1.60	1.54	4.46	4.85	5.33	3.84	5.22	5.71	6.32	4.36	ns
LVC MOS33_S12	1.31	1.40	1.60	1.54	3.46	3.89	4.42	3.41	4.22	4.75	5.41	3.92	ns
LVC MOS33_S16	1.31	1.40	1.60	1.54	3.06	3.43	3.88	3.72	3.82	4.29	4.87	4.23	ns
LVC MOS33_F4	1.31	1.40	1.60	1.54	4.70	5.01	5.36	3.58	5.46	5.87	6.35	4.09	ns
LVC MOS33_F8	1.31	1.40	1.60	1.54	3.62	4.04	4.56	3.06	4.38	4.90	5.55	3.58	ns
LVC MOS33_F12	1.31	1.40	1.60	1.54	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVC MOS33_F16	1.31	1.40	1.60	1.54	2.44	2.69	2.96	2.88	3.20	3.55	3.95	3.39	ns
LVC MOS25_S4	1.08	1.16	1.32	1.36	4.49	4.80	5.16	3.44	5.25	5.66	6.15	3.95	ns
LVC MOS25_S8	1.08	1.16	1.32	1.36	3.66	4.04	4.49	3.20	4.42	4.90	5.48	3.72	ns
LVC MOS25_S12	1.08	1.16	1.32	1.36	2.77	3.10	3.49	2.80	3.53	3.96	4.48	3.31	ns
LVC MOS25_S16	1.08	1.16	1.32	1.36	3.24	3.62	4.09	3.14	4.00	4.48	5.08	3.66	ns
LVC MOS25_F4	1.08	1.16	1.32	1.36	3.96	4.31	4.72	3.06	4.72	5.17	5.71	3.58	ns
LVC MOS25_F8	1.08	1.16	1.32	1.36	2.43	2.87	3.42	2.50	3.19	3.73	4.41	3.02	ns
LVC MOS25_F12	1.08	1.16	1.32	1.36	2.23	2.63	3.13	2.48	2.99	3.49	4.12	3.00	ns
LVC MOS25_F16	1.08	1.16	1.32	1.36	1.92	2.17	2.45	2.33	2.68	3.03	3.44	2.84	ns
LVC MOS18_S4	0.64	0.66	0.74	0.87	3.24	3.45	3.66	1.91	4.00	4.31	4.65	2.42	ns
LVC MOS18_S8	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVC MOS18_S12	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVC MOS18_S16	0.64	0.66	0.74	0.87	1.82	2.03	2.24	1.84	2.58	2.89	3.23	2.36	ns
LVC MOS18_S24 <sup>(1)</sup>	0.64	0.66	0.74	0.87	1.74	1.92	2.08	1.92	2.50	2.78	3.07	2.44	ns
LVC MOS18_F4	0.64	0.66	0.74	0.87	3.12	3.31	3.49	1.77	3.88	4.17	4.48	2.28	ns
LVC MOS18_F8	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVC MOS18_F12	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVC MOS18_F16	0.64	0.66	0.74	0.87	1.52	1.68	1.81	1.72	2.28	2.54	2.80	2.23	ns
LVC MOS18_F24 <sup>(1)</sup>	0.64	0.66	0.74	0.87	1.34	1.46	1.55	1.66	2.10	2.32	2.54	2.17	ns
LVC MOS15_S4	0.66	0.69	0.81	0.90	3.48	3.74	4.03	2.22	4.24	4.60	5.02	2.73	ns
LVC MOS15_S8	0.66	0.69	0.81	0.90	2.37	2.67	3.01	2.41	3.13	3.53	4.00	2.92	ns
LVC MOS15_S12	0.66	0.69	0.81	0.90	1.83	2.03	2.23	1.91	2.59	2.89	3.22	2.42	ns

**Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)**

I/O Standard	T <sub>IOP1</sub>				T <sub>IOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS15_S16	0.66	0.69	0.81	0.90	1.76	1.95	2.13	1.91	2.52	2.81	3.12	2.42	ns
LVC MOS15_F4	0.66	0.69	0.81	0.90	3.39	3.60	3.80	1.98	4.15	4.46	4.79	2.50	ns
LVC MOS15_F8	0.66	0.69	0.81	0.90	1.79	1.99	2.18	1.92	2.55	2.85	3.17	2.44	ns
LVC MOS15_F12	0.66	0.69	0.81	0.90	1.40	1.54	1.65	1.67	2.16	2.40	2.64	2.19	ns
LVC MOS15_F16	0.66	0.69	0.81	0.90	1.37	1.51	1.61	1.66	2.13	2.37	2.60	2.17	ns
LVC MOS12_S4	0.88	0.91	1.00	1.01	3.85	4.22	4.69	2.89	4.61	5.08	5.68	3.41	ns
LVC MOS12_S8	0.88	0.91	1.00	1.01	2.52	2.96	3.52	2.41	3.28	3.82	4.51	2.92	ns
LVC MOS12_S12 <sup>(1)</sup>	0.88	0.91	1.00	1.01	2.06	2.31	2.59	2.11	2.82	3.17	3.58	2.63	ns
LVC MOS12_F4	0.88	0.91	1.00	1.01	3.44	3.73	4.06	2.30	4.20	4.59	5.05	2.81	ns
LVC MOS12_F8	0.88	0.91	1.00	1.01	1.72	2.04	2.40	1.86	2.48	2.90	3.39	2.38	ns
LVC MOS12_F12 <sup>(1)</sup>	0.88	0.91	1.00	1.01	1.54	1.71	1.87	1.69	2.30	2.57	2.86	2.20	ns
SSTL135_S	0.61	0.64	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
SSTL15_S	0.61	0.64	0.73	0.73	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
SSTL18_I_S	0.64	0.67	0.76	0.79	1.59	1.74	1.85	1.95	2.35	2.60	2.84	2.47	ns
SSTL18_II_S	0.64	0.67	0.76	0.78	1.27	1.40	1.50	1.63	2.03	2.26	2.49	2.14	ns
DIFF_SSTL135_S	0.59	0.61	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
DIFF_SSTL15_S	0.63	0.67	0.77	0.79	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	0.79	1.50	1.63	1.72	1.95	2.26	2.49	2.71	2.47	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	0.79	1.13	1.22	1.25	1.66	1.89	2.08	2.24	2.17	ns
SSTL135_F	0.61	0.64	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
SSTL15_F	0.61	0.64	0.73	0.73	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
SSTL18_I_F	0.64	0.67	0.76	0.79	1.12	1.22	1.26	1.44	1.88	2.08	2.25	1.95	ns
SSTL18_II_F	0.64	0.67	0.76	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
DIFF_SSTL135_F	0.59	0.61	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
DIFF_SSTL15_F	0.63	0.67	0.77	0.79	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	0.79	1.10	1.19	1.23	1.52	1.86	2.05	2.22	2.03	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	0.79	1.02	1.10	1.14	1.50	1.78	1.96	2.13	2.02	ns

**Notes:**

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

**Table 20: 1.8V IOB High Performance (HP) Switching Characteristics**

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVDS	0.75	0.79	0.92	0.89	1.05	1.17	1.24	1.43	1.68	1.92	2.06	2.04	ns
HSUL_12	0.69	0.72	0.82	0.95	1.65	1.84	2.05	1.80	2.29	2.59	2.87	2.41	ns
DIFF_HSUL_12	0.69	0.72	0.82	0.92	1.65	1.84	2.05	1.47	2.29	2.59	2.87	2.08	ns
HSTL_I_S	0.68	0.72	0.82	0.84	1.15	1.28	1.38	1.46	1.79	2.03	2.20	2.07	ns
HSTL_II_S	0.68	0.72	0.82	0.84	1.05	1.17	1.26	1.44	1.69	1.93	2.08	2.05	ns
HSTL_I_18_S	0.70	0.72	0.82	0.86	1.12	1.24	1.34	1.41	1.75	2.00	2.16	2.02	ns
HSTL_II_18_S	0.70	0.72	0.82	0.86	1.06	1.18	1.26	1.44	1.70	1.94	2.08	2.05	ns
HSTL_I_12_S	0.68	0.72	0.82	0.94	1.14	1.27	1.37	1.43	1.78	2.02	2.20	2.04	ns
HSTL_I_DCI_S	0.68	0.72	0.82	0.78	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_S	0.68	0.72	0.82	0.78	1.05	1.17	1.26	1.33	1.69	1.93	2.08	1.94	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	0.76	1.15	1.28	1.38	1.40	1.78	2.03	2.20	2.01	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	0.76	1.05	1.16	1.24	1.32	1.69	1.92	2.06	1.93	ns
HSTL_II_T_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	0.89	1.15	1.28	1.38	1.47	1.79	2.03	2.20	2.08	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	0.89	1.05	1.17	1.26	1.47	1.69	1.93	2.08	2.08	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	0.76	1.15	1.28	1.38	1.47	1.78	2.03	2.20	2.08	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	0.76	1.05	1.17	1.26	1.40	1.69	1.93	2.08	2.01	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	0.89	1.12	1.24	1.34	1.46	1.75	2.00	2.16	2.07	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	0.89	1.06	1.18	1.26	1.47	1.70	1.94	2.08	2.08	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	0.75	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	0.75	1.05	1.16	1.24	1.41	1.69	1.92	2.06	2.02	ns
DIFF_HSTL_II_T_DCI_18_S	0.75	0.79	0.92	0.76	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
HSTL_I_F	0.68	0.72	0.82	0.84	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_II_F	0.68	0.72	0.82	0.84	0.97	1.08	1.15	1.29	1.61	1.84	1.97	1.90	ns
HSTL_I_18_F	0.70	0.72	0.82	0.86	1.04	1.16	1.24	1.32	1.68	1.91	2.06	1.93	ns
HSTL_II_18_F	0.70	0.72	0.82	0.86	0.98	1.09	1.16	1.35	1.62	1.85	1.98	1.96	ns
HSTL_I_12_F	0.68	0.72	0.82	0.94	1.02	1.13	1.21	1.26	1.65	1.88	2.03	1.87	ns
HSTL_I_DCI_F	0.68	0.72	0.82	0.78	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.78	0.97	1.08	1.15	1.22	1.61	1.84	1.97	1.83	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	0.76	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.76	0.98	1.09	1.16	1.27	1.61	1.85	1.98	1.88	ns
HSTL_II_T_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	0.89	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	0.89	0.97	1.08	1.15	1.35	1.61	1.84	1.97	1.96	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	0.76	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T <sub>IOP1</sub>				T <sub>IOP0</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVC MOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVC MOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVC MOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVC MOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVC MOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVC MOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVC MOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVC MOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVC MOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVC MOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVC MOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVC MOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVC MOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVC MOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVC MOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVC MOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVC MOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVC MOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVC MOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVC MOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVC MOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVC MOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVC MOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVC MOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVC MOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVC MOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVC MOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVC MOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVC MOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVC MOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVC MOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

**Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)**

I/O Standard	T <sub>IOP1</sub>				T <sub>IOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS12_F8	0.64	0.67	0.78	0.95	1.27	1.42	1.55	1.41	1.91	2.18	2.37	2.02	ns
LVDCI_18	0.47	0.50	0.60	0.86	1.99	2.15	2.35	2.44	2.62	2.91	3.17	3.05	ns
LVDCI_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	2.40	2.62	2.99	3.40	3.01	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.87	1.99	2.15	2.34	1.86	2.62	2.90	3.17	2.48	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	1.83	2.62	2.99	3.40	2.44	ns
HSLVDCI_18	0.68	0.72	0.82	0.86	1.99	2.15	2.35	2.43	2.62	2.91	3.17	3.04	ns
HSLVDCI_15	0.68	0.72	0.82	0.84	1.98	2.23	2.58	2.27	2.62	2.99	3.40	2.88	ns
SSTL18_I_S	0.68	0.72	0.82	0.86	1.02	1.15	1.24	1.41	1.66	1.90	2.07	2.02	ns
SSTL18_II_S	0.68	0.72	0.82	0.87	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.76	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.78	0.88	0.98	1.08	1.26	1.51	1.74	1.90	1.87	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.78	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL15_S	0.68	0.72	0.82	0.81	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.78	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.80	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL135_S	0.69	0.72	0.82	0.89	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL12_S	0.69	0.72	0.82	0.95	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.89	1.02	1.15	1.24	1.43	1.66	1.90	2.07	2.04	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.89	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.75	0.88	0.98	1.08	1.33	1.51	1.74	1.90	1.94	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.89	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.75	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.76	0.94	1.06	1.15	1.38	1.57	1.82	1.97	1.99	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.91	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.43	1.60	1.85	2.01	2.04	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.91	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.78	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.80	1.03	1.17	1.27	1.41	1.66	1.92	2.09	2.02	ns

**Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)**

I/O Standard	T <sub>IOP1</sub>				T <sub>IOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
SSTL18_I_F	0.68	0.72	0.82	0.86	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL18_II_F	0.68	0.72	0.82	0.87	0.97	1.09	1.16	1.36	1.61	1.84	1.99	1.98	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.76	0.89	1.02	1.10	1.30	1.53	1.77	1.92	1.91	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.24	1.53	1.77	1.92	1.85	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.27	1.53	1.77	1.92	1.88	ns
SSTL15_F	0.68	0.72	0.82	0.81	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.78	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.80	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL135_F	0.69	0.72	0.82	0.89	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL12_F	0.69	0.72	0.82	0.95	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.26	1.54	1.79	1.93	1.87	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.89	0.94	1.06	1.15	1.38	1.58	1.82	1.97	1.99	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.89	0.97	1.09	1.16	1.40	1.61	1.84	1.99	2.01	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.36	1.53	1.77	1.92	1.98	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.75	0.89	1.02	1.10	1.32	1.53	1.77	1.92	1.93	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.38	1.53	1.77	1.92	1.99	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.75	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.76	0.89	1.01	1.09	1.35	1.53	1.77	1.91	1.96	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.35	1.52	1.76	1.90	1.96	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.78	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.80	0.91	1.03	1.11	1.33	1.54	1.79	1.93	1.94	ns

**Notes:**

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of  $T_{IOTPHZ}$  and  $T_{IOIBUFDISABLE}$ .  $T_{IOTPHZ}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).  $T_{IOIBUFDISABLE}$  is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than  $T_{IOTPHZ}$  when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN\_TERM termination turn-off time is always faster than  $T_{IOTPHZ}$  when the INTERMDISABLE pin is used.

**Table 21: IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{IOTPHZ}$	T input to pad high-impedance	0.76	0.86	0.99	0.62	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	2.17	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	1.86	ns

## Input/Output Logic Switching Characteristics

Table 22: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
<b>Setup/Hold</b>						
$T_{ICE1CK}/T_{ICKCE1}$	CE1 pin Setup/Hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	0.56/-0.16	ns
$T_{ISRCK}/T_{ICKSR}$	SR pin Setup/Hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	0.88/-0.30	ns
$T_{IDOCKE2}/T_{IOCKDE2}$	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
$T_{IDOCKDE2}/T_{IOCKDDE2}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
$T_{IDOCKE3}/T_{IOCKDE3}$	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
$T_{IDOCKDE3}/T_{IOCKDDE3}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
<b>Combinatorial</b>						
$T_{IDIE2}$	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.09	0.10	0.12	0.14	ns
$T_{IDIDE2}$	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.15	ns
$T_{IDIE3}$	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.09	0.10	0.12	0.14	ns
$T_{IDIDE3}$	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.15	ns
<b>Sequential Delays</b>						
$T_{IDLOE2}$	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.36	0.39	0.45	0.54	ns
$T_{IDLODE2}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.55	ns
$T_{IDLOE3}$	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.36	0.39	0.45	0.54	ns
$T_{IDLODE3}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.55	ns
$T_{ICKQ}$	CLK to Q outputs	0.47	0.50	0.58	0.71	ns
$T_{RQ\_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.32	ns
$T_{GSRQ\_ILOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
$T_{RQ\_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.32	ns
$T_{GSRQ\_ILOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
<b>Set/Reset</b>						
$T_{RPW\_ILOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.68	ns, Min
$T_{RPW\_ILOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.68	ns, Min



Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V		0.9V		
		-3	-2/-2L	-1	-2L	
<b>Setup/Hold</b>						
$T_{ODCK}/T_{OCKD}$	D1/D2 pins Setup/Hold with respect to CLK	0.45/-0.13	0.50/-0.13	0.58/-0.13	0.79/-0.18	ns
$T_{OOCECK}/T_{OCKOCE}$	OCE pin Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/-0.10	ns
$T_{OSRCK}/T_{OCKSR}$	SR pin Setup/Hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	0.62/-0.04	ns
$T_{OTCK}/T_{OCKT}$	T1/T2 pins Setup/Hold with respect to CLK	0.49/-0.16	0.56/-0.16	0.68/-0.16	0.67/-0.18	ns
$T_{OTCECK}/T_{OCKTCE}$	TCE pin Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/-0.10	ns
<b>Combinatorial</b>						
$T_{ODQ}$	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	1.18	ns
<b>Sequential Delays</b>						
$T_{OCKQ}$	CLK to OQ/TQ out	0.41	0.43	0.49	0.63	ns
$T_{RQ\_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	1.12	ns
$T_{GSRQ\_OLOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
$T_{RQ\_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	1.12	ns
$T_{GSRQ\_OLOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
<b>Set/Reset</b>						
$T_{RPW\_OLOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	0.68	ns, Min
$T_{RPW\_OLOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	0.68	ns, Min

## Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
<b>Setup/Hold for Control Lines</b>						
$T_{ISCK\_BITSLIP}/$ $T_{ISCK\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	0.02/0.21	ns
$T_{ISCK\_CE}/$ $T_{ISCK\_CE}^{(2)}$	CE pin Setup/Hold with respect to CLK (for CE1)	0.39/-0.02	0.44/-0.02	0.63/-0.02	0.51/-0.22	ns
$T_{ISCK\_CE2}/$ $T_{ISCK\_CE2}^{(2)}$	CE pin Setup/Hold with respect to CLKDIV (for CE2)	-0.12/0.29	-0.12/0.31	-0.12/0.35	-0.17/0.40	ns
<b>Setup/Hold for Data Lines</b>						
$T_{ISCK\_D}/$ $T_{ISCK\_D}$	D pin Setup/Hold with respect to CLK	-0.02/0.11	-0.02/0.12	-0.02/0.15	-0.04/0.19	ns
$T_{ISCK\_DDL}/$ $T_{ISCK\_DDL}$	DDL pin Setup/Hold with respect to CLK (using IDELAY) <sup>(1)</sup>	-0.02/0.11	-0.02/0.12	-0.02/0.15	-0.03/0.19	ns
$T_{ISCK\_D\_DDR}/$ $T_{ISCK\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	-0.02/0.11	-0.02/0.12	-0.02/0.15	-0.04/0.19	ns
$T_{ISCK\_DDL\_DDR}/$ $T_{ISCK\_DDL\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY) <sup>(1)</sup>	0.11/0.11	0.12/0.12	0.15/0.15	0.19/0.19	ns
<b>Sequential Delays</b>						
$T_{ISCK\_Q}$	CLKDIV to out at Q pin	0.46	0.47	0.58	0.67	ns
<b>Propagation Delays</b>						
$T_{ISDO\_DO}$	D input to DO output pin	0.09	0.10	0.12	0.14	ns

**Notes:**

- Recorded at 0 tap value.
- $T_{ISCK\_CE2}$  and  $T_{ISCK\_CE2}$  are reported as  $T_{ISCK\_CE}/T_{ISCK\_CE}$  in TRACE report.