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Introduction

The Zynq®-7000 All Programmable SoCs are available in -3, -2, -1, and -1LI speed grades, with -3 having the highest performance. The -1LI devices can operate at either of two programmable logic (PL) V_{CCINT}/V_{CCBRAM} voltages, 0.95V and 1.0V, and are screened for lower maximum static power. The speed specification of a -1LI device is the same as the -1 speed grade. When operated at PL $V_{CCINT}/V_{CCBRAM} = 0.95V$, the -1LI static and dynamic power is reduced. Zynq-7000 device DC and AC characteristics are specified in commercial, extended, industrial and expanded (Q-temp) temperature ranges. Except for the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in the commercial, extended, industrial, or Q-temp temperature ranges.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

The available device/package combinations are outlined in:

- *Zynq-7000 All Programmable SoC Overview* ([DS190](#))
- *XA Zynq-7000 All Programmable SoC Overview* ([DS188](#))
- *Defense-grade Zynq-7000Q All Programmable SoC Overview* ([DS196](#))

This Zynq-7000 AP SoC data sheet, which covers the specifications for the XC7Z007S, XC7Z012S, XC7Z014S, XC7Z010, XA7Z010, XC7Z015, XC7Z020, XA7Z020, and XQ7Z020, complements the Zynq-7000 AP SoC documentation suite available on the Xilinx website at www.xilinx.com/zynq.

DC Characteristics

Table 1: Absolute Maximum Ratings⁽¹⁾

Symbol	Description	Min	Max	Units
Processing System (PS)				
V_{CCPINT}	PS internal logic supply voltage	-0.5	1.1	V
V_{CCPAUX}	PS auxiliary supply voltage	-0.5	2.0	V
V_{CCPLL}	PS PLL supply	-0.5	2.0	V
V_{CCO_DDR}	PS DDR I/O supply voltage	-0.5	2.0	V
$V_{CCO_MIO}^{(2)}$	PS MIO I/O supply voltage	-0.5	3.6	V
V_{PREF}	PS input reference voltage	-0.5	2.0	V
$V_{PIN}^{(2)(3)(4)(5)}$	PS MIO I/O input voltage	-0.40	$V_{CCO_MIO} + 0.55$	V
	PS DDR I/O input voltage	-0.55	$V_{CCO_DDR} + 0.55$	V
Programmable Logic (PL)				
V_{CCINT}	PL internal supply voltage	-0.5	1.1	V
V_{CCAUX}	PL auxiliary supply voltage	-0.5	2.0	V
V_{CCBRAM}	PL supply voltage for the block RAM memories	-0.5	1.1	V
V_{CCO}	PL supply voltage for HR I/O banks	-0.5	3.6	V
V_{REF}	Input reference voltage	-0.5	2.0	V

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
V _{IN} ⁽³⁾⁽⁴⁾⁽⁵⁾	I/O input voltage for HR I/O banks	-0.40	V _{CCO} + 0.55	V
	I/O input voltage (when V _{CCO} = 3.3V) for V _{REF} and differential I/O standards except TMDS_33 ⁽⁶⁾	-0.40	2.625	V
V _{CCBATT}	Key memory battery backup supply	-0.5	2.0	V
GTP Transceiver (XC7Z015 Only)				
V _{MGTAVCC}	Analog supply voltage for the GTP transmitter and receiver circuits	-0.5	1.1	V
V _{MGTAVTT}	Analog supply voltage for the GTP transmitter and receiver termination circuits	-0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	-0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.26	V
I _{DCIN-FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating	-	14	mA
I _{DCIN-MGTAVTT}	DC input current for receiver input pins DC coupled RX termination = V _{MGTAVTT}	-	12	mA
I _{DCIN-GND}	DC input current for receiver input pins DC coupled RX termination = GND	-	6.5	mA
I _{DCOUT-FLOAT}	DC output current for transmitter pins DC coupled RX termination = floating	-	14	mA
I _{DCOUT-MGTAVTT}	DC output current for transmitter pins DC coupled RX termination = V _{MGTAVTT}	-	12	mA
XADC				
V _{CCADC}	XADC supply relative to GNDADC	-0.5	2.0	V
V _{REFP}	XADC reference input relative to GNDADC	-0.5	2.0	V
Temperature				
T _{STG}	Storage temperature (ambient)	-65	150	°C
T _{SOL}	Maximum soldering temperature for Pb/Sn component bodies ⁽⁷⁾	-	+220	°C
	Maximum soldering temperature for Pb-free component bodies ⁽⁷⁾	-	+260	°C
T _j	Maximum junction temperature ⁽⁷⁾	-	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide (UG471)* or the *Zynq-7000 All Programmable SoC Technical Reference Manual (UG585)*.
- The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see [Table 4](#).
- See [Table 11](#) for TMDS_33 specifications.
- For soldering guidelines and thermal considerations, see the *Zynq-7000 All Programmable SoC Packaging and Pinout Specification (UG865)*.

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
PS					
V _{CCPINT}	PS internal logic supply voltage	0.95	1.00	1.05	V
V _{CCPAUX}	PS auxiliary supply voltage	1.71	1.80	1.89	V
V _{CCPLL}	PS PLL supply	1.71	1.80	1.89	V
V _{CCO_DDR}	PS DDR I/O supply voltage	1.14	-	1.89	V
V _{CCO_MIO} ⁽³⁾	PS MIO I/O supply voltage for MIO banks	1.71	-	3.465	V

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
$V_{PIN}^{(4)}$	PS DDR and MIO I/O input voltage	-0.20	-	$V_{CCO_DDR} + 0.20$ $V_{CCO_MIO} + 0.20$	V
PL					
$V_{CCINT}^{(5)}$	PL internal supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) internal supply voltage	0.92	0.95	0.98	V
V_{CCAUX}	PL auxiliary supply voltage	1.71	1.80	1.89	V
$V_{CCBRAM}^{(5)}$	PL block RAM supply voltage	0.95	1.00	1.05	V
	PL -1LI (0.95V) block RAM supply voltage	0.92	0.95	0.98	V
$V_{CCO}^{(6)(7)}$	PL supply voltage for HR I/O banks	1.14	-	3.465	V
$V_{IN}^{(4)}$	I/O input voltage	-0.20	-	$V_{CCO} + 0.20$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMDS_33 ⁽⁸⁾	-0.20	-	2.625	V
$I_{IN}^{(9)}$	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	-	-	10	mA
$V_{CCBATT}^{(10)}$	Battery voltage	1.0	-	1.89	V
GTP Transceiver (XC7Z015 Only)					
$V_{MGTAVCC}^{(11)}$	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}^{(11)}$	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	-	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	-	100	°C
	Junction temperature operating range for industrial (I) temperature devices	-40	-	100	°C
	Junction temperature operating range for expanded (Q) temperature devices	-40	-	125	°C

Notes:

- All voltages are relative to ground. The PL and PS share a common ground.
- For the design of the power distribution system consult the *Zynq-7000 All Programmable SoC PCB Design Guide* ([UG933](#)).
- Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1} .
- The lower absolute voltage specification always applies.
- V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at $\pm 5\%$.
- See [Table 11](#) for TMDS_33 specifications.
- A total of 200 mA per PS or PL bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .
- Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTP Transceiver User Guide* ([UG482](#)).

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V _{DRINT}	Data retention V _{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V _{DRI}	Data retention V _{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I _{REF}	PS_DDR_VREF 0/1, PS_MIO_VREF, and V _{REF} leakage current per pin	–	–	15	μA
I _L	Input or output leakage current per pin (sample-tested)	–	–	15	μA
C _{IN} ⁽²⁾	PL die input capacitance at the pad	–	–	8	pF
C _{PIN} ⁽²⁾	PS die input capacitance at the pad	–	–	8	pF
I _{RPU}	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 3.3V	90	–	330	μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 2.5V	68	–	250	μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.8V	34	–	220	μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.5V	23	–	150	μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.2V	12	–	120	μA
I _{RPD}	Pad pull-down (when selected) @ V _{IN} = 3.3V	68	–	330	μA
	Pad pull-down (when selected) @ V _{IN} = 1.8V	45	–	180	μA
I _{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I _{BATT} ⁽³⁾	Battery supply current	–	–	150	nA
R _{IN_TERM} ⁽⁴⁾	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_40)	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_50)	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_60)	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and PL HR I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI @-40°C to 125°C	AC Voltage Undershoot	% of UI @-40°C to 125°C
$V_{CCO} + 0.55$	100	-0.40	100
		-0.45	61.7
		-0.50	25.8
		-0.55	11.0
$V_{CCO} + 0.60$	46.6	-0.60	4.77
$V_{CCO} + 0.65$	21.2	-0.65	2.10
$V_{CCO} + 0.70$	9.75	-0.70	0.94
$V_{CCO} + 0.75$	4.55	-0.75	0.43
$V_{CCO} + 0.80$	2.15	-0.80	0.20
$V_{CCO} + 0.85$	1.02	-0.85	0.09
$V_{CCO} + 0.90$	0.49	-0.90	0.04
$V_{CCO} + 0.95$	0.24	-0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO} + 0.20V$ or below GND $-0.20V$, must not exceed the values in this table.

Table 5: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	XC7Z007S	N/A	122	122	N/A	mA
		XC7Z012S	N/A	122	122	N/A	mA
		XC7Z014S	N/A	122	122	N/A	mA
		XC7Z010	122	122	122	85	mA
		XC7Z015	122	122	122	85	mA
		XC7Z020	122	122	122	85	mA
		XA7Z010	N/A	N/A	122	N/A	mA
		XA7Z020	N/A	N/A	122	N/A	mA
		XQ7Z020	N/A	122	122	85	mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	XC7Z007S	N/A	13	13	N/A	mA
		XC7Z012S	N/A	13	13	N/A	mA
		XC7Z014S	N/A	13	13	N/A	mA
		XC7Z010	13	13	13	11	mA
		XC7Z015	13	13	13	11	mA
		XC7Z020	13	13	13	11	mA
		XA7Z010	N/A	N/A	13	N/A	mA
		XA7Z020	N/A	N/A	13	N/A	mA
		XQ7Z020	N/A	13	13	11	mA

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
I _{CCDDRQ}	PS quiescent V _{CCO_DDR} supply current	XC7Z007S	N/A	4	4	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	4	4	N/A	mA
		XC7Z010	4	4	4	4	mA
		XC7Z015	4	4	4	4	mA
		XC7Z020	4	4	4	4	mA
		XA7Z010	N/A	N/A	4	N/A	mA
		XA7Z020	N/A	N/A	4	N/A	mA
		XQ7Z020	N/A	4	4	4	mA
I _{CCINTQ}	PL quiescent V _{CCINT} supply current	XC7Z007S	N/A	34	34	N/A	mA
		XC7Z012S	N/A	77	77	N/A	mA
		XC7Z014S	N/A	78	78	N/A	mA
		XC7Z010	34	34	34	21/23 ⁽⁴⁾	mA
		XC7Z015	77	77	77	47/53 ⁽⁴⁾	mA
		XC7Z020	78	78	78	48/54 ⁽⁴⁾	mA
		XA7Z010	N/A	N/A	34	N/A	mA
		XA7Z020	N/A	N/A	78	N/A	mA
		XQ7Z020	N/A	78	78	48/54 ⁽⁴⁾	mA
I _{CCAUXQ}	PL quiescent V _{CCAUX} supply current	XC7Z007S	N/A	18	18	N/A	mA
		XC7Z012S	N/A	35	35	N/A	mA
		XC7Z014S	N/A	38	38	N/A	mA
		XC7Z010	18	18	18	16	mA
		XC7Z015	35	35	35	31	mA
		XC7Z020	38	38	38	34	mA
		XA7Z010	N/A	N/A	18	N/A	mA
		XA7Z020	N/A	N/A	38	N/A	mA
		XQ7Z020	N/A	38	38	34	mA
I _{CCOQ}	PL quiescent V _{CCO} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	3	3	N/A	mA
		XC7Z014S	N/A	3	3	N/A	mA
		XC7Z010	3	3	3	3	mA
		XC7Z015	3	3	3	3	mA
		XC7Z020	3	3	3	3	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	3	N/A	mA
		XQ7Z020	N/A	3	3	3	mA

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1LI	
I _{CCBRAMQ}	PL quiescent V _{CCBRAM} supply current	XC7Z007S	N/A	3	3	N/A	mA
		XC7Z012S	N/A	4	4	N/A	mA
		XC7Z014S	N/A	6	6	N/A	mA
		XC7Z010	3	3	3	1/2 ⁽⁴⁾	mA
		XC7Z015	4	4	4	2/2 ⁽⁴⁾	mA
		XC7Z020	6	6	6	3/4 ⁽⁴⁾	mA
		XA7Z010	N/A	N/A	3	N/A	mA
		XA7Z020	N/A	N/A	6	N/A	mA
		XQ7Z020	N/A	6	6	3/4 ⁽⁴⁾	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. The Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) estimates operating current. When the required power-on current exceeds the estimated operating current, XPE can display the power-on current.
4. The first value is at 0.95V, and the second value is at 1.0V.

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCPINT} , then V_{CCPAUX} and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0} , V_{CCO_MIO1} , and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The PS_POR_B input is required to be asserted to GND during the power-on sequence until V_{CCPINT} , V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels to ensure PS eFUSE integrity. For additional information about PS_POR_B timing requirements refer to [Resets](#).

The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX} , V_{CCPLL} , and the PS V_{CCO} supplies (V_{CCO_MIO0} , V_{CCO_MIO1} , and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX} , with an optional ferrite bead filter. Before V_{CCPINT} reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, V_{CCPAUX} is lower than 0.70V, or V_{CCO_MIO0} is lower than 0.90V. The condition must be held until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} / V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

GTP Transceivers (XC7Z015 Only)

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers (XC7Z015 only) is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (V_{CCPINT} , V_{CCPAUX} , V_{CCPLL} , V_{CCO_DDR} , V_{CCO_MIO0} , and V_{CCO_MIO1}) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCO} , that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 6: Power-On Current for Zynq-7000 Devices

Device	$I_{CCPINTMIN}$	$I_{CCPAUXMIN}$	$I_{CCDDRMIN}$	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7Z007S	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 40$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z012S	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 130$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z014S	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 70$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z010 XA7Z010	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 40$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z015	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 130$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7Z020 XA7Z020 XQ7Z020	$I_{CCPINTQ} + 70$	$I_{CCPAUXQ} + 40$	$I_{CCDDRQ} + 100$ mA per bank	$I_{CCINTQ} + 70$	$I_{CCAUXQ} + 60$	$I_{CCOQ} + 90$ mA per bank	$I_{CCBRAMQ} + 40$	mA

Table 7: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO_MIO} - V_{CCPAUX} > 2.625V$	$T_j = 125^\circ C^{(1)}$	–	300	ms
		$T_j = 100^\circ C^{(1)}$	–	500	
		$T_j = 85^\circ C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: PS DC Input and Output Levels⁽¹⁾

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVC MOS18	-0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	$V_{CCO_MIO} + 0.300$	0.450	$V_{CCO_MIO} - 0.450$	8	-8
MIO	LVC MOS25	-0.300	0.700	1.700	$V_{CCO_MIO} + 0.300$	0.400	$V_{CCO_MIO} - 0.400$	8	-8
MIO	LVC MOS33	-0.300	0.800	2.000	3.450	0.400	$V_{CCO_MIO} - 0.400$	8	-8
MIO	HSTL_I_18	-0.300	$V_{PREF} - 0.100$	$V_{PREF} + 0.100$	$V_{CCO_MIO} + 0.300$	0.400	$V_{CCO_MIO} - 0.400$	8	-8
DDR	SSTL18_I	-0.300	$V_{PREF} - 0.125$	$V_{PREF} + 0.125$	$V_{CCO_DDR} + 0.300$	$V_{CCO_DDR}/2 - 0.470$	$V_{CCO_DDR}/2 + 0.470$	8	-8
DDR	SSTL15	-0.300	$V_{PREF} - 0.100$	$V_{PREF} + 0.100$	$V_{CCO_DDR} + 0.300$	$V_{CCO_DDR}/2 - 0.175$	$V_{CCO_DDR}/2 + 0.175$	13.0	-13.0
DDR	SSTL135	-0.300	$V_{PREF} - 0.090$	$V_{PREF} + 0.090$	$V_{CCO_DDR} + 0.300$	$V_{CCO_DDR}/2 - 0.150$	$V_{CCO_DDR}/2 + 0.150$	13.0	-13.0
DDR	HSUL_12	-0.300	$V_{PREF} - 0.130$	$V_{PREF} + 0.130$	$V_{CCO_DDR} + 0.300$	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	-0.1

Notes:

1. Tested according to relevant specifications.

Table 9: PS Complementary Differential DC Input and Output Levels

Bank	I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
		V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	-	20% V_{CCO}	80% V_{CCO}	0.100	-0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	-	$(V_{CCO_DDR}/2) - 0.150$	$(V_{CCO_DDR}/2) + 0.150$	13.0	-13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	-	$(V_{CCO_DDR}/2) - 0.175$	$(V_{CCO_DDR}/2) + 0.175$	13.0	-13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	-	$(V_{CCO_DDR}/2) - 0.470$	$(V_{CCO_DDR}/2) + 0.470$	8.00	-8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q-\bar{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

PL I/O Levels

Table 10: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾

I/O Standard	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	8.00	-8.00
HSTL_I_18	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	8.00	-8.00
HSTL_II	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	16.00	-16.00
HSTL_II_18	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	16.00	-16.00
HSUL_12	-0.300	V _{REF} - 0.130	V _{REF} + 0.130	V _{CCO} + 0.300	20% V _{CCO}	80% V _{CCO}	0.10	-0.10
LVC MOS12	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	Note 3	Note 3
LVC MOS15	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	25% V _{CCO}	75% V _{CCO}	Note 4	Note 4
LVC MOS18	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} - 0.450	Note 5	Note 5
LVC MOS25	-0.300	0.7	1.700	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	Note 4	Note 4
LVC MOS33	-0.300	0.8	2.000	3.450	0.400	V _{CCO} - 0.400	Note 4	Note 4
LV TTL	-0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	-0.300	20% V _{CCO}	80% V _{CCO}	V _{CCO} + 0.300	10% V _{CCO}	90% V _{CCO}	0.10	-0.10
PCI33_3	-0.400	30% V _{CCO}	50% V _{CCO}	V _{CCO} + 0.500	10% V _{CCO}	90% V _{CCO}	1.50	-0.50
SSTL135	-0.300	V _{REF} - 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	13.00	-13.00
SSTL135_R	-0.300	V _{REF} - 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	8.90	-8.90
SSTL15	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 - 0.175	V _{CCO} /2 + 0.175	13.00	-13.00
SSTL15_R	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 - 0.175	V _{CCO} /2 + 0.175	8.90	-8.90
SSTL18_I	-0.300	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 - 0.470	V _{CCO} /2 + 0.470	8.00	-8.00
SSTL18_II	-0.300	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 - 0.600	V _{CCO} /2 + 0.600	13.40	-13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)).

Table 11: Differential SelectIO DC Input and Output Levels

I/O Standard	V _{ICM} ⁽¹⁾			V _{ID} ⁽²⁾			V _{OCM} ⁽³⁾			V _{OD} ⁽⁴⁾		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	-	-	-	1.250	-	Note 5		
MINI_LVDS_25	0.300	1.200	V _{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V _{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V _{CCO} -0.405	V _{CCO} -0.300	V _{CCO} -0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q-Q̄).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q-Q̄).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in [Table 13](#).

Table 12: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO}-0.400$	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO}-0.400$	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO}-0.400$	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO}-0.400$	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q-\bar{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)
Table 13: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and \bar{Q}	$R_T = 100\Omega$ across Q and \bar{Q} signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and \bar{Q}	$R_T = 100\Omega$ across Q and \bar{Q} signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	$R_T = 100\Omega$ across Q and \bar{Q} signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\Omega$ across Q and \bar{Q} signals	1.00	1.25	1.425	V
V_{IDIFF}	Differential input voltage: (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.3	1.2	1.500	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide (UG471)* for more information.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.7 and Vivado® Design Suite 2015.4 as outlined in [Table 14](#).

Table 14: Zynq-7000 All Programmable SoC Speed Specification Version By Device

ISE 14.7	Vivado 2016.3	Device
1.08	1.11	XC7Z010 and XC7Z020
N/A	1.11	XC7Z007S, XC7Z012S, XC7Z014S, and XC7Z015
1.06	1.09	XA7Z010 and XA7Z020
1.06	1.10	XQ7Z020

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq-7000 devices.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 15](#) correlates the current status of each Zynq-7000 device on a per speed grade basis.

Table 15: Zynq-7000 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7Z007S			-2E, -2I, -1C, -1I
XC7Z012S			-2E, -2I, -1C, -1I
XC7Z014S			-2E, -2I, -1C, -1I
XC7Z010			-3E, -2E, -2I, -1C, -1I, -1LI
XC7Z015			-3E, -2E, -2I, -1C, -1I, -1LI

Table 15: Zynq-7000 Device Speed Grade Designations (Cont'd)

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7Z020			-3E, -2E, -2I, -1C, -1I, -1LI
XA7Z010			-1I, -1Q
XA7Z020			-1I, -1Q
XQ7Z020			-2I, -1I, -1Q, -1LI

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 16 lists the production released Zynq-7000 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: Zynq-7000 Device Production Software and Speed Specification Release

Device	Speed Grade Designations						
	-3E	-2E	-2I	-1C	-1I	-1LI	-1Q
XC7Z007S	N/A	Vivado tools 2016.3 v1.11				N/A	N/A
XC7Z012S	N/A	Vivado tools 2016.3 v1.11				N/A	N/A
XC7Z014S	N/A	Vivado tools 2016.3 v1.11				N/A	N/A
XC7Z010	ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06	ISE tools 14.4 and the 14.4 device pack v1.05 and Vivado tools 2013.1 v1.06				Vivado tools 2014.4 v1.11	N/A
XC7Z015	Vivado tools 2013.4 v1.09					Vivado tools 2014.4 v1.11	N/A
XC7Z020	ISE tools 14.5 v1.06 and Vivado tools 2013.1 v1.06	ISE tools 14.4 and the 14.4 device pack v1.05 and Vivado tools 2013.1 v1.06				Vivado tools 2014.4 v1.11	N/A
XA7Z010	N/A				ISE tools 14.5 v1.04 and Vivado tools 2013.1 v1.04	N/A	ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05
XA7Z020	N/A				ISE tools 14.5 v1.04 and Vivado tools 2013.1 v1.04	N/A	ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05
XQ7Z020	N/A	ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05	N/A	ISE tools 14.6 v1.05 and Vivado tools 2013.2 v1.05		Vivado tools 2015.4 v1.10	ISE tools 14.7 v1.06 and Vivado tools 2013.3 v1.06

Selecting the Correct Speed Grade and Voltage in the Vivado Tools

It is important to select the correct device speed grade and voltage in the Vivado tools for the device that you are selecting.

To select the -3, -2, or -1 (PL 1.0V) speed specifications in the Vivado tools, select the **Zynq-7000**, **XA Zynq-7000**, or **Defense Grade Zynq-7000** sub-family, and then select the part name that is the device name followed by the package name followed by the speed grade. For example, select the **xc7z020clg484-3** part name for the XC7Z020 device in the CLG484 package and -3 speed grade.

To select the -1LI (PL 0.95V) speed specifications in the Vivado tools, select the **Zynq-7000** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7z020iclg484-1L** part name for the XC7Z020 device in the CLG484 package and -1LI (PL 0.95V) speed grade. The -1LI (PL 0.95V) speed specifications are not supported in the ISE tools.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See [Table 16](#) for the subset of the Zynq-7000 devices supported in the ISE tools.

PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* ([UG585](#)).

Table 17: CPU Clock Domains Performance

Symbol	Clock Ratio	Description	Speed Grade				Units
			-3	-2	-1C/-1I/-1LI	-1Q	
$F_{\text{CPU_6X4X_621_MAX}}^{(1)}$	6:2:1	Maximum CPU clock frequency	866	766	667	667	MHz
$F_{\text{CPU_3X2X_621_MAX}}$		Maximum CPU_3X clock frequency	433	383	333	333	MHz
$F_{\text{CPU_2X_621_MAX}}$		Maximum CPU_2X clock frequency	288	255	222	222	MHz
$F_{\text{CPU_1X_621_MAX}}$		Maximum CPU_1X clock frequency	144	127	111	111	MHz
$F_{\text{CPU_6X4X_421_MAX}}^{(1)}$	4:2:1	Maximum CPU clock frequency	710	600	533	533	MHz
$F_{\text{CPU_3X2X_421_MAX}}$		Maximum CPU_3X clock frequency	355	300	267	267	MHz
$F_{\text{CPU_2X_421_MAX}}$		Maximum CPU_2X clock frequency	355	300	267	267	MHz
$F_{\text{CPU_1X_421_MAX}}$		Maximum CPU_1X clock frequency	178	150	133	133	MHz

Notes:

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.

Table 18: PS DDR Clock Domains Performance⁽¹⁾

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
$F_{\text{DDR3_MAX}}$	Maximum DDR3 interface performance	1066	1066	1066	1066	Mb/s
$F_{\text{DDR3L_MAX}}$	Maximum DDR3L interface performance	1066	1066	1066	1066	Mb/s
$F_{\text{DDR2_MAX}}$	Maximum DDR2 interface performance	800	800	800	800	Mb/s
$F_{\text{LPDDR2_MAX}}$	Maximum LPDDR2 interface performance	800	800	800	800	Mb/s
$F_{\text{DDRCLK_2XMAX}}$	Maximum DDR_2X clock frequency	444	408	355	355	MHz

Notes:

1. All performance numbers apply to both internal and external V_{REF} configurations.

Table 19: PS-PL Interface Performance

Symbol	Description	Min	Max	Units
$F_{\text{EMIOGEMCLK}}$	EMIO gigabit Ethernet controller maximum frequency	–	125	MHz
$F_{\text{EMIOSDCLK}}$	EMIO SD controller maximum frequency	–	25	MHz
$F_{\text{EMIOSPICLK}}$	EMIO SPI controller maximum frequency	–	25	MHz
$F_{\text{EMIOJTAGCLK}}$	EMIO JTAG controller maximum frequency	–	20	MHz
$F_{\text{EMIOTRACECLK}}$	EMIO trace controller maximum frequency	–	125	MHz
F_{FTMCLK}	Fabric trace monitor maximum frequency	–	125	MHz
$F_{\text{EMIODMACLK}}$	DMA maximum frequency	–	100	MHz
$F_{\text{AXI_MAX}}$	Maximum AXI interface performance	–	250	MHz

PS Switching Characteristics

Clocks

Table 20: System Reference Clock Input Requirements

Symbol	Description	Min	Typ	Max	Units
T _{JTPSCLK}	PS_CLK RMS clock jitter tolerance	–	–	±0.5	%
T _{DCPSCLK}	PS_CLK duty cycle	40	–	60	%
T _{RFPCLK}	PS_CLK rise and fall time	–	–	6	ns
F _{PSCLK}	PS_CLK frequency	30	–	60	MHz

Table 21: PS PLL Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1C/-1I/-1LI	-1Q	
T _{LOCK_PSPLL}	PLL maximum lock time	60	60	60	60	µs
F _{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	1600	MHz
F _{PSPLL_MIN}	PLL minimum output frequency	780	780	780	780	MHz

Resets

Table 22: PS Reset Assertion Timing Requirements

Symbol	Description	Min	Typ	Max	Units
T _{PSPOR}	Required PS_POR_B assertion time ⁽¹⁾	100	–	–	µs
T _{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_CLK Clock Cycles

Notes:

- PS_POR_B needs to be asserted Low until T_{PSPOR} after PS supply voltages reach minimum levels.

The PS_POR_B deassertion must meet the following requirements to avoid coinciding with the secure lockdown window. Figure 1 shows the timing relationship between PS_POR_B and the last power supply ramp (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, or V_{CCO} in bank 0). T_{SLW} minimum and maximum parameters define the beginning and end, respectively, of the secure lockdown window relative to the last PL power supply reaching 250 mV. The PS_POR_B must not be deasserted within the secure lockdown window.

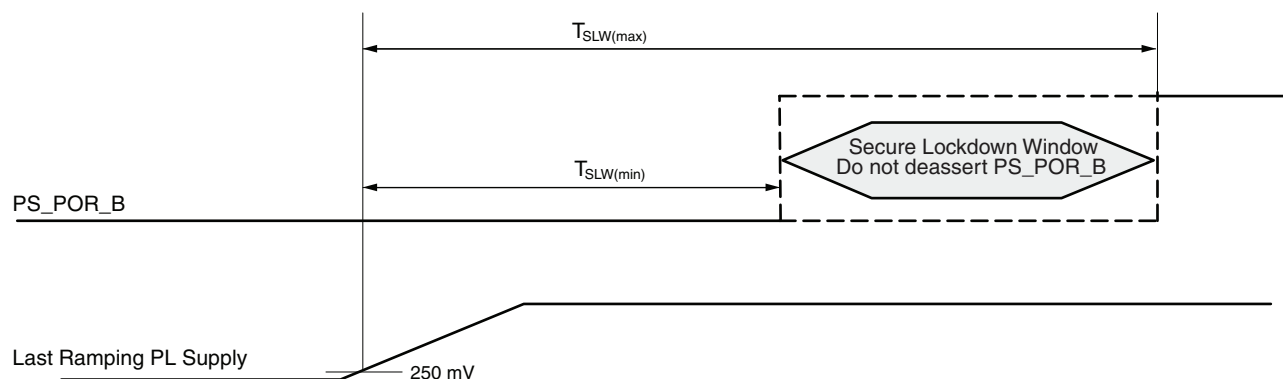


Figure 1: PS_POR_B and Power Supply Ramp Timing Requirements

Table 23: PS Reset/Power Supply Timing Requirements

Symbol	Description	PS_CLK Frequency (MHz)	Min	Max	Units
T _{SLW} ⁽¹⁾	128 KB CRC eFUSE disabled and PLL enabled. Default configuration	30	12	39	ms
		33.33	12	40	ms
		60	13	40	ms
	128 KB CRC eFUSE disabled and PLL in bypass.	30	-32	13	ms
		33.33	-27	13	ms
		60	-9	25	ms
	128 KB CRC eFUSE enabled and PLL enabled. ⁽²⁾	30	-19	9	ms
		33.33	-16	12	ms
		60	-3	25	ms
	128 KB CRC eFUSE enabled and PLL in bypass. ⁽²⁾	30	-830	-788	ms
		33.33	-746	-705	ms
		60	-408	-374	ms

Notes:

- Valid for power supply ramp times of less than 6 ms. For ramp times longer than 6 ms, see the BootROM Performance section of the *Zynq-7000 All Programmable SoC Technical Reference Manual (UG585)*.
- If any PS and PL power supplies are tied together, observe the PS_POR_B assertion time requirement (T_{PSPOR}) in [Table 22](#) and its accompanying note.

PS Configuration
Table 24: Processor Configuration Access Port Switching Characteristics

Symbol	Description	Min	Typ	Max	Units
F _{PCAPCK}	Maximum processor configuration access port (PCAP) frequency	-	-	100	MHz

DDR Memory Interfaces
Table 25: DDR3 Interface Switching Characteristics (1066 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
T _{DQVALID} ⁽²⁾	Input data valid window	450	-	ps
T _{DQDS} ⁽³⁾	Output DQ to DQS skew	131	-	ps
T _{DQDH} ⁽⁴⁾	Output DQS to DQ skew	288	-	ps
T _{DQSS}	Output clock to DQS skew	-0.11	0.09	T _{CK}
T _{CACK} ⁽⁵⁾	Command/address output setup time with respect to CLK	532	-	ps
T _{CKCA} ⁽⁶⁾	Command/address output hold time with respect to CLK	637	-	ps

Notes:

- Recommended V_{CCO_DDR} = 1.5V ±5%.
- Measurement is taken from V_{REF} to V_{REF}.
- Measurement is taken from either the rising edge of DQ that crosses V_{IH(AC)} or the falling edge of DQ that crosses V_{IL(AC)} to V_{REF} of DQS.
- Measurement is taken from either the rising edge of DQ that crosses V_{IL(DC)} or the falling edge of DQ that crosses V_{IH(DC)} to V_{REF} of DQS.
- Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH(AC)} or the falling edge of CMD/ADDR that crosses V_{IL(AC)} to V_{REF} of CLK.
- Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL(DC)} or the falling edge of CMD/ADDR that crosses V_{IH(DC)} to V_{REF} of CLK.

Table 26: DDR3 Interface Switching Characteristics (800 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{DQVALID}^{(2)}$	Input data valid window	500	–	ps
$T_{DQDS}^{(3)}$	Output DQ to DQS skew	232	–	ps
$T_{DQDH}^{(4)}$	Output DQS to DQ skew	401	–	ps
T_{DQSS}	Output clock to DQS skew	–0.10	0.06	T_{CK}
$T_{CACK}^{(5)}$	Command/address output setup time with respect to CLK	722	–	ps
$T_{CKCA}^{(6)}$	Command/address output hold time with respect to CLK	882	–	ps

Notes:

1. Recommended $V_{CCO_DDR} = 1.5V \pm 5\%$.
2. Measurement is taken from V_{REF} to V_{REF} .
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}(AC)$ or the falling edge of DQ that crosses $V_{IL}(AC)$ to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}(DC)$ or the falling edge of DQ that crosses $V_{IH}(DC)$ to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}(AC)$ or the falling edge of CMD/ADDR that crosses $V_{IL}(AC)$ to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}(DC)$ or the falling edge of CMD/ADDR that crosses $V_{IH}(DC)$ to V_{REF} of CLK.

Table 27: DDR3L Interface Switching Characteristics (1066 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{DQVALID}^{(2)}$	Input data valid window	450	–	ps
$T_{DQDS}^{(3)}$	Output DQ to DQS skew	189	–	ps
$T_{DQDH}^{(4)}$	Output DQS to DQ skew	267	–	ps
T_{DQSS}	Output clock to DQS skew	–0.13	0.04	T_{CK}
$T_{CACK}^{(5)}$	Command/address output setup time with respect to CLK	410	–	ps
$T_{CKCA}^{(6)}$	Command/address output hold time with respect to CLK	629	–	ps

Notes:

1. Recommended $V_{CCO_DDR} = 1.35V \pm 5\%$.
2. Measurement is taken from V_{REF} to V_{REF} .
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}(AC)$ or the falling edge of DQ that crosses $V_{IL}(AC)$ to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}(DC)$ or the falling edge of DQ that crosses $V_{IH}(DC)$ to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}(AC)$ or the falling edge of CMD/ADDR that crosses $V_{IL}(AC)$ to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}(DC)$ or the falling edge of CMD/ADDR that crosses $V_{IH}(DC)$ to V_{REF} of CLK.

Table 28: DDR3L Interface Switching Characteristics (800 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{DQVALID}^{(2)}$	Input data valid window	500	–	ps
$T_{DQDS}^{(3)}$	Output DQ to DQS skew	321	–	ps
$T_{DQDH}^{(4)}$	Output DQS to DQ skew	380	–	ps
T_{DQSS}	Output clock to DQS skew	–0.12	0.04	T_{CK}
$T_{CACK}^{(5)}$	Command/address output setup time with respect to CLK	636	–	ps

Table 28: DDR3L Interface Switching Characteristics (800 Mb/s)⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
T _{CKCA} ⁽⁶⁾	Command/address output hold time with respect to CLK	853	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.35V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 29: LPDDR2 Interface Switching Characteristics (800 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
T _{DQVALID} ⁽²⁾	Input data valid window	500	–	ps
T _{DQDS} ⁽³⁾	Output DQ to DQS skew	196	–	ps
T _{DQDH} ⁽⁴⁾	Output DQS to DQ skew	328	–	ps
T _{DQSS}	Output clock to DQS skew	0.90	1.06	T _{CK}
T _{CACK} ⁽⁵⁾	Command/address output setup time with respect to CLK	202	–	ps
T _{CKCA} ⁽⁶⁾	Command/address output hold time with respect to CLK	353	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 30: LPDDR2 Interface Switching Characteristics (400 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
T _{DQVALID} ⁽²⁾	Input data valid window	500	–	ps
T _{DQDS} ⁽³⁾	Output DQ to DQS skew	664	–	ps
T _{DQDH} ⁽⁴⁾	Output DQS to DQ skew	766	–	ps
T _{DQSS}	Output clock to DQS skew	0.90	1.06	T _{CK}
T _{CACK} ⁽⁵⁾	Command/address output setup time with respect to CLK	731	–	ps
T _{CKCA} ⁽⁶⁾	Command/address output hold time with respect to CLK	907	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from V_{REF} to V_{REF}.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 31: DDR2 Interface Switching Characteristics (800 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{DQVALID}^{(2)}$	Input data valid window	500	–	ps
$T_{DQDS}^{(3)}$	Output DQ to DQS skew	147	–	ps
$T_{DQDH}^{(4)}$	Output DQS to DQ skew	376	–	ps
T_{DQSS}	Output clock to DQS skew	–0.07	0.08	T_{CK}
$T_{CACK}^{(5)}$	Command/address output setup time with respect to CLK	732	–	ps
$T_{CKCA}^{(6)}$	Command/address output hold time with respect to CLK	938	–	ps

Notes:

1. Recommended $V_{CCO_DDR} = 1.8V \pm 5\%$.
2. Measurement is taken from V_{REF} to V_{REF} .
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}(AC)$ or the falling edge of DQ that crosses $V_{IL}(AC)$ to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}(DC)$ or the falling edge of DQ that crosses $V_{IH}(DC)$ to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}(AC)$ or the falling edge of CMD/ADDR that crosses $V_{IL}(AC)$ to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}(DC)$ or the falling edge of CMD/ADDR that crosses $V_{IH}(DC)$ to V_{REF} of CLK.

Table 32: DDR2 Interface Switching Characteristics (400 Mb/s)⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{DQVALID}^{(2)}$	Input data valid window	500	–	ps
$T_{DQDS}^{(3)}$	Output DQ to DQS skew	385	–	ps
$T_{DQDH}^{(4)}$	Output DQS to DQ skew	662	–	ps
T_{DQSS}	Output clock to DQS skew	–0.11	0.06	T_{CK}
$T_{CACK}^{(5)}$	Command/address output setup time with respect to CLK	1760	–	ps
$T_{CKCA}^{(6)}$	Command/address output hold time with respect to CLK	1739	–	ps

Notes:

1. Recommended $V_{CCO_DDR} = 1.8V \pm 5\%$.
2. Measurement is taken from V_{REF} to V_{REF} .
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}(AC)$ or the falling edge of DQ that crosses $V_{IL}(AC)$ to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}(DC)$ or the falling edge of DQ that crosses $V_{IH}(DC)$ to V_{REF} of DQS.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}(AC)$ or the falling edge of CMD/ADDR that crosses $V_{IL}(AC)$ to V_{REF} of CLK.
6. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}(DC)$ or the falling edge of CMD/ADDR that crosses $V_{IH}(DC)$ to V_{REF} of CLK.

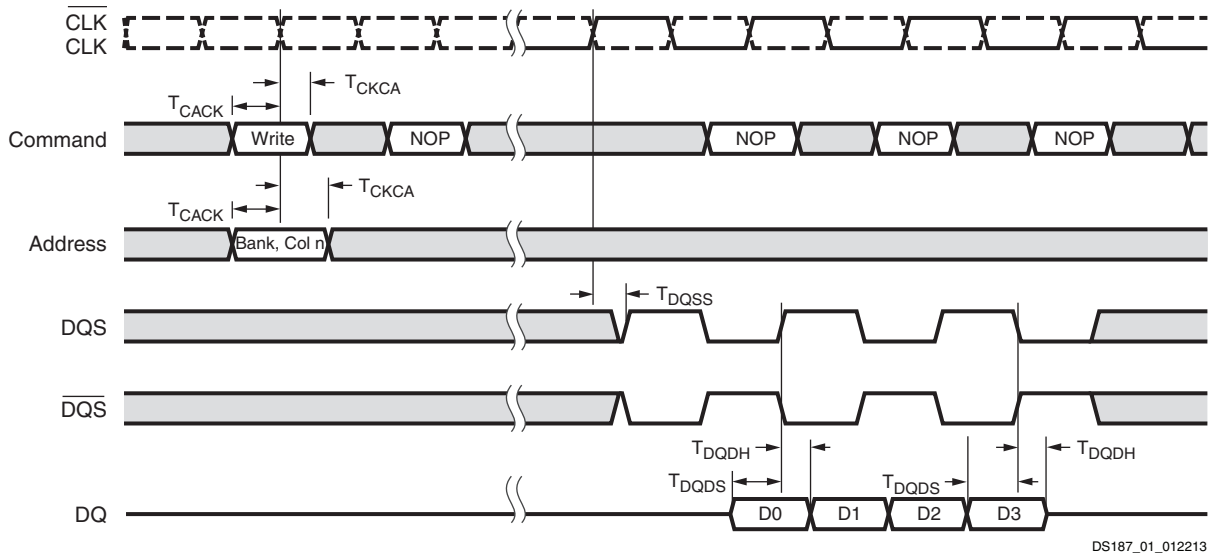


Figure 2: DDR Output Timing Diagram

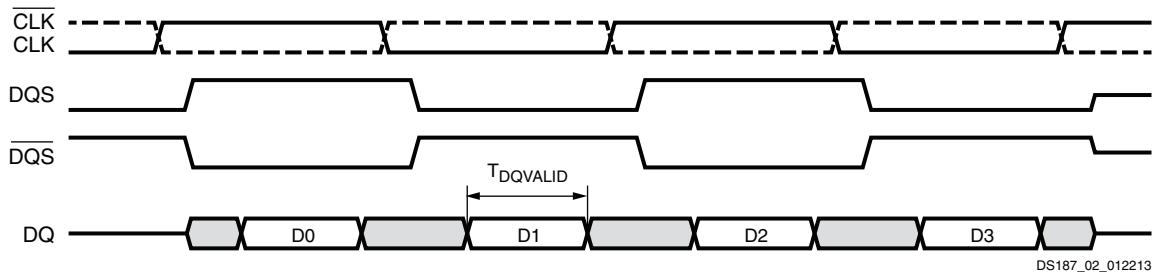


Figure 3: DDR Input Timing Diagram

Static Memory Controller

Table 33: SMC Interface Delay Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Min	Max	Units
T _{NANDDOUT}	NAND_IO output delay from last register to pad	4.12	6.45	ns
T _{NANDALE}	NAND_ALE output delay from last register to pad	5.08	6.33	ns
T _{NANDCLE}	NAND_CLE output delay from last register to pad	4.87	6.40	ns
T _{NANDWE}	NAND_WE_B output delay from last register to pad	4.69	5.89	ns
T _{NANDRE}	NAND_RE_B output delay from last register to pad	5.12	6.44	ns
T _{NANDCE}	NAND_CE_B output delay from last register to pad	4.68	5.89	ns
T _{NANDDIN}	NAND_IO setup time and input delay from pad to first register	1.48	3.09	ns
T _{NANDBUSY}	NAND_BUSY setup time and input delay from pad to first register	2.48	3.33	ns
T _{SRAMA}	SRAM_A output delay from last register to pad	3.94	5.73	ns
T _{SRAMDOUT}	SRAM_DQ output delay from last register to pad	4.66	6.45	ns
T _{SRAMCE}	SRAM_CE output delay from last register to pad	4.57	5.95	ns
T _{SRAMOE}	SRAM_OE_B output delay from last register to pad	4.79	6.13	ns
T _{SRAMBLS}	SRAM_BLS_B output delay from last register to pad	5.25	6.74	ns
T _{SRAMWE}	SRAM_WE_B output delay from last register to pad	5.12	6.48	ns
T _{SRAMDIN}	SRAM_DQ setup time and input delay from pad to first register	1.93	3.05	ns
T _{SRAMWAIT}	SRAM_WAIT setup time and input delay from pad to first register	2.26	3.15	ns
F _{SMC_REF_CLK}	SMC reference clock frequency	–	100	MHz

Notes:

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

Quad-SPI Interfaces

Table 34: Quad-SPI Interface Switching Characteristics

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All ⁽¹⁾⁽²⁾	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF ⁽¹⁾	-0.10 ⁽³⁾	2.30	ns
		30 pF ⁽²⁾	-1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF ⁽¹⁾	2.00	-	ns
		30 pF ⁽²⁾	3.30	-	
$T_{QSPICKD1}$	Input data hold time	15 pF ⁽¹⁾	1.30	-	ns
		30 pF ⁽²⁾	1.50	-	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All ⁽¹⁾⁽²⁾	1	-	$F_{QSPI_REF_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All ⁽¹⁾⁽²⁾	1	-	$F_{QSPI_REF_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF ⁽¹⁾	-	100 ⁽⁴⁾	MHz
		30 pF ⁽²⁾	-	70 ⁽⁴⁾	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All ⁽¹⁾⁽²⁾	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF ⁽¹⁾	-0.10	3.80	ns
		30 pF ⁽²⁾	-1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time	All ⁽¹⁾⁽²⁾	6	-	ns
$T_{QSPICKD2}$	Input data hold time	All ⁽¹⁾⁽²⁾	12.5	-	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All ⁽¹⁾⁽²⁾	1	-	$F_{QSPI_REF_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All ⁽¹⁾⁽²⁾	1	-	$F_{QSPI_REF_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All ⁽¹⁾⁽²⁾	-	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI_REF_CLK}$	Quad-SPI reference clock frequency	All ⁽¹⁾⁽²⁾	-	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. The $T_{QSPICKO1}$ is an effective value. Use it to compute the available memory device input setup and hold timing budgets based on the given device clock-out duty-cycle limits.
4. Requires appropriate component selection/board design.

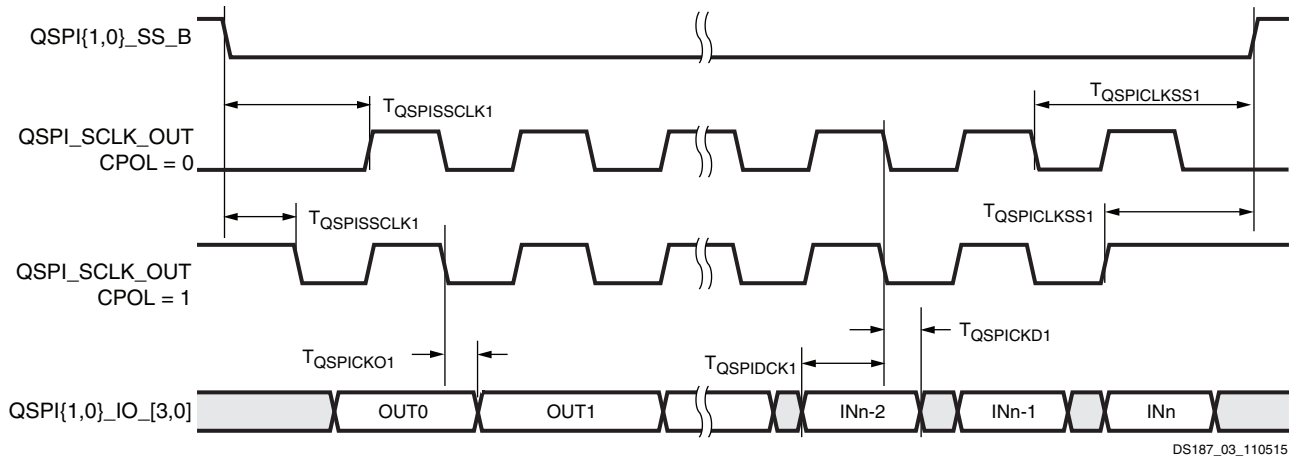


Figure 4: Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram

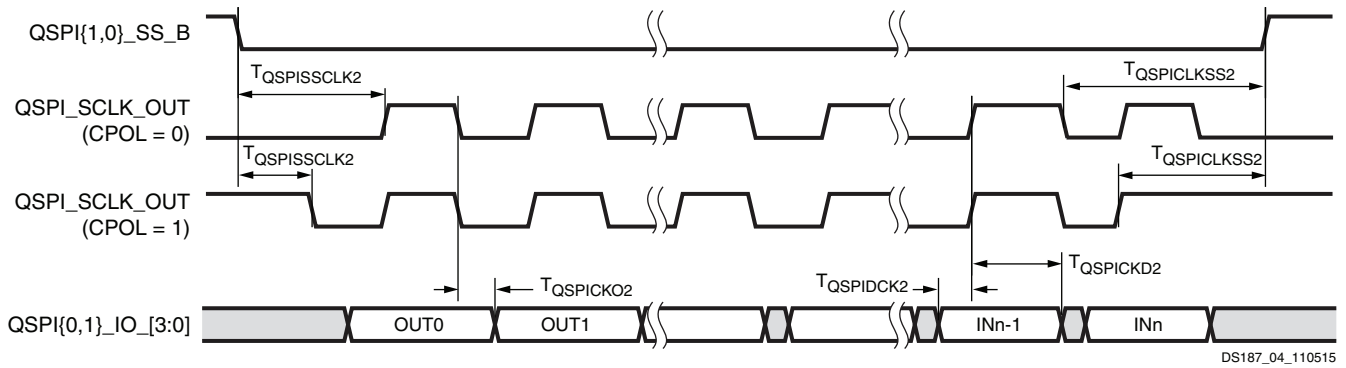


Figure 5: Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram

ULPI Interfaces

Table 35: ULPI Interface Clock Receiving Mode Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	3.00	–	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	1.00	–	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs	1.70	–	8.86	ns
$F_{ULPICLK}$	ULPI device clock frequency	–	60	–	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, 60 MHz device clock frequency.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

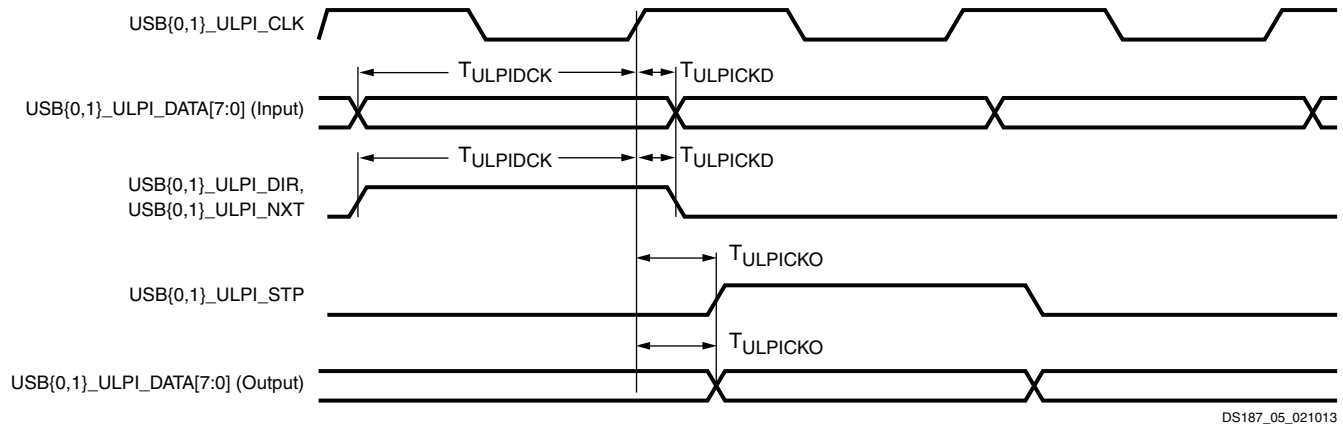


Figure 6: ULPI Interface Timing Diagram