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8-Bit

SAL-XC866

8-Bit Single-Chip Microcontroller

Data Sheet

V1.1 2012-12

Microcontrollers

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8-Bit

SAL-XC866

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Data Sheet
V1.1 2012-12

Microcontrollers

SAL-XC866 Data Sheet
Revision History: **2012-12**   V1.1

Previous Version: V1.0 2011-02

Page	Subjects (major changes since last revision)
-	Removed the "preliminary" wording from the data sheet.

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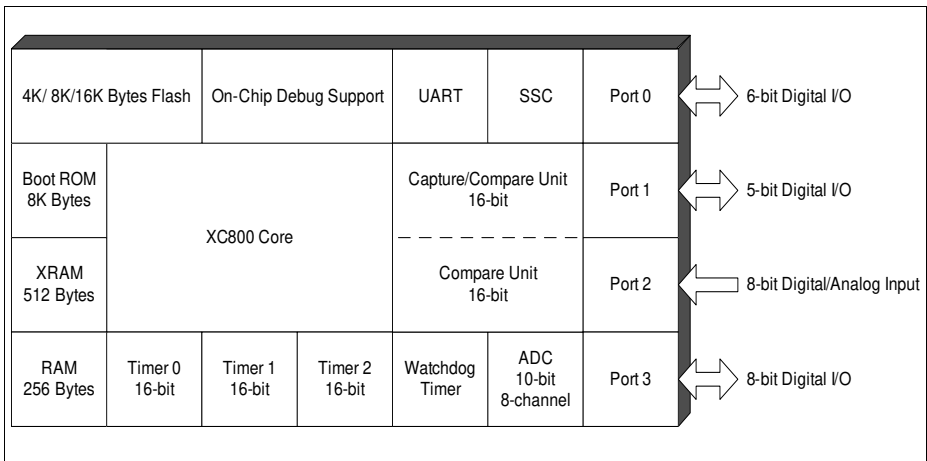## Table of Contents   Page

8-Bit Single-Chip Microcontroller **SAL-XC866**
XC800 Family

1 Summary of Features

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM
  - 256 bytes of RAM
  - 512 bytes of XRAM
  - 4/8/16 Kbytes of Flash
    (includes memory protection strategy)
- I/O port supply at 3.3 V/5.0 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

(further features are on next page)

4K/ 8K/16K Bytes Flash	On-Chip Debug Support		UART	SSC	Port 0	⟺ 6-bit Digital I/O
Boot ROM 8K Bytes	XC800 Core		Capture/Compare Unit 16-bit		Port 1	⟺ 5-bit Digital I/O
XRAM 512 Bytes			Compare Unit 16-bit		Port 2	⟸ 8-bit Digital/Analog Input
RAM 256 Bytes	Timer 0 16-bit / Timer 1 16-bit / Timer 2 16-bit		Watchdog Timer	ADC 10-bit 8-channel	Port 3	⟺ 8-bit Digital I/O

Figure 1   SAL-XC866 Functional Units

Features (continued):

- Reset generation
  – Power-On reset
  – Hardware reset
  – Brownout reset for core logic supply
  – Watchdog timer reset
  – Power-Down Wake-up reset
- On-chip OSC and PLL for clock generation
  – PLL loss-of-lock detection
- Power saving modes
  – slow-down mode
  – idle mode
  – power-down mode with wake-up capability via RXD or EXINT0
  – clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Four ports
  – 19 pins as digital I/O
  – 8 pins as digital/analog input
- 8-channel, 10-bit ADC
- Three 16-bit timers
  – Timer 0 and Timer 1 (T0 and T1)
  – Timer 2
- Capture/compare unit for PWM signal generation (CCU6)
- Full-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- On-chip debug support
  – 1 Kbyte of monitor ROM (part of the 8-Kbyte Boot ROM)
  – 64 bytes of monitor RAM
- PG-TSSOP-38 pin package
- Temperature range T_A:
  – SAL (-40 to 150 °C)

SAL-XC866 Variant Devices

The SAL-XC866 product family features devices with different configurations and program memory sizes, offering cost-effective solution for different application requirements.

The list of SAL-XC866 devices and their differences are summarized in **Table 1**.

Table 1   Device Summary

Device Type	Device Name	Power Supply (V)	P-Flash Size (Kbytes)	D-Flash Size (Kbytes)	LIN BSL Support
Flash[1]	SAL-XC866L-4FRA	5.0	12	4	Yes
	SAL-XC866L-2FRA	5.0	4	4	Yes
	SAL-XC866L-4FRA	3.3	12	4	Yes
	SAL-XC866L-2FRA	3.3	4	4	Yes

[1] The flash memory (P-Flash and D-Flash) can be used for code or data.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

• The derivative itself, i.e. its function set, the temperature range, and the supply voltage
• the package and the type of delivery

For the available ordering codes for the SAL-XC866, please refer to your responsible sales representative or your local distributor.

As this document refers to all the derivatives, some descriptions may not apply to a specific product. For simplicity all versions are referred to by the term SAL-XC866 throughout this document.

2 General Device Information

2.1 Block Diagram
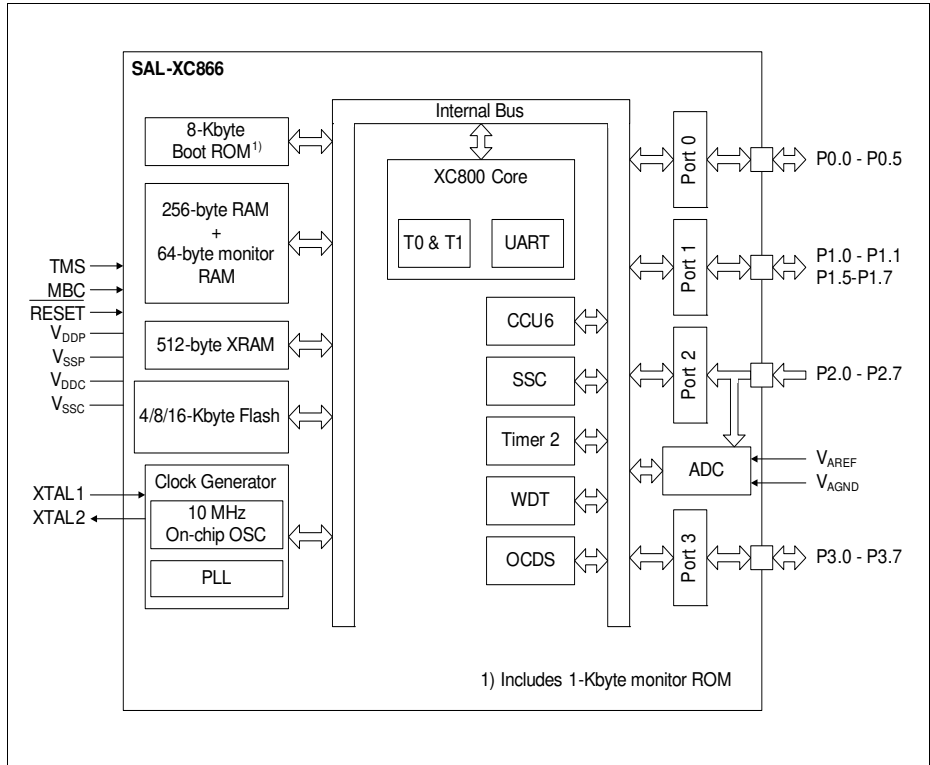
Figure 2   SAL-XC866 Block Diagram

2.2 Logic Symbol
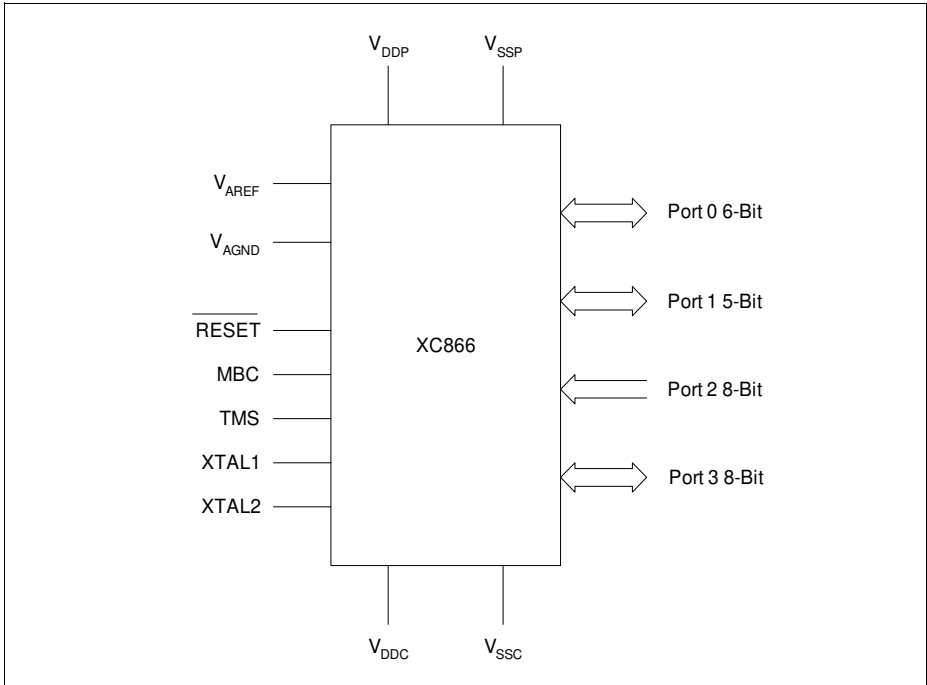
Figure 3   SAL-XC866 Logic Symbol

2.3 Pin Configuration

MBC	1	38	$\overline{RESET}$
P0.3/SCLK_1/COUT63_1	2	37	P3.5/COUT62_0
P0.4/MTSR_1/CC62_1	3	36	P3.4/CC62_0
P0.5/MRST_1/EXINT0_0/COUT62_1	4	35	P3.3/COUT61_0
XTAL2	5	34	P3.2/CCPOS2_2/CC61_0
XTAL1	6	33	P3.1/CCPOS0_2/CC61_2/COUT60_0
V_{SSC}	7	32	P3.0/CCPOS1_2/CC60_0
V_{DDC}	8	31	P3.7/EXINT4/COUT63_0
P1.6/CCPOS1_1/T12HR_0/EXINT6	9	30	P3.6/CTRAP_0
P1.7/CCPOS2_1/T13HR_0	10	29	P1.5/CCPOS0_1/EXINT5/EXF2_0/RXDO_0
TMS	11	28	P1.1/EXINT3/TDO_1/TXD_0
P0.0/TCK_0/T12HR_1/CC61_1/CLKOUT/RXDO_1	12	27	P1.0/RXD_0/T2EX
P0.2/$\overline{CTRAP\_2}$/TDO_0/TXD_1	13	26	P2.7/AN7
P0.1/TDI_0/T13HR_1/RXD_1/EXF2_1/COUT61_1	14	25	V_{AREF}
P2.0/CCPOS0_0/EXINT1/T12HR_2/TCK_1/CC61_3/AN0	15	24	V_{AGND}
P2.1/CCPOS1_0/EXINT2/T13HR_2/TDI_1/CC62_3/AN1	16	23	P2.6/AN6
P2.2/CCPOS2_0/$\overline{CTRAP\_1}$/CC60_3/AN2	17	22	P2.5/AN5
V_{DDP}	18	21	P2.4/AN4
V_{SSP}	19	20	P2.3/AN3

XC866

Figure 4 **SAL-XC866 Pin Configuration, PG-TSSOP-38 Package** (top view)

2.4 Pin Definitions and Functions

Table 2 **Pin Definitions and Functions**

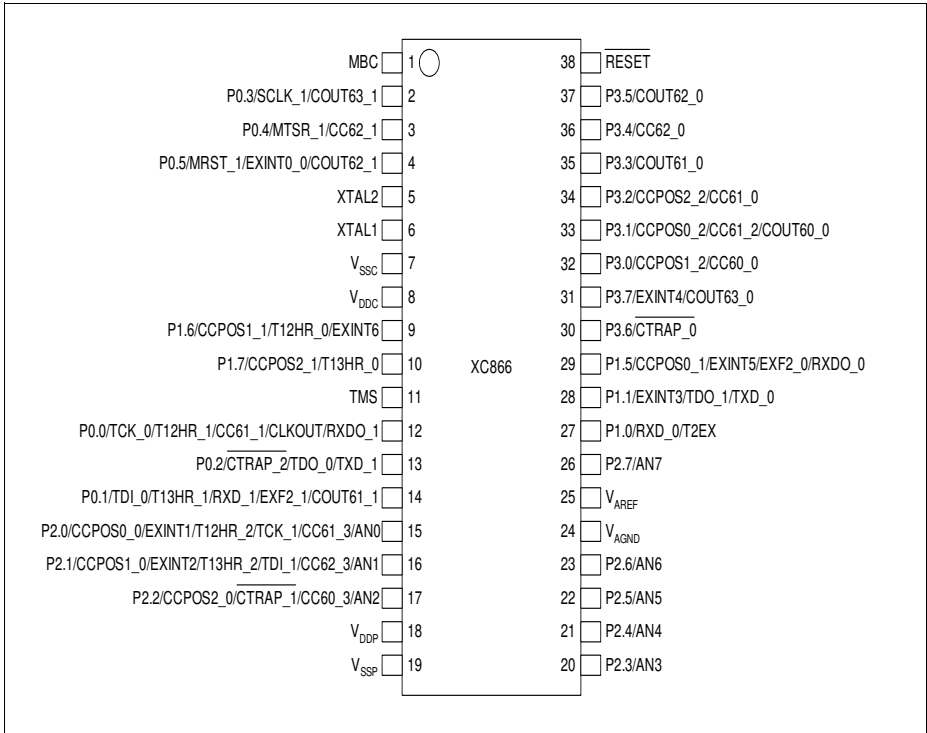| Symbol	Pin Number	Type	Reset State	Function	
P0		I/O		**Port 0** Port 0 is a 6-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, and the SSC.	
P0.0	12		Hi-Z	TCK_0	JTAG Clock Input
				T12HR_1	CCU6 Timer 12 Hardware Run Input
				CC61_1	Input/Output of Capture/Compare channel 1
				CLKOUT	Clock Output
				RXDO_1	UART Transmit Data Output
P0.1	14		Hi-Z	TDI_0	JTAG Serial Data Input
				T13HR_1	CCU6 Timer 13 Hardware Run Input
				RXD_1	UART Receive Data Input
				COUT61_1	Output of Capture/Compare channel 1
				EXF2_1	Timer 2 External Flag Output
P0.2	13		PU	$\overline{CTRAP}$_2	CCU6 Trap Input
				TDO_0	JTAG Serial Data Output
				TXD_1	UART Transmit Data Output/ Clock Output
P0.3	2		Hi-Z	SCK_1	SSC Clock Input/Output
				COUT63_1	Output of Capture/Compare channel 3
P0.4	3		Hi-Z	MTSR_1	SSC Master Transmit Output/ Slave Receive Input
				CC62_1	Input/Output of Capture/Compare channel 2
P0.5	4		Hi-Z	MRST_1	SSC Master Receive Input/ Slave Transmit Output
				EXINT0_0	External Interrupt Input 0
				COUT62_1	Output of Capture/Compare channel 2

Table 2   Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P1		I/O		**Port 1** Port 1 is a 5-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, and the SSC.	
P1.0	27		PU	RXD_0 T2EX	UART Receive Data Input Timer 2 External Trigger Input
P1.1	28		PU	EXINT3 TDO_1 TXD_0	External Interrupt Input 3 JTAG Serial Data Output UART Transmit Data Output/ Clock Output
P1.5	29		PU	CCPOS0_1 EXINT5 EXF2_0 RXDO_0	CCU6 Hall Input 0 External Interrupt Input 5 TImer 2 External Flag Output UART Transmit Data Output
P1.6	9		PU	CCPOS1_1 T12HR_0 EXINT6	CCU6 Hall Input 1 CCU6 Timer 12 Hardware Run Input External Interrupt Input 6
P1.7	10		PU	CCPOS2_1 T13HR_0	CCU6 Hall Input 2 CCU6 Timer 13 Hardware Run Input P1.5 and P1.6 can be used as a software chip select output for the SSC.

Table 2   Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P2		I		**Port 2** Port 2 is an 8-bit general purpose input-only port. It can be used as alternate functions for the digital inputs of the JTAG and CCU6. It is also used as the analog inputs for the ADC.	
P2.0	15		Hi-Z	CCPOS0_0	CCU6 Hall Input 0
				EXINT1	External Interrupt Input 1
				T12HR_2	CCU6 Timer 12 Hardware Run Input
				TCK_1	JTAG Clock Input
				CC61_3	Input of Capture/Compare channel 1
				AN0	Analog Input 0
P2.1	16		Hi-Z	CCPOS1_0	CCU6 Hall Input 1
				EXINT2	External Interrupt Input 2
				T13HR_2	CCU6 Timer 13 Hardware Run Input
				TDI_1	JTAG Serial Data Input
				CC62_3	Input of Capture/Compare channel 2
				AN1	Analog Input 1
P2.2	17		Hi-Z	CCPOS2_0	CCU6 Hall Input 2
				$\overline{CTRAP\_1}$	CCU6 Trap Input
				CC60_3	Input of Capture/Compare channel 0
				AN2	Analog Input 2
P2.3	20		Hi-Z	AN3	Analog Input 3
P2.4	21		Hi-Z	AN4	Analog Input 4
P2.5	22		Hi-Z	AN5	Analog Input 5
P2.6	23		Hi-Z	AN6	Analog Input 6
P2.7	26		Hi-Z	AN7	Analog Input 7

Table 2   Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P3		I		**Port 3** Port 3 is a bidirectional general purpose I/O port. It can be used as alternate functions for the CCU6.	
P3.0	32		Hi-Z	CCPOS1_2	CCU6 Hall Input 1
				CC60_0	Input/Output of Capture/Compare channel 0
P3.1	33		Hi-Z	CCPOS0_2	CCU6 Hall Input 0
				CC61_2	Input/Output of Capture/Compare channel 1
				COUT60_0	Output of Capture/Compare channel 0
P3.2	34		Hi-Z	CCPOS2_2	CCU6 Hall Input 2
				CC61_0	Input/Output of Capture/Compare channel 1
P3.3	35		Hi-Z	COUT61_0	Output of Capture/Compare channel 1
P3.4	36		Hi-Z	CC62_0	Input/Output of Capture/Compare channel 2
P3.5	37		Hi-Z	COUT62_0	Output of Capture/Compare channel 2
P3.6	30		PD	$\overline{\text{CTRAP}\_0}$	CCU6 Trap Input
P3.7	31		Hi-Z	EXINT4	External Interrupt Input 4
				COUT63_0	Output of Capture/Compare channel 3

Table 2 **Pin Definitions and Functions** (cont'd)

Symbol	Pin Number	Type	Reset State	Function
V_{DDP}	18	–	–	**I/O Port Supply (3.3 V/5.0 V)** **Also used by EVR and analog modules.**
V_{SSP}	19	–	–	**I/O Port Ground**
V_{DDC}	8	–	–	**Core Supply Monitor (2.5 V)**
V_{SSC}	7	–	–	**Core Supply Ground**
V_{AREF}	25	–	–	**ADC Reference Voltage**
V_{AGND}	24	–	–	**ADC Reference Ground**
XTAL1	6	I	Hi-Z	**External Oscillator Input** **(NC if not needed)**
XTAL2	5	O	Hi-Z	**External Oscillator Output** **(NC if not needed)**
TMS	11	I	PD	**Test Mode Select**
RESET	38	I	PU	**Reset Input**
MBC[1]	1	I	PU	**Monitor & BootStrap Loader Control**

[1] An external pull-up device in the range of 4.7 kΩ to 100 kΩ is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.

3 Functional Description

3.1 Processor Architecture

The SAL-XC866 is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the SAL-XC866 CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. Access to the Flash memory, however, requires an additional wait state (one machine cycle). The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The SAL-XC866 CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and SFRs. **Figure 5** shows the CPU functional blocks.
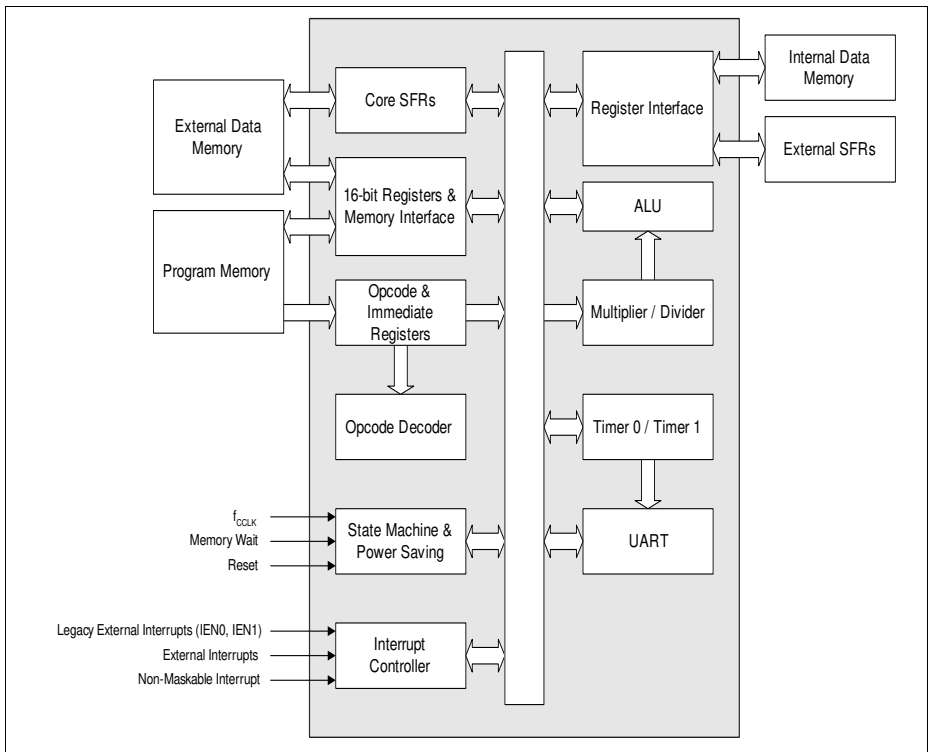
Figure 5 **CPU Block Diagram**

3.2 Memory Organization

The SAL-XC866 CPU operates in the following five address spaces:

• 8 Kbytes of Boot ROM program memory
• 256 bytes of internal RAM data memory
• 512 bytes of XRAM memory
• a 128-byte Special Function Register area
• 4/8/16 Kbytes of Flash program memory

Figure 6 illustrates the memory address spaces of the SAL-XC866-4FR devices.
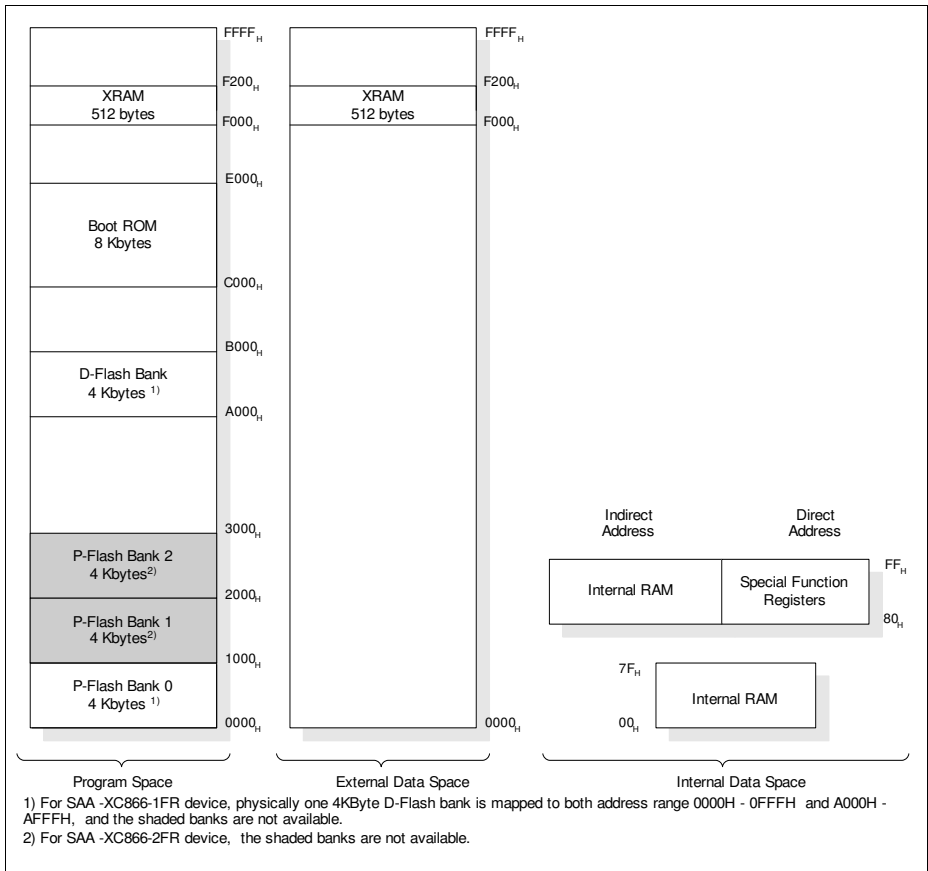

Figure 6   Memory Map of SAL-XC866 Flash Devices

3.2.1 Memory Protection Strategy

The SAL-XC866 memory protection strategy includes:

• Read-out protection: The Flash Memory can be enabled for read-out protection and ROM memory is always protected.
• Program and erase protection: The Flash memory in all devices can be enabled for program and erase protection.

Flash memory protection is available in two modes:

• Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
• Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 3**.

Table 3　　Flash Protection Modes

Mode	0	1
Activation	Program a valid password via BSL mode 6	
Selection	MSB of password = 0	MSB of password = 1
P-Flash contents can be read by	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
P-Flash program and erase	Not possible	Not possible
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash or D-Flash
D-Flash program	Possible	Not possible
D-Flash erase	Possible, on the condition that bit DFLASHEN in register MISC_CON is set to 1 prior to each erase operation	Not possible

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. A password match triggers an automatic erase of the read-protected Flash contents, see **Table 4**, and the programmed password is erased. The Flash protection is then disabled upon the next reset.

For XC866-2FR and XC866-4FR devices:

The selection of protection type is summarized in **Table 4**.

Table 4   Flash Protection Type for XC866-2FR and XC866-4FR devices

PASSWORD	Type of Protection	Flash Banks to Erase when Unprotected
$1XXXXXXX_B$	Flash Protection Mode 1	All Banks
$0XXXXXXX_B$	Flash Protection Mode 0	P-Flash Bank

Although no protection scheme can be considered infallible, the SAL-XC866 memory protection strategy provides a very high level of protection for a general purpose microcontroller.

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 7**.

SYSCON0
**System Control Register 0**   **Reset Value: 00_H**

7	6	5	4	3	2	1	0
		0			1	0	RMAP
		r			rw	r	rw

Field	Bits	Type	Description
RMAP	0	rw	**Special Function Register Map Control** 0 The access to the standard SFR area is enabled. 1 The access to the mapped SFR area is enabled.
1	2	rw	**Reserved** Returns the last value if read; should be written with 1.
0	1,[7:3]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: The RMAP bit must be cleared/set by ANL or ORL instructions. The rest bits of SYSCON0 should not be modified.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.
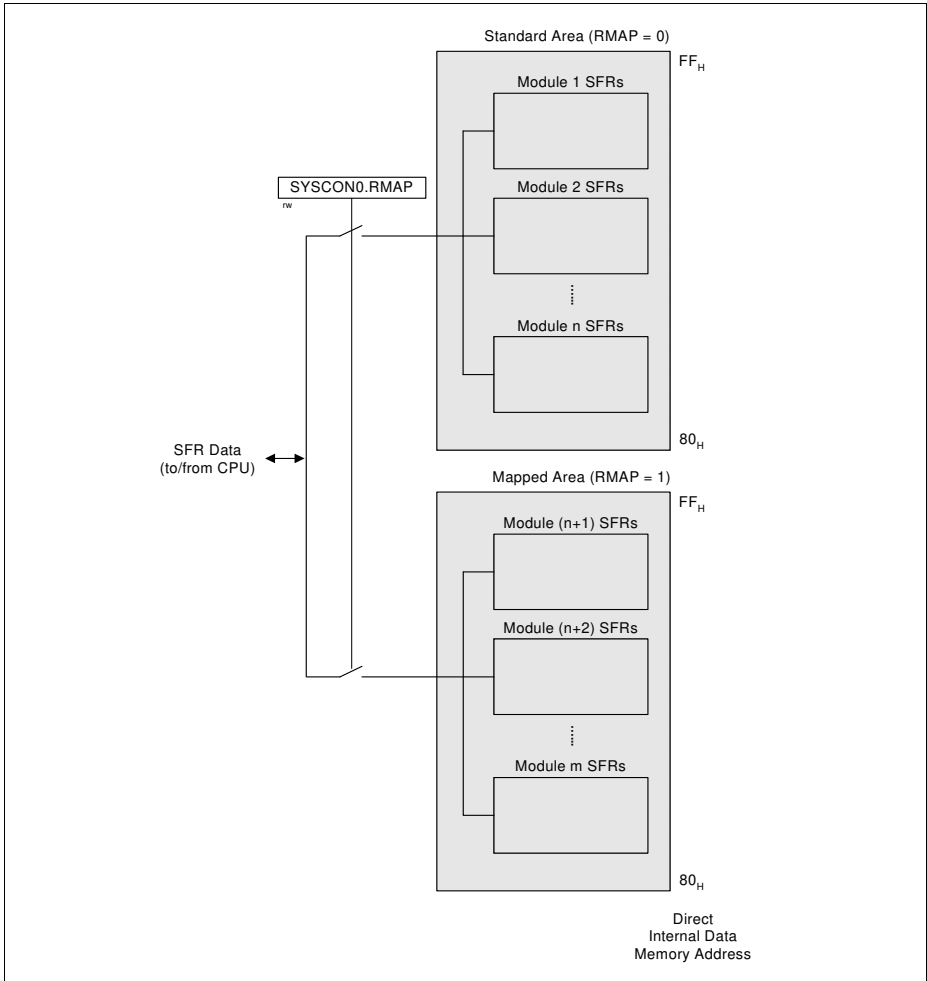
Figure 7   Address Extension by Mapping

3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the SAL-XC866 has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 8**.
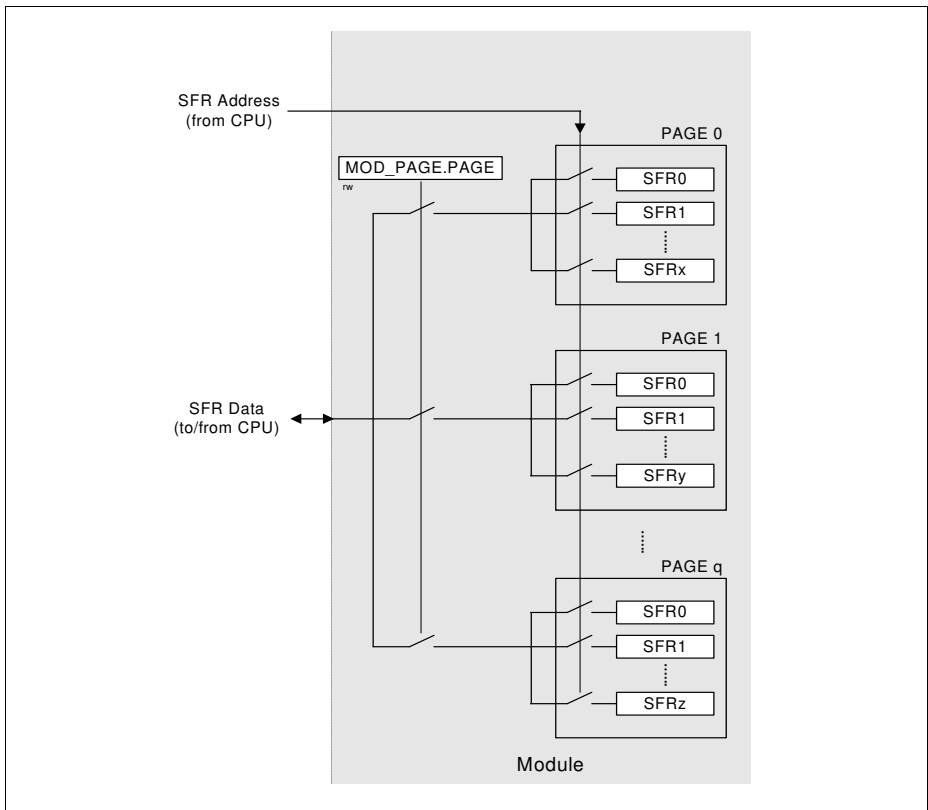
Figure 8   Address Extension by Paging