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Device Package User Guide

UG112 (v3.7) September 5, 2012

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/31/04	1.0	Initial release
02/04/05	1.1	Added Pb-free packaging information.
05/31/06	2.0	Extensive updates and new material added.
05/18/07	3.0	Updated "Material Data Declaration Sheet (MDDS)" in Chapter 1; revised link to "Xilinx Packaging Material Content Data for Standard and PB-Free Packages". Revised "Part Marking" in Chapter 1; added "Ordering Information", "Marking Template", Table 1-1: "Example Part Numbers (FPGA, CPLD, and PROM)", and Table 1-2: "Xilinx Device Marking Definition—Example". Updated "Flip-Chip BGA Packages" in Chapter 1; added content to "Package Construction" to clarify Type I and Type II lid usage. Updated "Thermal Management & Thermal Characterization Methods & Conditions" in Chapter 3; removed "Junction-to-Board Measurement - ΨJB", added link to new "Data Acquisition and Package Thermal Database", added Figure 3-11, page 53, "Package Thermal Data Query for Device-Specific Data" (query tool replaces Table 3-1: "Summary of Thermal Resistance for Packages", which was removed). Updated "Recommended PCB Design Rules for BGA, CSP, and CCGA Packages," page 87; added missing (D) values for CP56 and CP132 packages and corrected SF363 package specification (D) value in Table 5-3, page 88. Added CS48 to Table 5-4, page 88. Updated Table 6-2, page 108 to include MSL ratings for Pb-free packages. Updated "Package Peak Reflow Temperature" in Chapter 7; correction to peak reflow temperature. Added post-wash bake details to "Post Reflow Washing" section.
12/18/08	3.1	Added link to Package Thermal Data Query Tool on xilinx.com. Updated remaining external links. Added Spartan®-3A DSP information to Table 1-1, page 13. Added these packages to Table 2-3, page 36: FG484 and FGG484. Added these packages to Table 5-3, page 88: SFG363, FF676, FGG484, FFG676, FT64 and FTG64. Removed these packages from Table 5-3, page 88: FF896, FFG896, FF1704, FFG1704, FF1696 and FFG1696. Added these packages to Table 5-4, page 88: CS484 and CSG484.

Date	Version	Revision
03/17/09	3.2	Revised "Small Form Factor Packages," page 15 to include description of third template used for marking small form factor packages. Revised "Package Construction," page 20 to describe flip-chip package vent hole locations. Added missing Pb-free packages to Table 1-3, page 27. Revised mass of FG676 and FGG676 packages in Table 1-3, page 27. Added CS484 and CSG484 information to Table 1-3, page 27 and Table 2-3, page 36. Added FF1136 and FFG1136 tray and box information to Table 2-3, page 36. Changed link from DS529 to UG331 in third paragraph of "Data Acquisition and Package Thermal Database," page 52. Added CS484 electrical data to Table 4-1, page 75. Added note to Table 5-3, page 88, referring to UG195. Revised humidity value in third paragraph of "Dry Bake Recommendation and Dry Bag Policy," page 107. Revised humidity value in first and fourth paragraph of "Expiration Date," page 107. Updated links in Table A-1, page 121.
04/23/09	3.3	Added FG400, FGG400, FF323, FFG323, FF324, FFG324, FF665, FFG665, FF676, FFG676, FF1153, FFG1153, FF1156, FFG1156, FF1738, FFG1738, FF1760, and FFG1760 to Table 2-3, page 36. Revised the via land diameters for CF1140, CF1144, and CF1509 packages in Table 5-5, page 89.
06/10/09	3.4	Revised third paragraph of "Package Construction," page 20 about EF flip-chip package epoxy protection. Revised second paragraph of "Post Reflow Washing," page 117 excepting EF packages from cleaning solution/solvent recommendation.
11/06/09	3.5	Added link to MDDS documents under "Material Data Declaration Sheet (MDDS)," page 10. Added FF896, EF1152, EF1704, FF1704, EF668, and EF672 to Table 5-3, page 88. Added EF957 to Table 5-4, page 88.
09/22/10	3.6	Added CS225/CSG225 and CS324/CSG324 in Table 2-3, page 36. Added CF1752 to heading in CF1509 column, and changed "Solder (ball) land pitch" to "Solder (column) land pitch" in Table 5-5, page 89. Added VO48/VOG48 in Table 6-2, page 108.
09/05/12	3.7	Updated "Thermal Management," page 39. Updated "Characterization Methods," page 47 and added "Calibration of System Monitor," page 47. Removed T_t and T_l from and added T_S to "Definition of Terms," page 48. Updated "Junction-to-Case Measurement — qJC," page 49, with JEDEC Standard JESD51-14. Updated document references in "Data Acquisition and Package Thermal Database," page 52. Removed "Junction-to-Top Measurement — Ψ_{JT}" and "Support for Compact Thermal Models (CTM)." Updated note for T_A in "Thermal Data Usage Examples," page 54. Updated "Additional Power Management Options," page 57.

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Chapter 4: Package Electrical Characteristics

Appendix A: Additional Information

Chapter 1

Package Information

Package Overview

Introduction to Xilinx Packaging

Electronic packages are interconnectable housings for semiconductor devices. The major functions of the electronic packages are to provide electrical interconnections between the IC and the board and to efficiently remove heat generated by the device.

Feature sizes are constantly shrinking, resulting in increased number of transistors being packed into the device. Today's submicron technology is also enabling large-scale functional integration and system-on-a-chip solutions. In order to keep pace with these new advancements in silicon technologies, semiconductor packages have also evolved to provide improved device functionality and performance.

Feature size at the device level is driving package feature sizes down to the design rules of the early transistors. To meet these demands, electronic packages must be flexible to address high pin counts, reduced pitch and form factor requirements. At the same time, packages must be reliable and cost effective.

Packaging Technology at Xilinx

Xilinx provides a wide range of leaded and array packaging solutions for our advanced silicon products. Xilinx® advanced packaging solutions include overmolded plastic ball grid arrays (PBGA), small form factor Chip Scale Packages, “Cavity-Down” BGAs, flip-chip BGAs, flip-chip ceramic column grid arrays (CCGA), as well as the newer lead frame packages such as Quad Flat No-Lead (QFN) packages to meet various pin counts and density requirements. Packages from Xilinx are designed, optimized, and characterized to support the long-term mechanical reliability requirements as well as to support the cutting-edge electrical and thermal performance requirements for our high-speed advanced FPGA products.

Pb-free Packaging Solutions from Xilinx

Xilinx also develops packaging solutions that are safer for the environment. Today, standard packages from Xilinx do not contain substances that are identified as harmful to the environment including cadmium, hexavalent chromium, mercury, PBB, and PBDE. Pb-free solutions take that one step further and also do not contain lead (Pb). This makes Pb-free solutions from Xilinx RoHS (Reduction of Hazardous Substances) compliant. Pb-free packages from Xilinx are also JEDEC J-STD-020 compliant, meaning that the packages are made to be more robust so they are capable of withstanding higher reflow temperatures. Xilinx is now ready to support the industry requirements for Pb-free packaging solutions.

Package Drawings

Package drawings are mechanical specifications that include exact dimensions for the placement of pins, height of the package, and related information.

Package drawings are available online at http://www.xilinx.com/support/documentation/package_specifications.htm.

Material Data Declaration Sheet (MDDS)

The MDDS template used by Xilinx is based on the Electronic Industries Alliance (EIA) September 19, Material Composition Declaration Guide dated September 19, 2003 for Level A and Level B materials of interest.

As per EIA, "Level A" List is composed of materials and substances subject to currently enacted legislation that:

a. Prohibits their use and/or marketing
b. Restricts their use and/or marketing
c. Requires reporting or results in other regulatory effect.

As per EIA, "Level B" List is composed of materials and substances that the industry has determined relevant for disclosure because they meet one or more of the following criteria:

a. Precious materials/substances that provide economic value for end-of-life management purposes
b. Materials/substances that are of significant environmental, health, or safety interest
c. Materials/substances that would trigger hazardous waste management requirements
d. Materials/substances that could have a negative impact on end-of-life management.

See the EIA standard for more specific information.

MDDS documents are available online at http://www.xilinx.com/support/documentation/package_specifications.htm.

Information about Pb-Free and RoHS-compliant products is available at http://www.xilinx.com/system_resources/lead_free.

Package Samples

Xilinx offers two types of non-product-specific package samples that can help develop custom processes and perform board-level tests. These samples can be ordered with ordering codes as detailed below.

Mechanical Samples XCMECH-XXXXX (where XXXXX is the package code of interest)

This part type is used for mechanical evaluations, process setup, etc. Most packages are based on the JEDEC outline, and these parts are at times referred to as "dummy" parts since mechanical samples do not contain a die.

Example:

To order a FG676 package as a mechanical sample (without the die), the part number would be XCMECH-FG676.

Daisy Chain Samples XCDAISY-XXXXX (where XXXXX is the package code of interest)

Use this part type to perform board-based evaluations (such as vibrations and temperature cycles) to see how well the solder balls withstand these mechanical conditions. For Xilinx daisy chain parts (XCDAISY-XXXXX), a specific ball assignment chain is available. If you do not have a board already made, you can use our default chain. You can purchase these parts from Xilinx through standard sales outlets. Xilinx does not support unique chains because these parts do not have the volume to justify the development effort.

Example:

To order a FG676 package in a daisy-chained configuration, the part number would be XCDAISY-FG676.

Specifications and Definitions

Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25 mils, 50 mils, or 100 mils (0.025 in., 0.050 in. or 0.100 in.).

The JEDEC standards for PQFP, HQFP, TQFP, VQFP, CSP, and BGA packages define package dimensions in millimeters. The lead frame packages have lead spacings of 0.5 mm, 0.65 mm, or 0.8 mm. The CSP and BGA packages have ball pitches of 0.5 mm, 0.8 mm, 1.00 mm, or 1.27 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters.

Pressure Handling Capacity

For mounted BGA packages, including flip chips, a direct compressive (non-varying) force applied normally to the lid or top of package with a tool head that coincides with the lid (or is slightly bigger) will not induce mechanical damage to the device including external balls, provided the force is not over 5.0 grams per external ball, and the device and board are supported to prevent any flexing or bowing.

These components are tested in sockets with loads in the 5 to 10 gm/ball range for short durations. Analysis using a 10g/ball (e.g., 10 kg for FF1148) showed little impact on short-term but some creep over time. 20 gm/ball and 45 gm/ball loads at 85°C over a six week period has shown the beginning of bridging of some outer balls; these were static load tests. The component can survive forces greater than the 5 gm limit while in short-term situations. However, sustained higher loads should be avoided (particularly if they are overlaid with thermal or power cycle loads). Within the recommended limits, circuit board needs to be properly supported to prevent any flexing resulting from force application. Any flexing or bowing resulting from such a force can likely damage the package-to-board connections. Besides the damage that can occur from bending, the only major concern is long-term creep and bulging of the solder balls in compression to cause bridging. For the life of a part, staying below the recommended limit will ensure against that remote possibility.

Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100-pin and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

Cavity-Up or Cavity-Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). Called "Cavity-Up," this has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins), copper based BGA packages, and Ceramic Quad Flat Packs are assembled "Cavity-Down," with the die attached to the inside top of the package, for optimal heat transfer to the ambient air. More information on "Cavity-Up" packages and "Cavity-Down" packages can be found in the "Package Technology Descriptions" section.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

Part Marking

Ordering Information

An example of an ordering code for a Xilinx FPGA is XC4VLX60-10FFG668CS2. The ordering code stands for:

XC4VLX – Family (Virtex®-4 LX)

60 – Number of system gates or logic cells (60,000 logic cells)

-10 – Speed grade (-10 speed)

FFG – Package type (Pb-free flip-chip BGA)

668 – number of pins (668 pins)

C – Temperature grade (Commercial)

S2 – Step 2

Other examples are shown in Table 1-1.

Table 1-1: **Example Part Numbers (FPGA, CPLD, and PROM)**

Family	Part Number	Sample Ordering Code
Virtex-5 LX	XC5VLX##	XC5VLX110 -1 FFG676C
Virtex-5 LXT	XC5VLX##T	XC5VLX330T-1FF1738I
Virtex-5 SXT	XC5VSX##T	XC5VSX35T-2FF665C
Virtex-4 LX	XC4VLX##	XC4VLX25 -10 FF668C
Virtex-4 SX	XC4VSX##	XC4VSX55 -11 FF1148C
Virtex-II Pro	XC2VP##	XC2VP7 -7 FG456C
Virtex-II	XC2V##	XC2V1000 -5 FG456C
Virtex-E	XCV##E	XCV300E -6 PQ240C
Virtex	XCV##	XCV300 -6 PQ240C
Spartan®-3	XC3S##	XC3S1000 -4 FG676C
Spartan-3A	XC3S##A	XC3S50A -4 FTG256C
Spartan-3E	XC3S##E	XC3S250E -4 FT256C
Spartan-II	XC2S##	XC2S50 -6 PQ208C
Spartan-IIE	XC2S##E	XC2S50E -6 PQ208C
Spartan-3AN	XC3Sx###AN	XC3S400AN-4FG400I
Spartan-3A DSP	XC3SD####A	XC3SD1800A-4CS484LI
Spartan	XCS##	XCS20 -4 PQ208C
Spartan-XL	XCS##XL	XCS20XL -4 PQ208C
4000E	XC4##E	XC4013E -3 HQ240C
4000XL	XC4##XL	XC4013XL -3 PQ208C
CoolRunner™-II	XC2C##	XC2C256 -7 PQ208C
CoolRunner (XPLA3)	XCR##XL	XCR3512XL -7 PQ208C
9500XV	XC95##XV	XC9536XV -7 VQ44I
9500XL	XC95##XL	XC9572XL -7 TQ100C
9500	XC95##	XC95216 -10 HQ208C

Notes:

1. Automotive parts use “XA” instead of “XC”.
2. QML-certified parts use “XQ” instead of “XC”.
3. Aerospace parts have an “R” after “XQ” instead of “XC”.

Examples

CPLD Ordering Information

An example of an ordering number for a Xilinx CPLD is XC2C256-7PQ108I, and is defined as follows:

XC2C – Family (CoolRunner-II)

256 – Number of macrocells (256 macrocells)

-7 – Speed grade (-7 speed)

PQ – Package type (Plastic Quad Flat Pack)

208 – Number of pins (208 pins)

I – Temperature grade (Industrial)

PROM Ordering Information

An example of an ordering number for a Xilinx PROM is XC18V04VQ44C, and is defined as follows:

XC18V – Family - 1800 (ISP) PROM

04 – PROM size (18V00, 17V00, 1700E/L) or equivalent Spartan-II or Spartan-IIE device (17S00A/XL/L), 4 Mb of storage capacity

VQ – Package type (Plastic Quad Flat Pack)

44 – Number of pins (44 pins)

C – Temperature grade (commercial)

To determine the valid ordering combinations for a given device, consult the device data sheet. Data sheets are available at
http://www.xilinx.com/support/documentation/index.htm

Marking Template

Large Form Factor Packages

On December 26, 1995, Product Change Notice (PCN) 95013 was issued to acknowledge a change to the Xilinx standard for package marking. You can view this notice at

http://www.xilinx.com/support/documentation/customer_notices/pcn95013.pdf

Xilinx part marking follows generalized marking templates that are different for small and large packages. Within each group, some minor variations exist due to device family branding.

The large package template (Figure 1-1) consists of the Xilinx Logo, the family brand logo, and 4 lines of information.

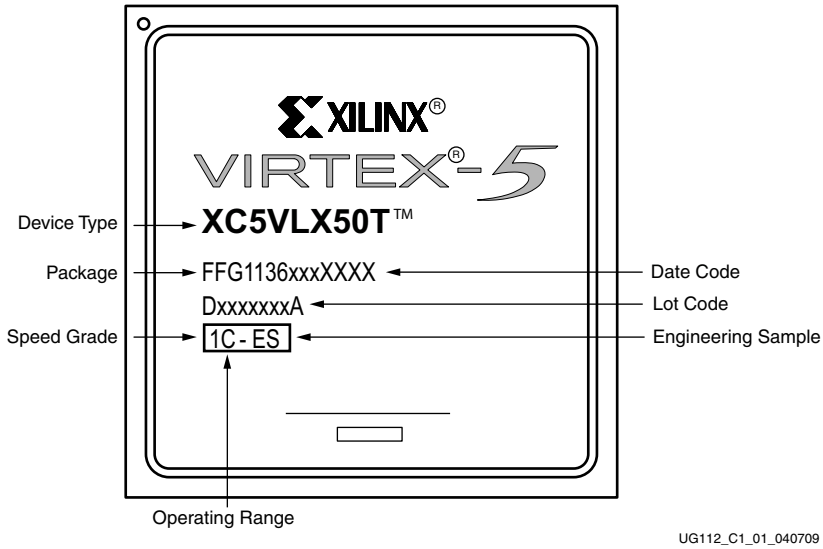

Figure 1-1: **Top Marking (for Large Device Packages)**

Table 1-2: **Xilinx Device Marking Definition—Example**

Item	Description	
Corporate Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.	
Family Brand Logo	Product family name with trademark and trademark-registered status. This line is optional and could appear blank.	
1st Line	Device type.	
2nd Line	Package type and pin count, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A G in the third letter of a package type indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/system_resources/lead_free/index.htm.	
3rd Line	Ten alphanumeric characters for assembly, lot, and step information. The last digit is usually an A or an M if a stepping version does not exist.	
4th Line	Device speed grade and temperature range. If a grade is not marked on the package, the product is considered commercial grade. Other variations for the 4th line:	
	1C-xxxx	The xxxx indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	1C-ES	The ES indicates an Engineering Sample.

Small Form Factor Packages

A second template is used on smaller packages that do not have enough room for six lines of marking. This marking is used mainly for PROMs, and can be found on some medium-size packages as well.

Line 1

Product name code, eight characters. Five or six characters (for example, 1765D) designate the product name representation (usually the name without the “XC”). The name is followed by the PROM package designator (usually a single character). The last letter represents the temperature range (for example, M, I, C).

Line 2

Six numeric characters preceded by the “X” of the Xilinx logo. The first numeric character after the “X” designates the last digit of the year in which the product was assembled. This digit will be the same every 10 years. The next two numeric characters identify the assembly work week. The last three characters are the final three digits of the Assembly number for the lot.

Line 3

This line is usually left blank for customer PROM designator marking.

A third template is used for CPLD and Spartan FPGA small form factor packages. Information is provided on four lines.

Line 1

Product name code (without XC). For example, 9536XL or 3S250E preceded by the "X" of the Xilinx logo.

Line 2

Consists of 11 alphanumeric characters. The first character is a letter that represents the manufacturing location. The next five numeric characters are the lot number. The last four numeric characters are the four digit date code in YYWW format.

Line 3

Indicates the country of origin.

Line 4

Consists of about seven alphanumeric characters. The first two characters are the CPLD or Spartan FPGA package designator and are followed by a three letter mask code. The last two characters are the speed and temperature range.

Package Technology Descriptions

Pb-Free Packaging

Recent legislative directives and corporate driven initiatives around the world have called for the elimination of Pb and other hazardous substances in electronics used in many sectors of the electronics industry. The Pb-free program at Xilinx was established in 1999 as a proactive effort to develop and qualify suitable material sets and processes for Pb-free applications. Xilinx has taken the leadership position by quickly forming partnerships with our customers, suppliers, and participating in industry consortiums to provide technical solutions that are aligned with industry requirements.

Pb-free Material Set

Xilinx has researched alternatives for Pb compounds and has selected matte Sn lead finish for lead-frame packages and SnAgCu solder balls for BGA packages. In addition, suitable material sets are chosen and qualified for higher reflow temperatures (245ºC – 260ºC) that are required by Pb-free soldering processes. Pb-free products from Xilinx are designated

with an additional "G" in the package designator portion of the part number. For example, FGG1152 is the Pb-free version of FG1152.

Features

- RoHS compliant
- Compliant to JEDEC-J-STD-020 standard for peak reflow temperature (245ºC – 260ºC)
- Packages marked with Pb-free identifier

Backward Compatibility

Backward compatibility, as described in this chapter, refers only to the soldering process. Pb-free devices from Xilinx have the same form, fit and function as standard Pb-based products. No changes are required for board design when using Pb-free products from Xilinx. However, finish materials for boards might need to be adjusted.

Lead frame packages (PQG, TQG, VQG, PCG, QFG, etc.) from Xilinx are backward compatible, meaning that the component can be soldered with Sn/Pb solder using Sn/Pb soldering process. Lead-frame packages from Xilinx use a matte Sn plating on the leads which is compatible with both Pb-free soldering alloys and Sn/Pb soldering alloy.

BGA packages (CPG, FTG, FGG, BGG, etc.), however, are not recommended to be soldered with SnPb solder using a Sn/Pb soldering process. The traditional Sn/Pb soldering process usually has a peak reflow temperature of 205ºC - 220ºC. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields might be compromised.

For more information on Xilinx Pb-free solutions, refer to http://www.xilinx.com/system_resources/lead_free/index.htm, and for more information on the Pb-free reflow process, refer to XAPP427.

Tin Whisker Mitigation

Following are some of the efforts Xilinx is making to mitigate tin whiskering in Pb-free lead-frame packages (non-BGA):

a. Tin whisker growth mitigation practices are:
   - Annealing matte tin for 1 hour @ 150°C within 8 hours after tin plating
   - Minimum thicker plating thickness 400 micro inches (10 micro meter)

b. Xilinx assembly subcontractors comply with JEDEC standards for tin whisker test conditions outlined by:
   - JESD22A121.01 (May 2005)
   - JESD201 (March 2006)

c. The lead finish method for Xilinx Pb-Free lead-frame product is:
   - 100% matte tin plating over a bare Cu lead frame

Cavity-Up Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the system circuit board. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields.

The substrate is made of a mutilayer BT (bismaleimide triazene) epoxy-based material. Power and ground pins are grouped together and the signal pins are assigned in the perimeter format for ease of routing on to the board. The package is offered in a die up format and contains a wirebonded device that is covered with a mold compound.

Package Construction

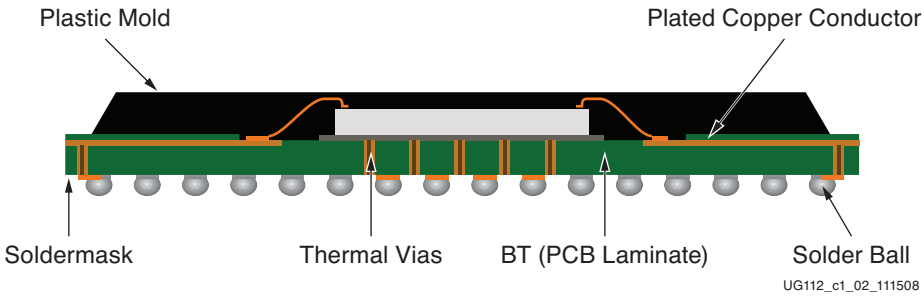

Figure 1-2: **Cavity-Up Ball Grid Array Package**

As shown in the cross section of Figure 1-2, the BGA package contains a wire bonded die on a single-core printed circuit board with an overmold. Beneath the die are the thermal vias which can dissipate the heat through a portion of the solder ball array and ultimately into the power and ground planes of the system circuit board. This thermal management technique provides better thermal dissipation than a standard PQFP package. Metal planes also distribute the heat across the entire package, enabling a 15–20% decrease in thermal resistance to the case.

Key Features/Advantages of Xilinx Cavity-Up BGA Packages

- High board assembly yield since board attachment process is self-centering
- SMT compatible, resulting in minimum capital investment
- Extendable to multichip modules
- Low profile and small footprint
- Improved electrical performance (short wire length)
- Enhanced thermal performance
- Excellent board level reliability

Cavity-Down Thermally Enhanced BGA Packages

Copper-based cavity-down BGAs are high-performance, low-profile packages that offer superior electrical and thermal characteristics. This technology is especially applicable for high-speed, high-power semiconductors such as the Virtex device family.

Package Construction

Figure 1-3 depicts the cross-section of the cavity-down BGA package. It should be noted that this is a solid construction without any internal cavity. The backside die is attached directly to the copper heat spreader and conducts heat out of the package through an epoxy die attach adhesive. The larger the die size and the package body size, the better the thermal performance. The incorporation of the copper heat spreader also results in thermal resistance values that are lowest among the packages offered by Xilinx.

Attached to the heatspreader is a copper stiffener with cavity out to accommodate the die. Along with the heatspreader, this stiffener provides the mechanical flexural strength and warpage control for the package. On the exposed surface of the stiffener is a laminate or build-up structure that contains the circuit traces, the power and ground planes if any, and the sites for the connecting solder balls. The laminate is made of either a glass-reinforced high-glass transition temperature (Tg) bismaleimide triazine (BT) or build-up structure. Xilinx uses laminate with up to four layers, including PWR and GND planes.

Key Features/Advantages of Xilinx Cavity-Down BGAs

- Lowest thermal resistance (θ_{JA} < 13°C/W)
- Superior electrical performance
- Low profile and light weight construction
- Excellent board-level reliability

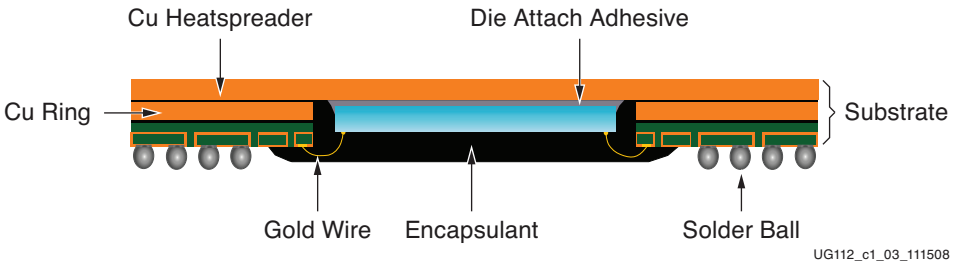

Figure 1-3: **Cavity-Down BGA Package**

Flip-Chip BGA Packages

Flip chip is a packaging interconnect technology that replaces peripheral bond pads of traditional wirebond interconnect technology with area array interconnect technology at the die/substrate interface. The bond pads are either redistributed on the surface of the die or in some very limited cases, they are directly dropped from the core of the die to the surface. Because of this inherent distribution of bond pads on the surface of the device, more bond pads and I/Os can be packed into the device.

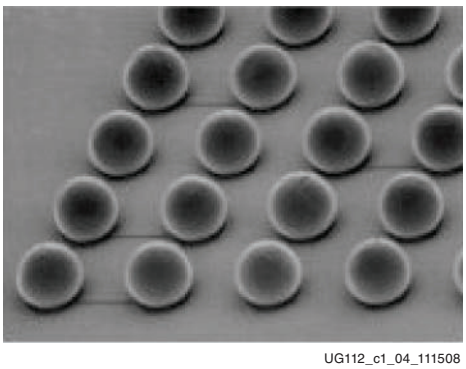

Figure 1-4: **Eutectic Bumps**

The Xilinx flip-chip BGA package is offered for Xilinx high-performance FPGA products. Unlike traditional packaging in which the die is attached to the substrate face up and the connection is made by using wire, the solder bumped die in flip-chip BGA is flipped over and placed face down, with the conductive bumps connecting directly to the matching metal pads on the laminate substrate.

Unlike traditional packaging technology in which the interconnection between the die and the substrate is made possible using wire, flip chip utilizes conductive bumps that are placed directly on the area array pads of the die surface. The area array pads contain wettable metallization for solders (either eutectic or high lead) where a controlled amount of solder is deposited either by plating or screen-printing. These parts are then reflowed to yield bumped dies with relatively uniform solder bumps over the surface of the device. The device is then flipped over and reflowed on a ceramic or organic laminate substrate. The solder material at molten stage is self-aligning and produces good joints even if the chips are placed offset to the substrates. After the die is soldered to the substrate, the gap (standoff) formed between the chip and the substrate is filled with an organic compound called underfill. The underfill is a type of epoxy that helps distribute stresses from these solder joints to the surface of the whole die and hence improve the reliability and fatigue performance of these solder joints.

This interconnect technology has emerged in applications related to high performance communications, networking and computer applications as well as in consumer applications where miniaturization, high I/O count, and good thermal performance are key attributes.

Package Construction

Flip-chip BGA packages for high-performance applications are built on high-density multi-layer organic laminate substrates. Because the flip-chip bump pads are in area array configuration, it requires very fine lines and geometry on the substrates to be able to successfully route the signals from the die to the periphery of the substrates. Multilayer build-up structures offer this layout flexibility on flip-chip packages.

Figure 1-5 and Figure 1-6 show cross-section views of the package constructions. Note that two types of lids are used to assemble flip-chip BGA packages; type I lids (as shown in with flat top) and type II lids (as shown in Figure 1-6 with hat-type top), depending on the package type. Use the package drawing specification (to determine the lid type used on the specific packages, see http://www.xilinx.com/support/documentation/package_specifications.htm.

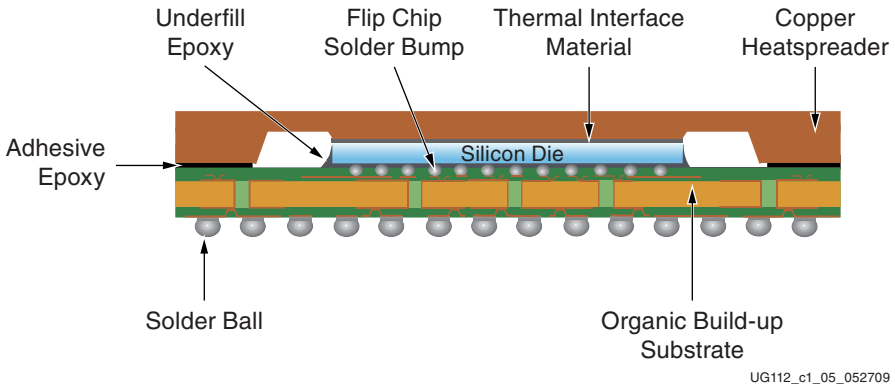

Figure 1-5: **Flip-Chip BGA Package with Type I Lid**

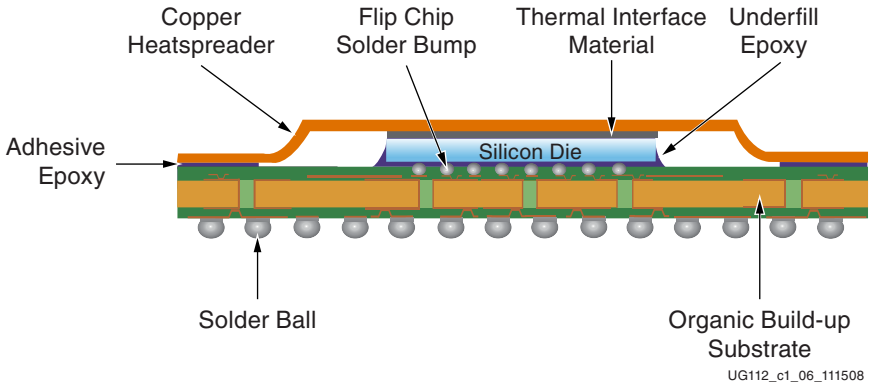

Figure 1-6: **Flip-Chip BGA Package with Type II Lid**

Xilinx flip-chip packages are not hermetically sealed, and exposure to cleaning solvents or excessive moisture during board assembly can pose serious package reliability concerns. Small vents are placed by design between the heatspreader (lid) and the organic substrate to allow for outgassing and moisture evaporation. These vent holes are located in the middle of all four sides of FF flip-chip packages. Solvents or other corrosive chemicals can seep through these vents and attack the organic materials and components inside the package and are strongly discouraged during board assembly of Xilinx flip-chip BGA packages. The only exception would be for EF flip-chip packages in which special epoxy protection is applied to protect against solvents.

Key Features/Advantages of Flip-Chip BGA Packages

- Easy access to core power/ground, resulting in better electrical performance
- Excellent thermal performance (direct heatsinking to backside of the die)
- Higher I/O density since bond pads are in area array format
- Higher frequency switching with better noise control

Assembling Flip-Chip BGAs

The Xilinx flip-chip BGAs conform to JEDEC body sizes and footprint standards. These packages follow the EIA moisture level classification for plastic surface mount components (PSMC). Standard surface mount assembly process should be used with consideration for the slightly higher thermal mass for these packages.

Like other SMT components, flip-chip BGA assembly involves the following process: screen printing, solder reflow, post reflow washing. The following will serve as a guideline on how to assemble flip-chip BGAs onto PCBs.

Screen Printing Machine Parameters

Below is an example of the parameters that were used for the screen printing process. Note that these might not be optimized parameters. Optimized parameters will depend on user's applications and setup.

- Equipment: MPM Ultraprint 2000
- Squeegee Type: Metal
- Squeegee Angle: 45°

- Squeegee Pressure: 24 lbs/sq. in.
- Squeegee Speed: 0.7 in/second
- Print Cycle: One pass
- Stencil Snap Off: 0.10 inches
- Stencil Lift Off Speed: Slow

Screen Printing Process Parameters

- Solder paste: Alpha Metals WS609 (water soluble)
- Stencil aperture: 0.0177 inches diameter
- Stencil thickness: 0.006 inches
- Aperture creation: Laser cut

It is highly recommended to use either a no-clean solder paste or a water soluble solder paste. If cleaning is required, then a water soluble solder paste should be used.

Chip Scale Packages

Chip Scale Packages have emerged as a dominant packaging option for meeting the demands of miniaturization while offering improved performance. Applications for Chip Scale Packages are targeted to portable and consumer products where real estate is of utmost importance, miniaturization is key, and power consumption/dissipation must be low. A Chip Scale Package is defined as a package that fits the definition of being between 1 to 1.2 times the area of the die that the package contains while having a pitch of less than 1 mm.

By employing CSP packages, system designers can dramatically reduce board real estate and increase the I/O counts.

Package Construction

Although there are currently more than 50 different types of CSPs available in the market, Xilinx CSP packages fall into two categories, as shown in Figure 1-7: flex-based substrates and rigid BT-based substrates. Although, both types meet the reliability requirement at the component and board level, BT-based substrate was chosen for the newer devices because of the large vendor base producing/supporting the BT-based substrates.

Key Features/Advantages of CSP Packages

- An extremely small form factor which significantly reduces board real estate for such applications as PCMCIA cards, portable and wireless designs, and PC add-in cards
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other packages
- A very thin, light-weight package

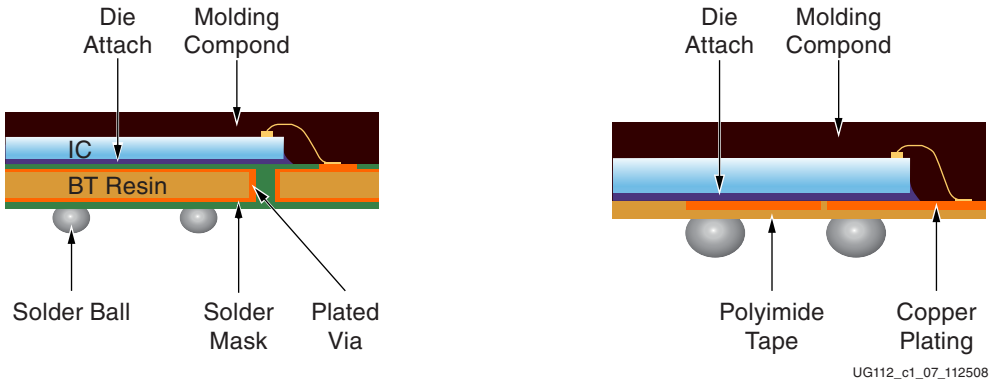

Figure 1-7: **Rigid BT-Based Substrate Chip Scale Packages, Left; Flex-Based Tape Substrate, Right**

Quad Flat No-Lead (QFN) Packages

Quad Flat No-Lead (QFN) or MLF package is a robust and low-profile lead frame-based plastic package that has several advantages over traditional lead frame packages. The exposed die-attach paddle enables efficient thermal dissipation when directly soldered to the PCB. Additionally, this near chip scale package offers improved electrical performance, smaller package size, and an absence of external leads. Since the package has no external leads, coplanarity and bent leads are no longer a concern.

Xilinx Quad Flat No-Lead packages are ideal for portable applications where size, weight, and performance matter.

Package Construction

The QFN is a molded leadless package with land pads on the bottom of the package. Electrical contact to the PCB is made by soldering the land pads to the PCB. The backside of the die is attached to the exposed paddle through the die attach material which is electrically conductive. The exposed pad therefore represents a weak ground and should be left floating or connected to a ground net.

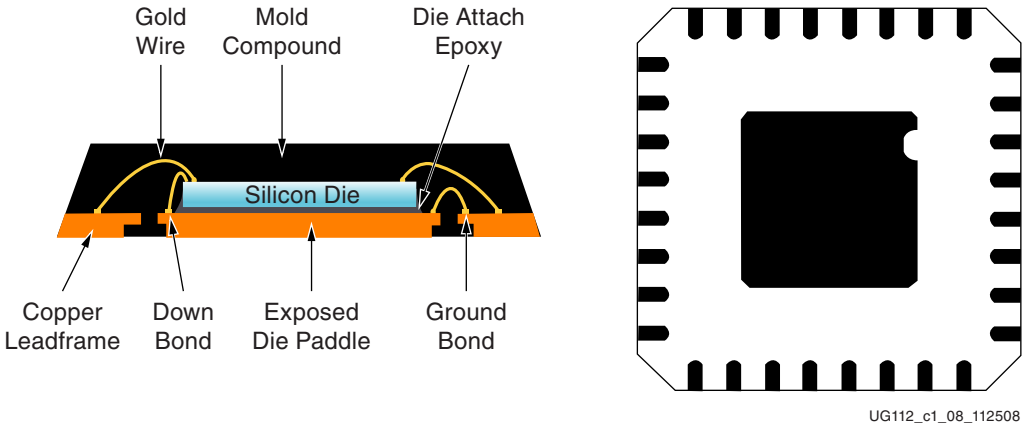

Figure 1-8: **QFN Cross Section (Left) and Bottom View (Right)**

Key Features/Advantages of QFN Packages

- Small size and light weight
- Excellent thermal and electrical performance
- Compatible with conventional SMT processes

Ceramic Column Grid Array (CCGA) Packages

Ceramic Column Grid Array (CCGA) packages are surface-mount-compatible packages that use high-temperature solder columns as interconnections to the board. Compared to the solder spheres, the columns have lower stiffness and provide a higher stand-off. These features significantly increase the reliability of the solder joints. When combined with a high-density, multilayer ceramic substrate, this packaging technology offers a high density, reliable packaging solution. Ceramic offers the following benefits:

Key Features/Advantages of CCGA Packages

- High planarity and excellent thermal stability at high temperature
- CTE matches well with the silicon die
- Low moisture absorption

Xilinx offers 3 different formats of CCGA: “Cavity-Down” wire-bonded CCGA, “Cavity-Up” wire-bonded CCGA, and flip-chip CCGA.

Cavity-Down Wire-Bonded CCGA – CG560 Package Construction

CG560 is offered with the Xilinx XQV1000 and XQVR1000 devices. It is pin-compatible with the plastic BG560 package. Below are additional attributes of CG560.

- Interconnect: 90Pb/10Sn hard solder column interposer, attached with 63Sn/37Pb soft solder.
- Hermetically sealed with eutectic Sn/Au

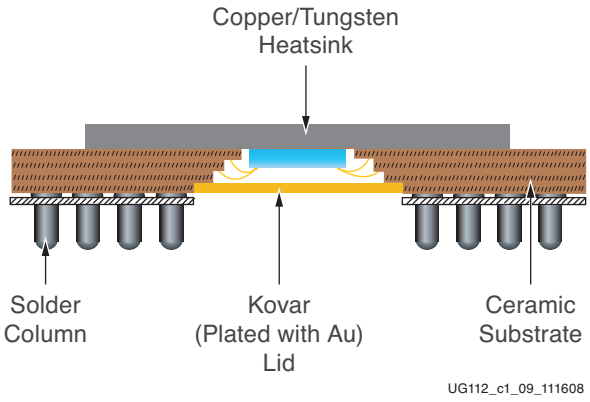

Figure 1-9: **CG560 Package**

Cavity-Up Wire-Bonded BGA – CG717 Package Construction

CG717 is offered with the Xilinx XQ2V3000 and XQR2V3000 devices. It is pin-compatible with the plastic BG728 package. Below are additional attributes of CG717.

- Interconnect: 80Pb/20Sn hard solder column, attached with 63Sn/37Pb soft solder.

- Hermetically sealed with eutectic Sn/Au

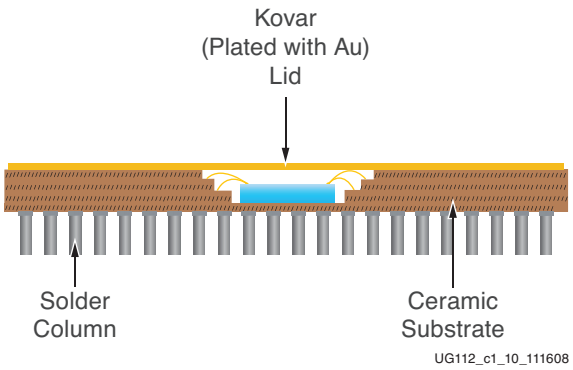

Figure 1-10: **CG717 Package**

Flip-Chip CCGA – CF1144 Package Construction

Flip-Chip CCGA is targeted for applications that require high performance, density, and high reliability. CF1144 is offered with the Xilinx XQ2V6000 and XQR2V6000 devices. The CF1144 package is pin-compatible with the plastic flip-chip FF1152 package. Below are additional attributes of CF1144:

- 95Pb/5Sn flip-chip solder bumps
- 90Pb/10Sn hard solder column

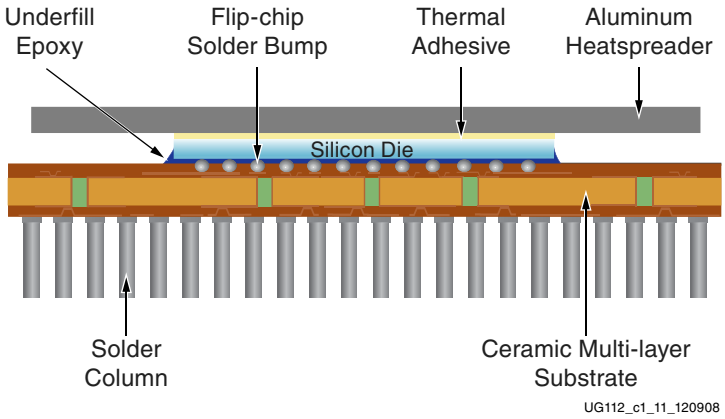

Figure 1-11: **CF1144 Package**

Thermally Enhanced Lead Frame Packaging

Xilinx offers thermally enhanced quad flat pack packages on XC4000 Series devices and some earlier Virtex devices. This section discusses the performance and usage of these packages (designated HQ).

Key Features/Advantages of Thermally Enhanced Lead Frame Packages

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.