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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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XDPL8105 - Digital Flyback Controller IC

XDP™ digital power

Datasheet

About this document

Scope and purpose

This document contains information about Infineon high-performance single-stage digital flyback controller XDPL8105 for LED lighting applications. Features and electrical characteristics are listed and explained.

Intended audience

This document is intended for customers wishing to design high-performance single-stage digital flyback AC-DC converters for LED lighting based on the XDPL8105 controller

Revision History

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev. 1.0, 2016-09-28	

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Overview

Product highlights

- Highly accurate primary side controlled output current (Line/load regulation typical within +/- 3%)
- High power quality (typical PF up to 0.99 and THD < 10%)
- High Efficiency (up to 91%)
- Configurable output current with no BOM change
- Supports universal input voltage (85 – 305 V AC)
- Supports wide output load voltage (up to 4 times of minimum output load voltage)
- Ideal for application with dimming signal from micro-controller on primary side
- Supports fully isolated 0 – 10 V dimming with Infineon CDM10V
- Supports low output current dimming.
- Low standby power

Features

- Single stage QR Flyback with PFC and high precision primary side controlled constant current output
- Excellent line and load regulation
- Supports AC input (45 ~ 65 Hz) and/or DC input voltage operation
- Integrated 600 V startup cell
- Low Bill Of Material (BOM)
- Configurable parameters, e.g. adjustable voltage and current ranges, protection modes
- Supports non-dimmed and/or dimmed applications.
- Intelligent thermal management with adaptive thermal protection

Applications

- Electronic control gear for LED luminaires (5 W to 80 W)

Description

The XDPL8105 is a high performance microcontroller-based digital single-stage flyback controller with power factor correction (PFC) for constant output current applications. The IC is available in a DSO-8 package and supports a wide feature set, requiring a minimum of external components. The digital engine offers the possibility to configure operational parameters and protection modes, which helps to ease the design phase and allows a reduced number of hardware variants in production. Accurate primary side output current control is implemented to eliminate the need for secondary side feedback circuitry.

Table 1

Product Type	Package
XDPL8105	PG-DSO-8

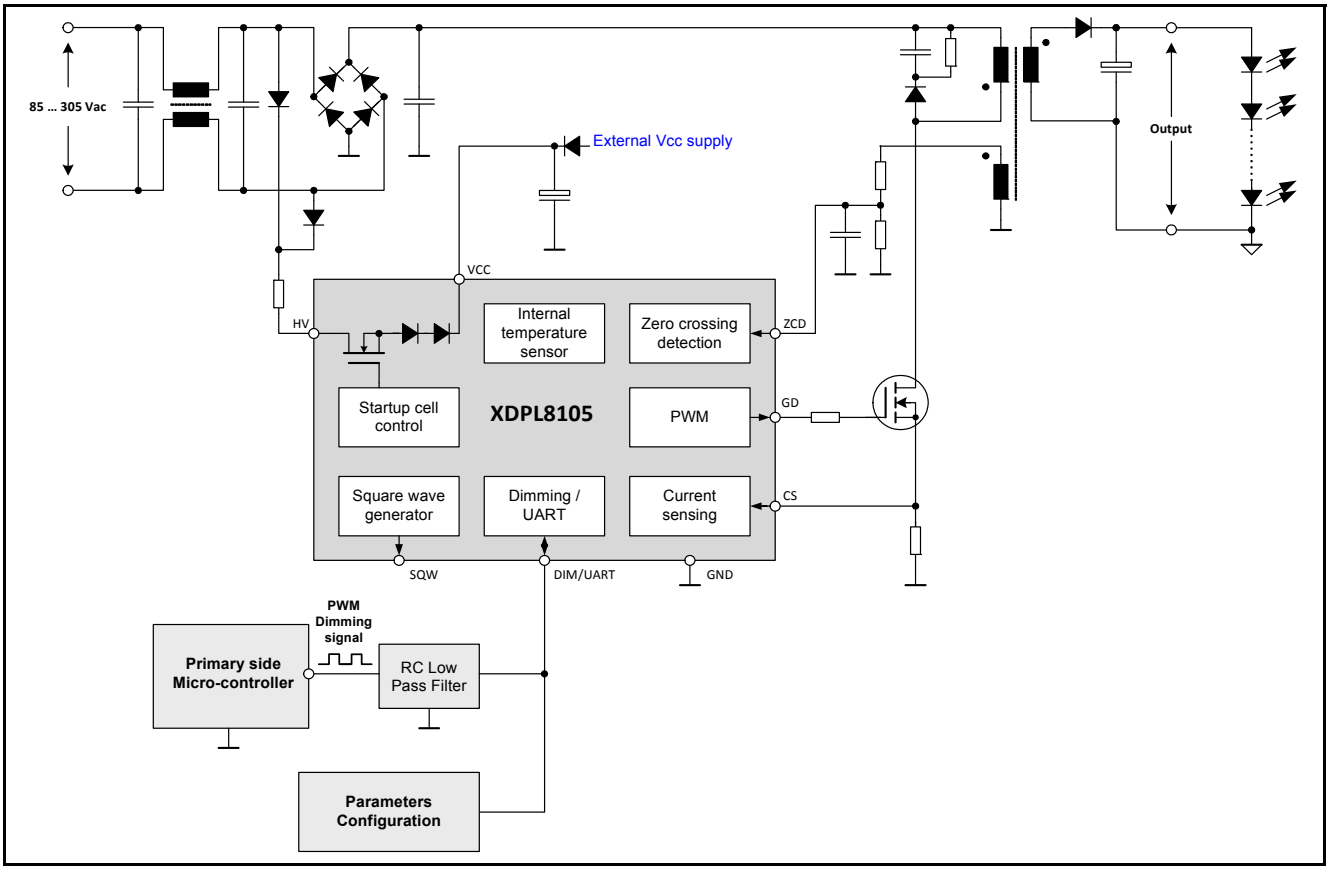

Figure 1 Typical application 1 (Primary side micro-controller dimming)

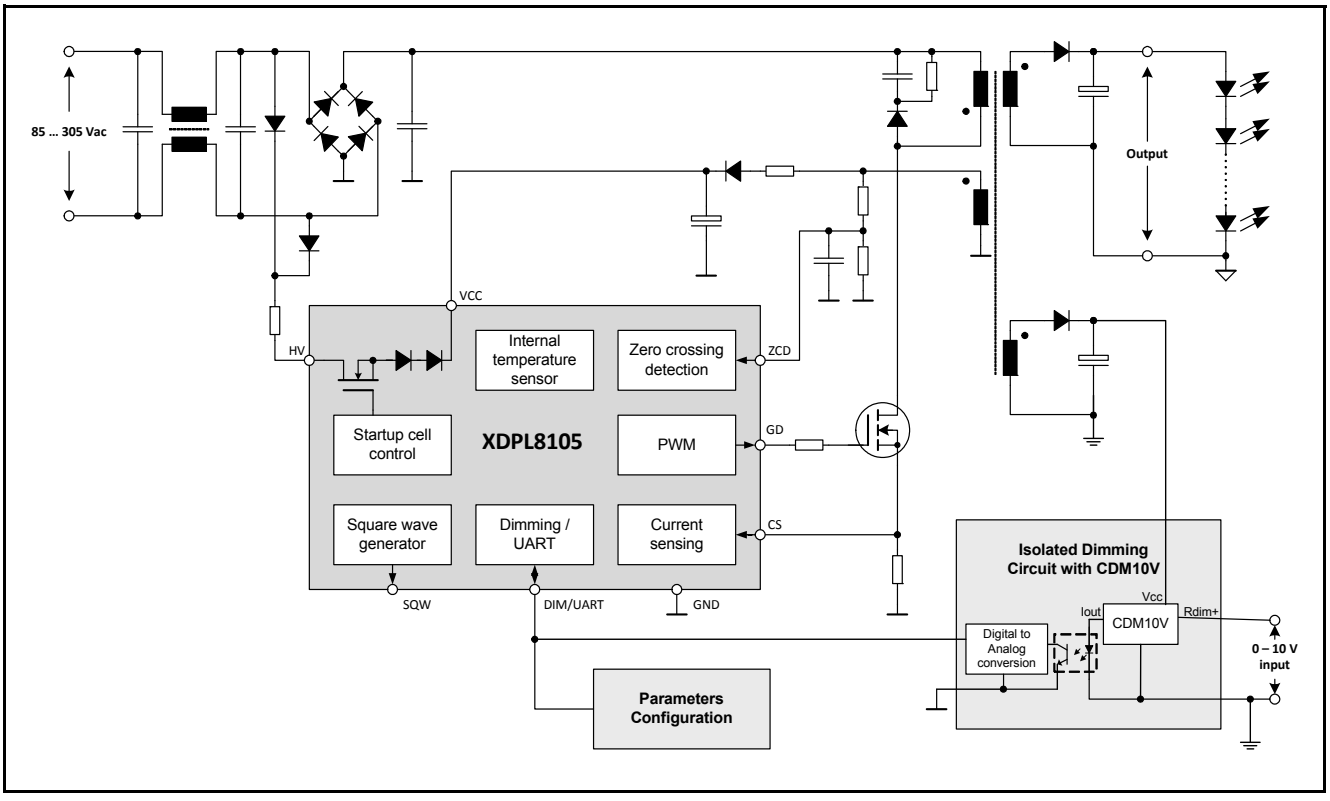

Figure 2 Typical application 2 (Secondary side 0-10V dimming)

1 Pin configuration and description

The pin configuration is shown in **Figure 3**. The pin functions are listed and described in **Table 2**.

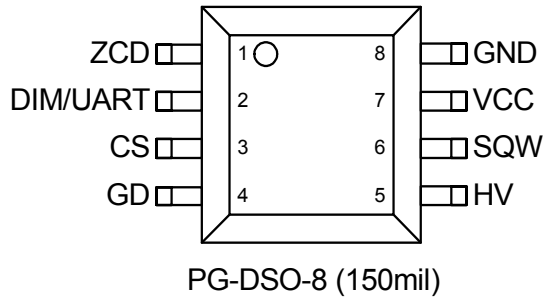

Figure 3 Pin configuration

Table 2 Pin definitions and functions

Symbol	Pin	Type	Function
ZCD	1	I	**Zero crossing detection** Pin ZCD is connected to an auxiliary winding via the resistor divider for zero crossing detection. Output & input voltage are also measured with the sampled positive & negative voltage sensing.
DIM/UART	2	I/O	**Dimming / UART** Shared functioning pin with either as dimming Input or UART configuration. The dimming input voltage, V_{DIM} sensing range is from 0.1 to 2V. Once the pin voltage exceeds 2.2V (for example when the isolated USB interface board is connected to the IC), this pin will function as UART configuration and the IC will stay in non-dimming operation unless it is reset or restarted.
CS	3	I	**Current sense** Pin CS is connected to an external shunt resistor and the source of the power MOSFET.
GD	4	O	**Gate driver** Output signal to drive an external power MOSFET.
HV	5	I	**High voltage** Pin HV is connected to the rectified input voltage via external resistor. An internal 600 V HV startup-cell is used to pre-charge VCC for IC startup once the mains input voltage is applied. Furthermore sampled high voltage sensing is used for synchronization with the input voltage frequency.
SQW	6	O	**Square wave generator** Pin SQW is capable of providing a square wave signal for driving the isolated dimming transformer circuit, if necessary. Otherwise, this signal can be turned off by parameter configuration.
VCC	7	I	**Voltage supply** IC power supply
GND	8	—	**Power and signal ground**

2 Functional description

The functional description provides an overview about the integrated functions and features as well as their relationship. The mentioned parameters and equations are based on typical values at T_A = 25 °C. The corresponding min. and max. values are shown in the electrical characteristics.

2.1 Introduction

The XDPL8105 is a digital AC/DC flyback controller with Power Factor Correction (PFC). The PFC function enables a rectified sinusoidal input current waveform with a power factor typically up to 0.99 and THD < 10% for a wide range of operating conditions. XDPL8105 provides primary side constant output current control that avoids the secondary side control feedback loop circuitry usually needed in isolated power converters. This approach supports a low part count that is necessary to build up the application. XDPL8105 has multi-mode operations and it selects the best mode of operation based on operating conditions. The multi-mode operation will automatically switch between quasi-resonant mode (QRM) and discontinuous mode (DCM) and active burst mode (ABM). In addition, XDPL8105 supports both secondary side 0 - 10 V dimming and primary side micro-controller dimming application. Digital and RF interfaces can be supported by a microcontroller using a digital-to-analog converter.

The XDPL8105 provides a high flexibility in the design-in of the application. A graphic user interface (GUI) tool called .dp Vision supports users to tune a set of configurable parameters. The configuration can be done via a single pin UART interface at pin DIM/UART.

2.2 Controller features

Table 3 gives an overview about the controller features that are described in the mentioned chapters.

Table 3 Controller features

Primary side voltage and current sensing	**Chapter 2.2.1**
Primary side control scheme for output current control	**Chapter 2.2.2**
Power factor correction (PFC)	**Chapter 2.2.3**
Dimming via pin DIM/UART	**Chapter 2.2.4**
Isolated dimming interface with CDM10V (optional)	**Chapter 2.2.5**
Wide output load voltage range circuit (optional)	**Chapter 2.2.6**
Automatic output discharge circuit (optional)	**Chapter 2.2.7**
VCC startup function combined with direct input monitoring	**Chapter 2.2.8**
Configurable soft start and output charging	**Chapter 2.2.9**
Configurable gate voltage rising slope at pin GD (Lower EMI)	**Chapter 2.2.10**

2.2.1 Primary side voltage and current sensing

The XDPL8105 provides a primary side control of the output current by means of measuring the input peak current and measuring the conduction period of the output diode. Input and output voltages are measured at pin ZCD using an external resistor divider and an auxiliary winding of the transformer. The voltage signal V_{AUX} contains the information of the rectified input voltage V_{in} and the output voltage V_{out} at the secondary side. **Figure 4** shows typical current and voltage waveforms of the Quasi-Resonant flyback application.

The following topics are described:

- Input current sensing via pin CS and output current calculation (**Chapter 2.2.1.1**)
- Input voltage sensing via pin ZCD (**Chapter 2.2.1.2**)
- Output voltage sensing via pin ZCD (**Chapter 2.2.1.3**)

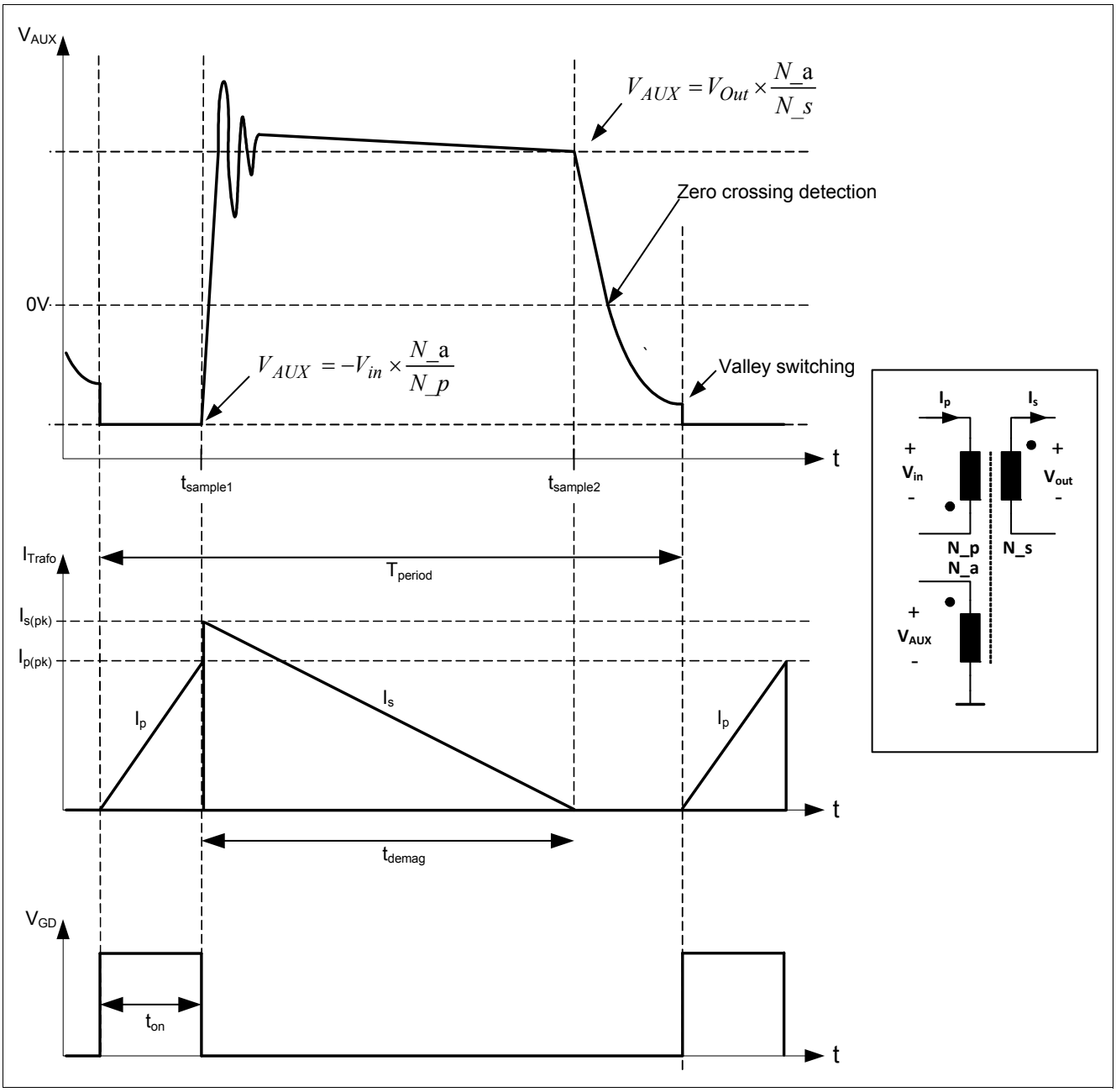

Figure 4 Typical waveforms (Example with QRM valley switching)

2.2.1.1 Input current sensing via pin CS and output current calculation

The output current I_{out} is determined by the primary input peak current $I_{p,pk}$ which is sensed at pin CS at time $t_{sample1}$, by the duration of conduction of the output diode ($t_{sample2}$ - $t_{sample1}$) and by the switching period t_{period}. The result is used for the control loop and for output overcurrent protections (**Chapter 2.3.7**).

2.2.1.2 Input voltage sensing via pin ZCD

The input voltage is measured using current I_{IV} at pin ZCD at time $t_{sample1}$. As the voltage V_{AUX} is a negative voltage, pin ZCD is clamped to a fixed negative voltage V_{INPCLN} (**Figure 5**). The negative current I_{IV} (flowing out of pin ZCD) is proportional to the input voltage. The monitored input voltage is used for input over- and undervoltage protection (**Chapter 2.3.4**).

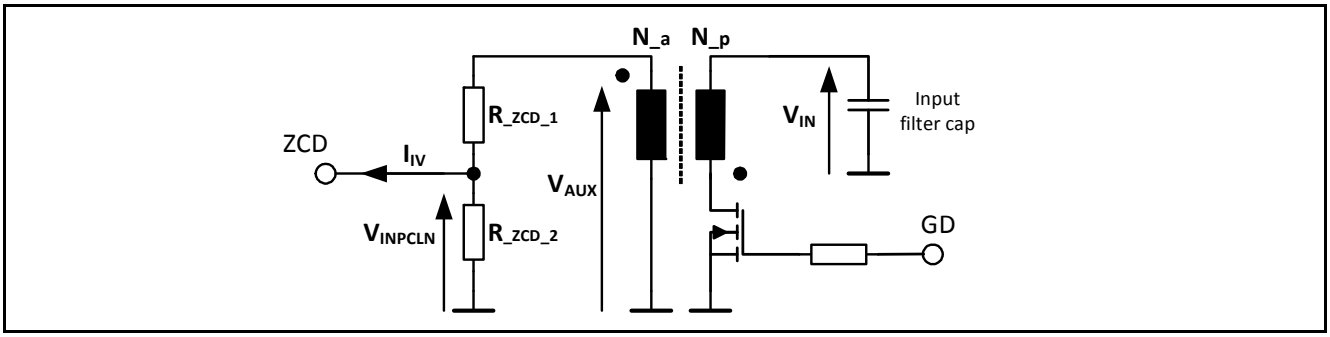

Figure 5 Input voltage sensing via pin ZCD

2.2.1.3 Output voltage sensing via pin ZCD

The output voltage is measured using voltage V_{ZCDSH} at pin ZCD at time $t_{sample2}$ (**Figure 6**). The measured voltage at pin ZCD and the dimensioning of the resistor divider are used to calculate the reflected output voltage at the auxiliary winding. The sensed output voltage is used for output over- and undervoltage protection (**Chapter 2.3.3**). The relation between VCC and ZCD can be decoupled by adding a voltage regulator for VCC (**Chapter 2.2.6**).

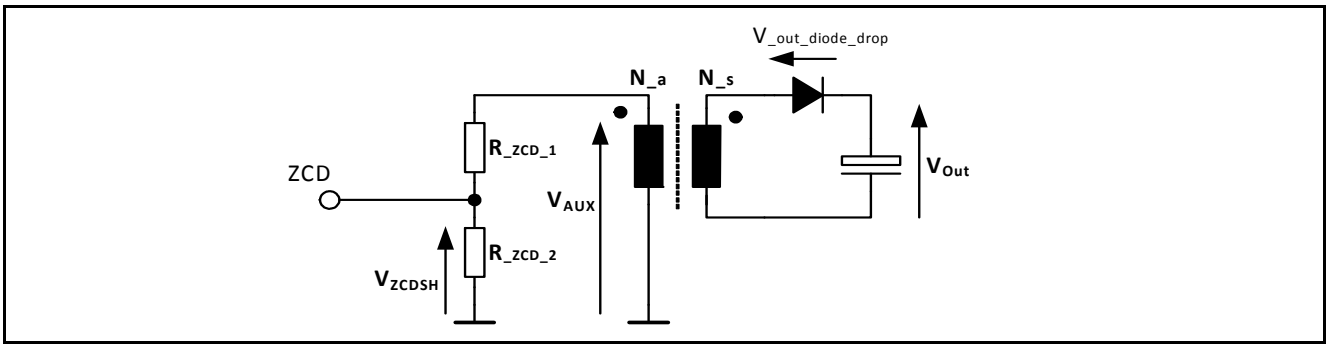

Figure 6 Output voltage sensing via pin ZCD

Note: Please note that the time ($t_{sample2}$ - $t_{sample1}$) has to be longer than 2.0 µs to ensure that the reflected output voltage can be correctly sensed at pin ZCD!

2.2.2 Primary side control scheme for output current control

The basic control scheme for the primary side constant current control is shown in **Figure 7**.

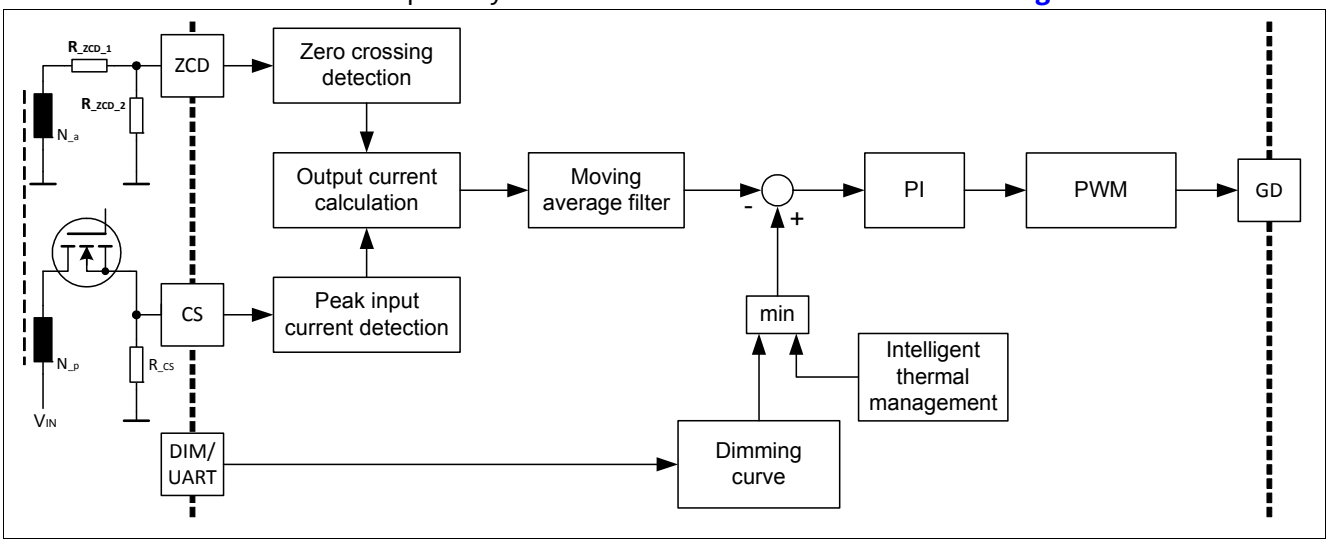

Figure 7 Integrated PI control scheme for output current control

The sampled signal V_{CS} at pin CS and zero crossing detection at pin ZCD are used to estimate the output current I_{out} as described in **Chapter 2.2.1.1**. The internal reference current $I_{\_out\_set}$ is weighted according to thermal management and dimming curve. The average estimated output current is compared with the weighted reference current to generate an error signal. The error signal is fed into a PI regulator to control the PWM at pin GD for the power MOSFET. The coefficients of the PI regulator are configurable.

The PI regulator allows different modes of operation as shown in **Figure 8**:

- Quasi-resonant mode (QRM)
  This mode controls the on-time and maximizes the efficiency by switching on at the 1st valley of the V_{AUX} signal. This ensures zero-current switching with a minimum of switching losses.
- Discontinuous mode (DCM)
  This mode is used if the on-time cannot be reduced further in QRM while the output is being dimmed. The controller will extend the switching period later than the 1st valley to control the output power.
- Active-Burst mode (ABM)
  To extend the dimming range even further, XDPL8105 features an ABM which is automatically aligned with the input frequency to avoid any undesired effects like flicker or shimmer as well as to reduce any audible noise.

The controller will autonomously select the best mode of operation based on operation conditions like input voltage, input frequency and dimming input voltage which defines the output power.

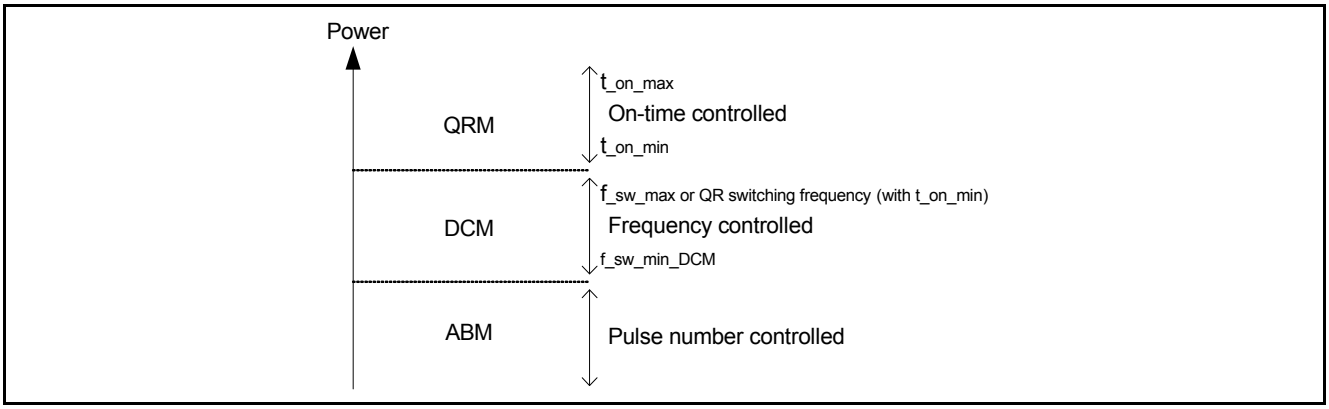

Figure 8 Overview of operation modes

2.2.3 Power factor correction (PFC)

The gate driver GD is used for driving the power MOSFET of the flyback. Constant output current regulation and a sinusoidally shaped input current are achieved by on-time control. The quasi-constant on-time t_{on} ensures high PF and low THD performance. The internal control signal t_{on} is calculated by the digital engine so that the output current is close to the target current (**Chapter 2.2.2**).

Optionally, an enhanced PFC (EPFC) scheme can be enabled to compensate the input current distortion caused by the EMI filter[1]. In this scheme, the on-time is a function of the internal controller signal t_{on}, the input voltage V_{in}, output voltage V_{out}, output current I_{out}, phase angle and a configurable gain parameter ($C_{\_EMI}$) optimizing the input current waveform (**Chapter 2.4**).

2.2.4 Dimming via pin DIM/UART

The voltage sensed at pin DIM/UART is used to determine the output current level. **Figure 9** shows the relation of DIM/UART voltage to the output current target value. Levels of $V_{\_DIM\_min}$ and $V_{\_DIM\_max}$[2] ensure that minimum current $I_{\_out\_dim\_min}$ and maximum current $I_{\_out\_set}$ can always be achieved, making the application robust against dimmer and other component tolerances. The sampled voltage V_{DIM} at pin DIM/UART is digitally filtered to stabilize light output. The XDPL8105 can also be configured to use a linear or a quadratic dimming curve.

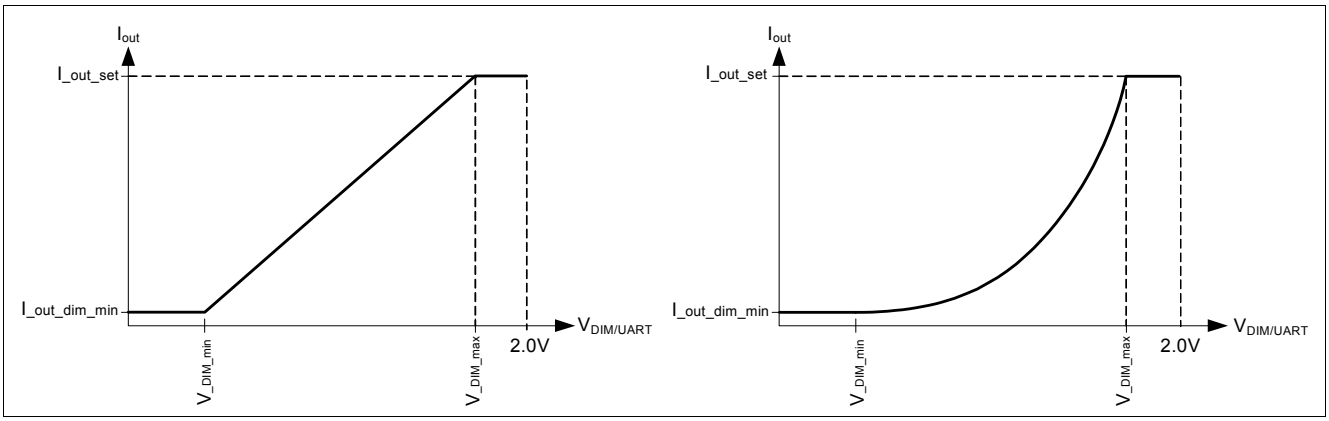

Figure 9 Dimming curves based on pin DIM/UART voltage

1) Patent pending
2) fixed at 1.72V

Optionally, the dim-to-off feature can be enabled by parameter EN_DIM_TO_OFF, so that the output current can be turned off and on with DIM/UART pin voltage of V_DIM_off and V_DIM_on respectively.

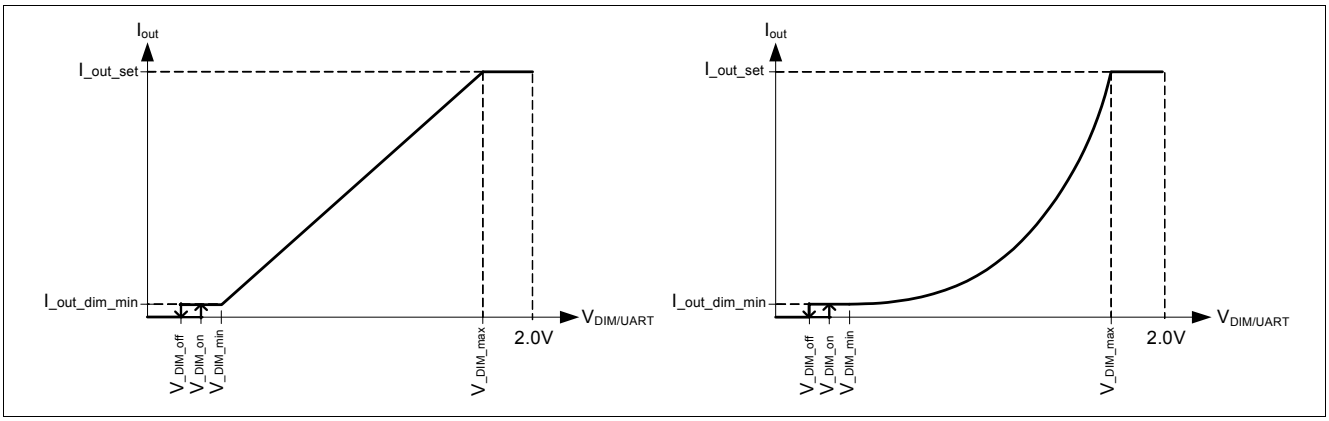

Figure 10 Dimming curves based on pin DIM/UART voltage (with dim-to-off feature enabled)

Note: The dim-to-off feature requires an active voltage source to exit the dim-to-off state.

In some cases where the dimming control circuitry is on the primary side and it is using PWM control, please use the RC low pass filter circuit which will convert the PWM dimming signal to an analog dimming voltage for measurement on pin DIM/UART.

2.2.5 Isolated dimming interface with CDM10V (optional)

Figure 11 shows an exemplary schematic of a 0-10V dimming interface for low BOM cost, using CDM10V by Infineon. CDM10V is a fully integrated 0-10V dimming interface IC which transmits secondary side analog voltage based signals from 0-10V dimmer to primary side, by driving an external opto-coupler with a 5mA current based PWM signal. The secondary auxiliary winding is necessary to supply the operating voltage of CDM10V. For more details about CDM10V, please visit Infineon website: http://www.infineon.com/cdm10v

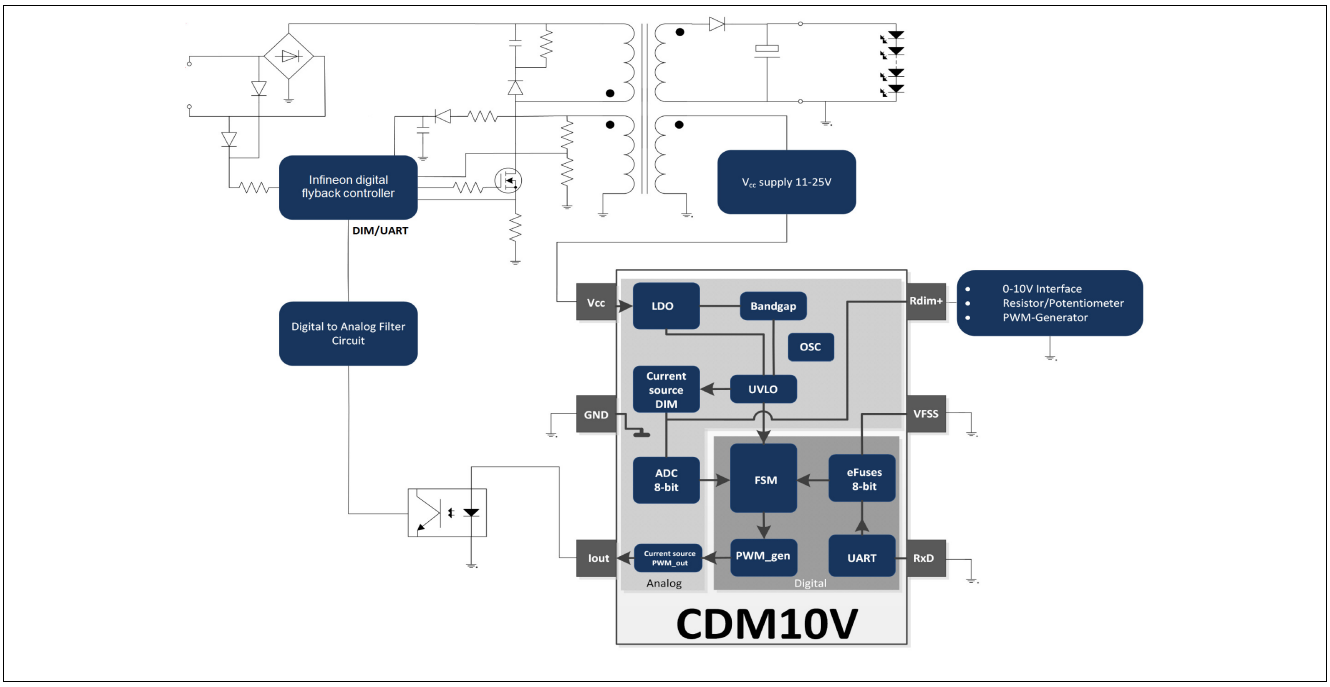

Figure 11 Optional circuit for isolated dimming with CDM10V

2.2.6 Wide output load voltage range circuit (optional)

If wide output load voltage is required, a regulator for VCC is required. This regulator limits the maximum voltage at pin VCC during steady state operation. **Figure 12** shows an exemplary schematic for the optional wide output voltage range support. A wide output voltage range impacts efficiency due to the necessary voltage regulator for VCC.

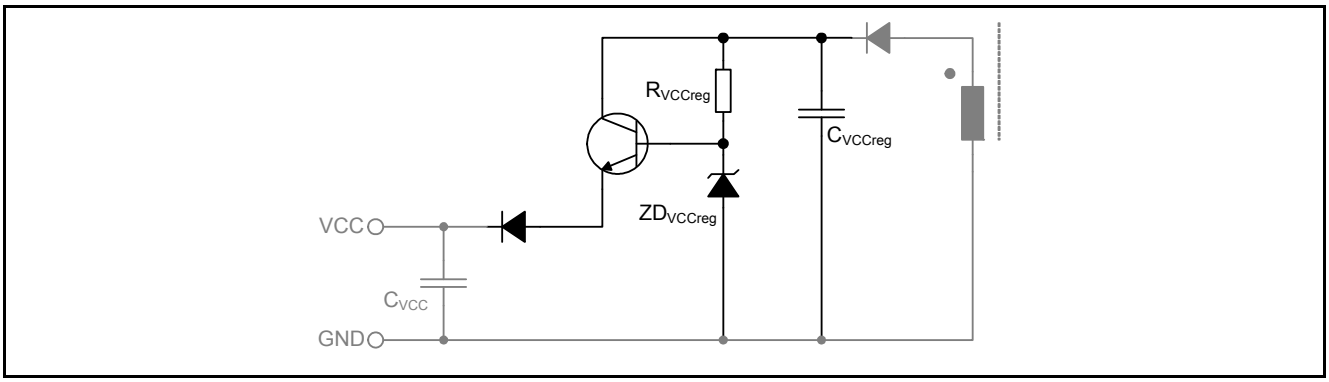

Figure 12 Optional wide output voltage range circuit

2.2.7 Automatic output discharge circuit (optional)

In case of a fault (e.g. Open Load) the output capacitors stay charged and may keep a high voltage. It is therefore recommended to add an automatic output discharge circuit. This circuit discharges the output capacitors if the main switch stops switching. For the circuit design, please refer the schematic in the application note of the XDPL8105 40W reference design with CDM10V.

2.2.8 VCC startup function combined with direct input monitoring

There are two main functions supported at pin HV which needs to be connected to the input voltage via resistor and two diodes.

The integrated HV startup-cell is switched on during the VCC startup phase before the IC is activated. Current flows from pin HV to pin VCC via an internal diode, which charges the capacitor at pin VCC. Once the voltage at pin VCC exceeds the V_{VCCon} threshold, the IC enables the active operating phase and switches off the HV startup-cell.

Furthermore, a direct input monitoring is supported that is controlled by an internal timer. The timer switches on the HV startup cell for a very short time after a defined period. During this short on-time the current is sensed at pin HV by a comparator to synchronize to frequency and phase of the input voltage.

2.2.9 Configurable soft start and output charging

After startup condition(e.g. input voltage, junction temperature) is checked within the limits, the IC initiates a soft-start. During soft-start, the switching stress for the power MOSFET, diode and transformer is minimized. The cycle-by-cycle current limit is increased in steps with a configurable time t_{ss} for each step. The number of soft start steps is defined by parameter n_{ss}[1)]. After startup pin CS maximum voltage limit of V_{start_OCP1} level has been reached, the output will be charged up with maximum on-time and V_{start_OCP1} level to the minimum output voltage that ensures self-supply, V_{out_start} but below the fully dimmed minimum output LED voltage, $V_{out\_dim\_min}$. After the output voltage reaches V_{out_start} level, the output constant current control loop

1) fixed at 3

(**Chapter 2.2.2**) takes over and the pin CS maximum voltage limit will be changed from $V_{\_start\_OCP1}$ to $V_{\_OCP1}$ level.

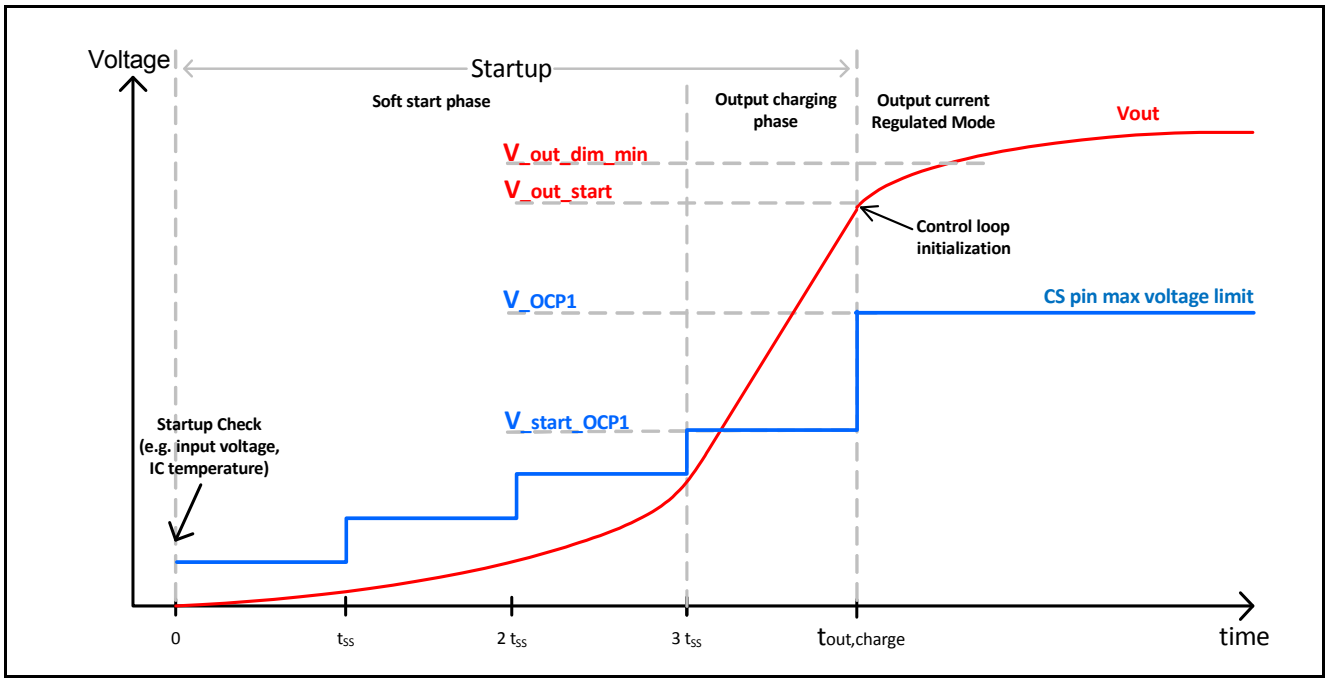

Figure 13 Configurable soft start and output charging phase

2.2.10 Configurable gate voltage rising slope at pin GD (Lower EMI)

The gate driver output signal can be configured with respect to the rising slope for switching on the power MOSFET. This feature can save BOM components (1 diode & 1 resistor) which are conventionally added to achieve the same purpose for EMI improvement. The maximum gate drive current $I_{\_GD\_pk}$ for the gate driver slope can be set between 30 mA and 118 mA (**Chapter 2.4**). **Figure 14** shows the gate driver output signal.

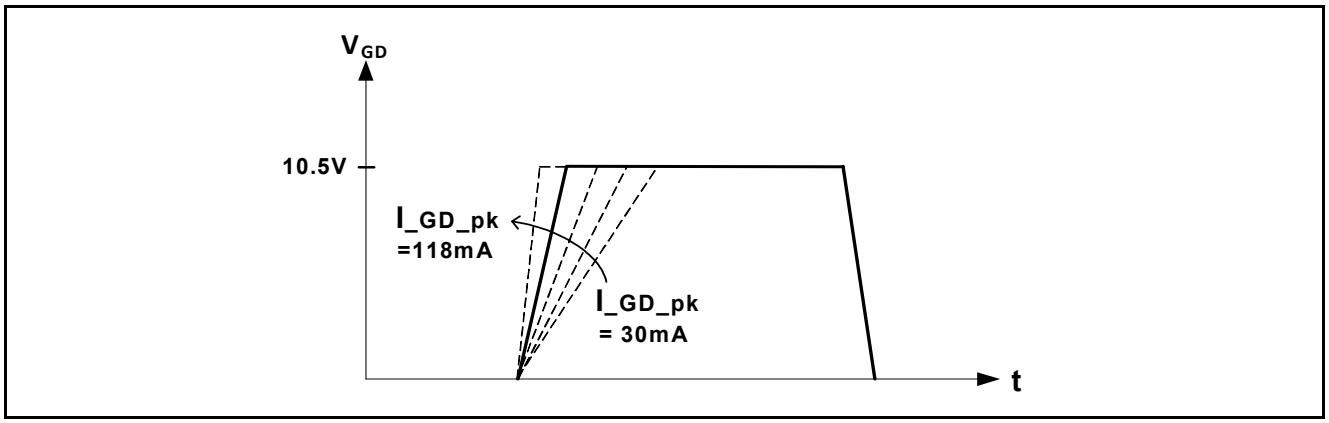

Figure 14 Configurable gate voltage rising slope for lower EMI

2.3 Protection features

Table 4 gives an overview about the available protection features and corresponding default actions in case a protection feature is triggered. Two protection reactions (auto restart mode and latch mode) are implemented.

Auto restart mode

Once the auto restart mode is activated, the IC stops the power MOSFET switching at pin GD and reduces the current consumption to a minimum. After the configurable auto restart time $t_{auto\_restart}$ the IC initiates a new start-up[1]. During this auto restart, the HV startup-cell is switched on and off in order to keep the VCC between V_{UVLO} and V_{OVLO} thresholds[2]. The auto restart cycle starts first with charging the VCC capacitor by means of switching on the HV startup cell until the V_{VCCon} threshold is exceeded. A regular startup procedure with soft start is initiated afterwards.

Latch mode

When latch mode is activated, the power MOSFET switching at pin GD is immediately stopped. The HV startup-cell is switched on and off in order to keep the VCC between V_{UVLO} and V_{OVLO} thresholds. The device stays in this state until input voltage is completely removed and the VCC voltage drops below the V_{UVLO} threshold. The IC can then be re-started by applying input voltage.

Table 4 Protection Features

Protection Feature	Active Period (if enabled)	Reaction	Description
Undervoltage lockout for VCC	Always on	Hardware restart	Chapter 2.3.1
Overvoltage protection for VCC	Always on	Latch mode[1]	Chapter 2.3.2
Overvoltage protection for V_{out}	Always on	Auto restart[1]	Chapter 2.3.3
Undervoltage protection for V_{out}	Activated after startup[2]	Auto restart	Chapter 2.3.3
Startup Undervoltage protection for V_{out}	During startup	Auto restart	Chapter 2.3.3
Overvoltage protection for V_{in}	Always on[2]	Latch mode	Chapter 2.3.4
Undervoltage protection for V_{in}	Always on[2]	Auto restart	Chapter 2.3.4
Input overcurrent detection level 1	Always on	Current limiting	Chapter 2.3.5
Input overcurrent protection level 2	Always on	Latch mode	Chapter 2.3.6
Output current protection (average)	Activated after startup[2]	Auto restart	Chapter 2.3.7
Output current protection (peak)	Activated after startup[2]	Auto restart	Chapter 2.3.7
Overtemperature protection	Always on	Latch mode	Chapter 2.3.8
Firmware protections (1st Watchdog & RAM Parity)	Always on	Auto restart	Chapter 2.3.9

1) Protection which its reaction can be configured to either auto restart mode or latch mode.
2) Protection which can be disabled or enabled by configuration.

1) After $t_{auto\_restart}$, the VCC will be charged to V_{VCCon} again(see Chapter 2.2.8). Therefore, the effective auto-restart time is longer than $t_{auto\_restart}$
2) This feature can be disabled for applications with externally supplied VCC.

2.3.1 Undervoltage lockout for VCC

An undervoltage lockout unit (UVLO) is implemented which ensures a defined enabling and disabling of the IC operation depending on the supply voltage at pin VCC. The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the IC and V_{UVOFF} for disabling the IC. Once the mains input voltage is applied, current flows through an external resistor into pin HV via the integrated diode to pin VCC. The IC is enabled once VCC exceeds the threshold V_{VCCon} and enters normal operation if no fault condition is detected. In this phase VCC will drop until the self supply via the auxiliary winding takes over the supply at pin VCC. For proper startup, the output voltage of V_{out_start} level for Vcc self supply via auxiliary winding must be in place before VCC falls below V_{UVOFF} threshold and before timeout of t_{start_max} for the startup output undervoltage detectionoccurs (See **Chapter 2.3.3**)

2.3.2 Overvoltage protection for VCC

Overvoltage detection at pin VCC is implemented via a threshold of V_{VCC_max}.

2.3.3 Over / undervoltage protection for output voltage

Overvoltage (e.g. Open Load) or undervoltage (e.g. Output short) detection of the output voltage V_{out} is provided by the measurement and calculation as described in **Chapter 2.2.1.3**. The overvoltage protection reaction (auto-restart or latch) and detection thresholds V_{outOV} are configurable. For output overvoltage protection in auto-restart reaction, either slow or fast auto-restart can also be selected.

Please note that there are possibilities where critical protection like output over-voltage not working properly (example: wrong parameter configurations loaded). Thus, please consider adding zener diode or any voltage suppressor device/circuit on output for reinforced safety purpose.

Note: It is mandatory to have output discharge resistor/circuit which discharges the output capacitor after triggering open load protection at V_outOV. Latch reaction is recommended for open load protection as it can shut down the unit to prevent output overcharged if the discharge resistor ohmic value is too high.

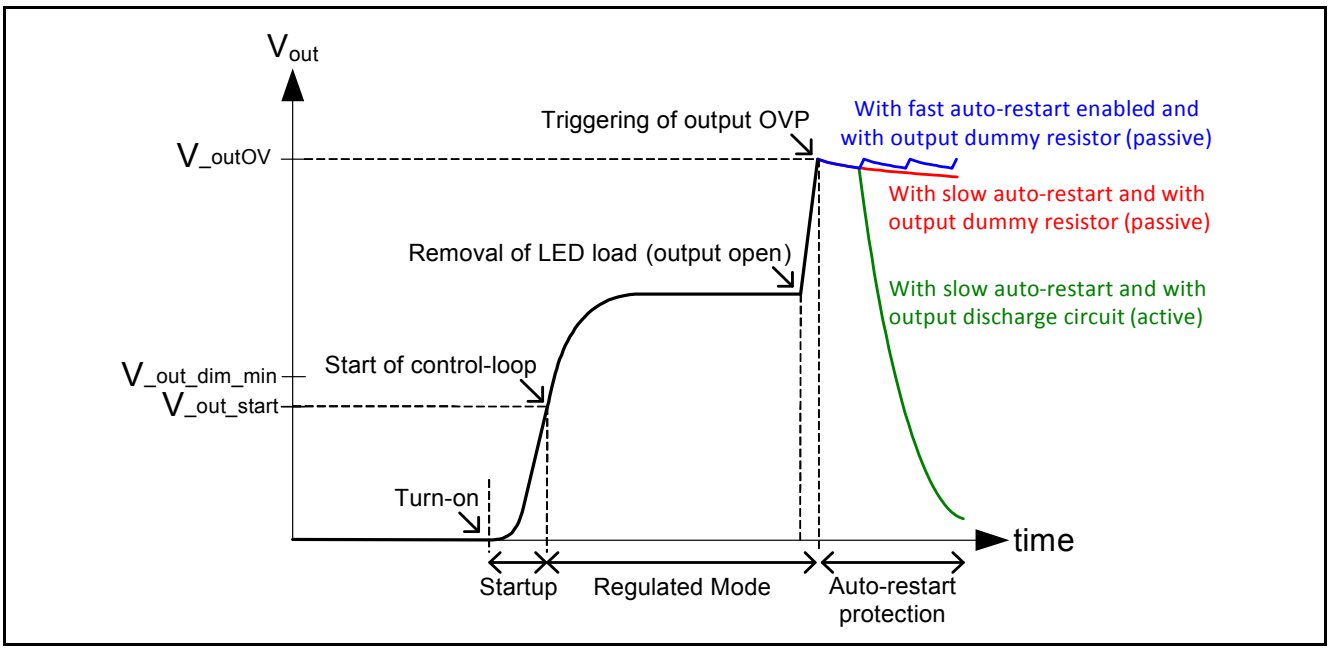

Figure 15 Voltage threshold for output overvoltage protection

The undervoltage protection reaction is fixed as auto-restart and its detection threshold $V_{\_outUV}$ is fixed at 50% of the configurable fully dimmed minimum output load voltage parameter, $V_{\_out\_dim\_min}$. Output undervoltage protection is disabled during the startup phase.

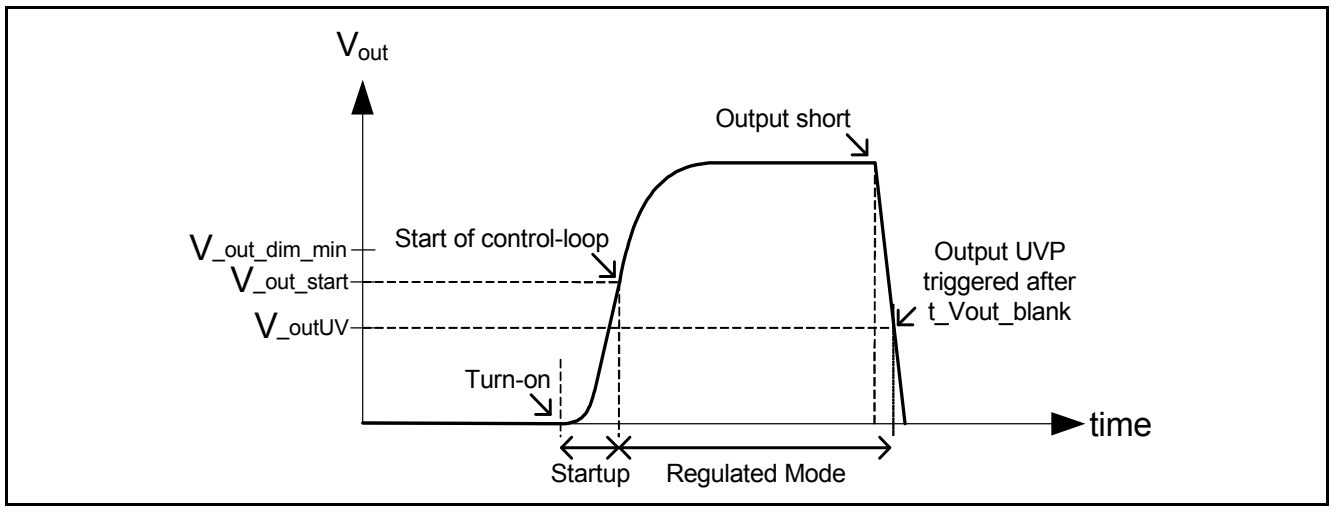

Figure 16 Voltage threshold for output undervoltage protection

In case of output short/undervoltage, the auxiliary winding cannot provide power to VCC during startup because the output voltage stays below $V_{\_out\_start}$ or $V_{\_outUV}$. Therefore, the startup output undervoltage protection is triggered if the output voltage has not reached $V_{\_out\_start}$ before a configurable timeout of $t_{\_start\_max}$ occurs during the startup phase. To ensure that the startup undervoltage protection is in auto-restart reaction, the pin VCC capacitance has to be high enough to maintain the VCC above V_{UVOFF} threshold long enough until the timeout of $t_{\_start\_max}$ occurs during the startup phase.

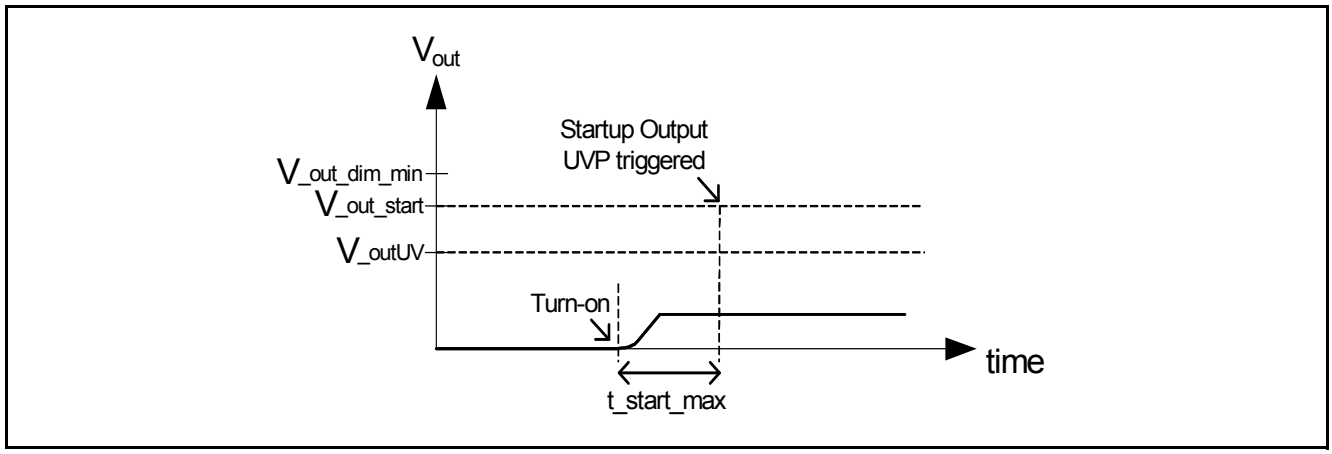

Figure 17 Voltage and timing threshold for startup output undervoltage protection

2.3.4 Over / undervoltage protection for input voltage

An over / undervoltage detection of the input voltage V_{in} is provided by the measurement and calculation as described in **Chapter 2.2.1.2**. The V_{in} rms value is calculated based on the measured V_{in} peak value and compared to the configurable internal input over / undervoltage protection thresholds $V_{\_inOV}$ and $V_{\_inUV}$ (**Chapter 2.4**).

Figure 18 shows an exemplary setting of both over- and undervoltage thresholds together with configurable startup thresholds $V_{\_in\_start\_min}$ and $V_{\_in\_start\_max}$ to create hysteresis for flicker-free operation at auto-restart.

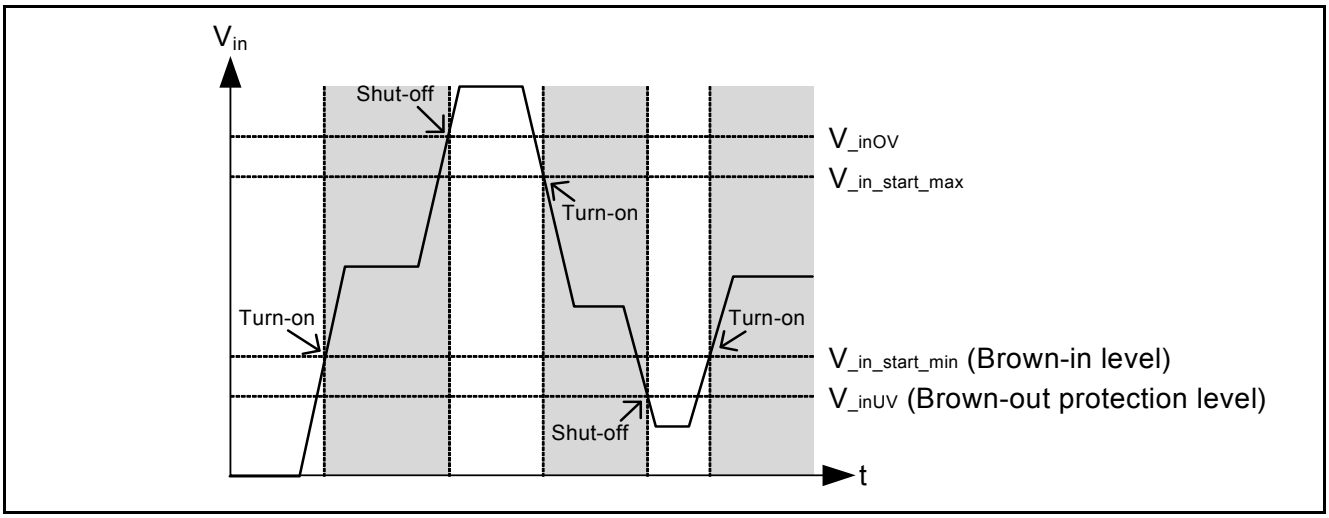

Figure 18 Voltage threshold for input over / undervoltage protection

2.3.5 Input overcurrent detection level 1 (OCP1)

The input overcurrent protection level 1 is performed by means of the cycle-by-cycle peak current limitation to $V_{\_OCP1}$. A leading edge blanking, $t_{\_CSLEB}$ prevents the IC from falsely switching off the power MOSFET due to a leading edge spike.

2.3.6 Input overcurrent protection level 2 (OCP2)

The input overcurrent protection level 2 is meant for covering fault conditions like a short in the transformer primary winding. In this case overcurrent protection level 1 will not limit properly the peak current due to the very steep slope of the peak current. Once the threshold $V_{\_OCP2}$ is exceeded for longer than $t_{\_CSOCP2}$, the protection is triggered.

2.3.7 Output overcurrent protections

The XDPL8105 includes protections against exceeding an average and peak current limit. The average output current is calculated over one half cycle of the input frequency to remove the output current ripple. With auto-restart reaction, either slow auto-restart or fast auto-restart can be selected.

2.3.8 Overtemperature protection

XDPL8105 offers a conventional as well as an adaptive overtemperature protection scheme using an internal temperature sensor.

Note: Please note that the internal temperature sensor may not be able to sense and protect the temperature of external components (e.g. power MOSFET, VCC regulator) without sufficient thermal coupling.

Conventional overtemperature protection

The overtemperature protection initiates a thermal shutdown once the internal temperature detection level $T_{\_critical}$ is reached. With latch mode protection, IC will turn off and only restart after recycling of input power. At startup, junction temperature has to be below $T_{\_start}$.

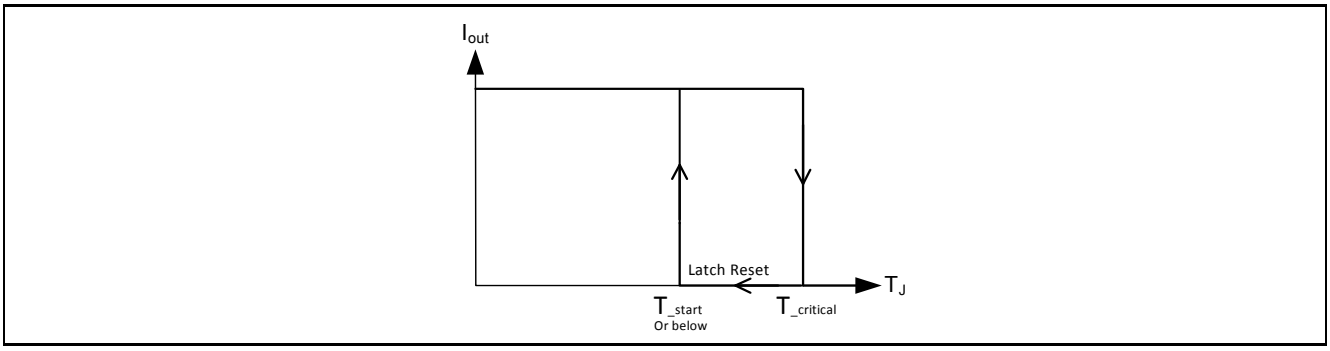

Figure 19 Conventional temperature protection

Adaptive temperature protection

To protect load and driver against overtemperature, XDPL8105 features a reduction of output current below maximum current I_out_set. As long as temperature T_hot is exceeded, the current is gradually reduced as shown in **Figure 20**. If a reduction down to a minimum current I_out_red is not able to compensate the increase of temperature, the overtemperature protection (with latch mode) is entered when T_critical is reached.

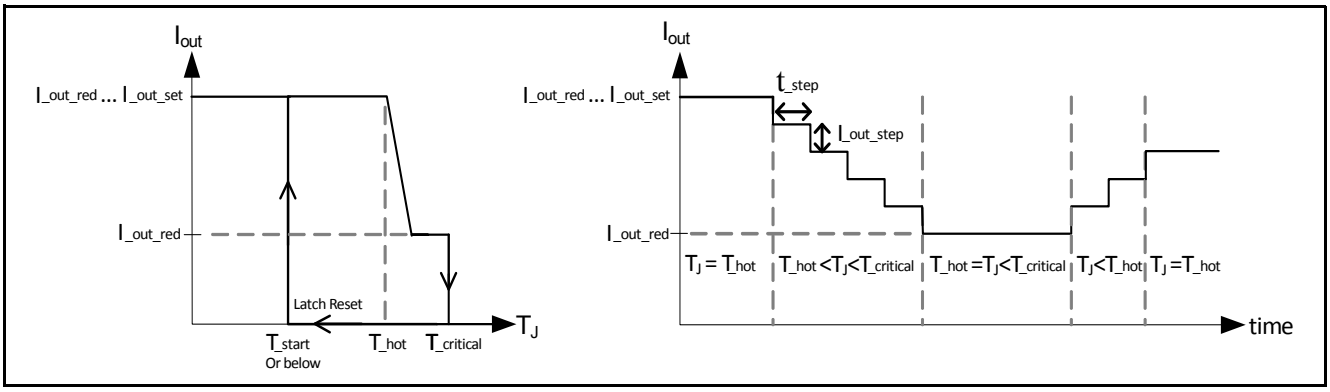

Figure 20 Adaptive temperature protection

2.3.9 Firmware protections

XDPL8105 includes several protections to ensure the integrity and flow of the firmware:

- A hardware watchdog triggers a protection in case the firmware does not service the watchdog within a defined time period.
- A RAM parity check triggers a protection in case a bit in the memory flips.
- A cyclic redundancy check (CRC) at each startup verifies the integrity of firmware and parameters.
- A first firmware watchdog triggers a protection if the ADC hardware cannot provide all necessary information within a defined time period. This may occur if timing requirements for the ADC are exceeded.
- A second firmware watchdog triggers a protection if the execution of protection checks and the control loop are not matching a defined time period. This may occur if timing requirements are exceeded (e.g. operation beyond frequency limits).

2.4 Configuration and support

The configuration of XDPL8105 is supported by the GUI tool .dp vision provided by Infineon. This chapter describes the configuration procedure via the UART interface. Furthermore, it contains an overview about the parameters and functions that can be configured.

2.4.1 Configuration procedure and design-in support

Figure 21 shows the setup for the configuration of XDPL8105. The Infineon graphic user interface (GUI) .dpVision connects to XDPL8105 via the isolated USB interface board called .dp Interface Gen2. The .dp interface Gen 2 provides power via VCC to XDPL8105 and connects via UART interface at pin DIM/UART. The common UART interface enables communication with the IC even without the interactive GUI tool. This allows easy configuration during mass production.

When VCC exceeds the V_{VCCon} threshold, XDPL8105 will sense pin DIM/UART for a UART connection. If power is provided by VCC and no input voltage is applied at startup, XDPL8105 will enter configuration mode. Also, XDPL8105 will enter configuration mode if no parameters have been programmed so far, regardless of input voltage being applied or not.

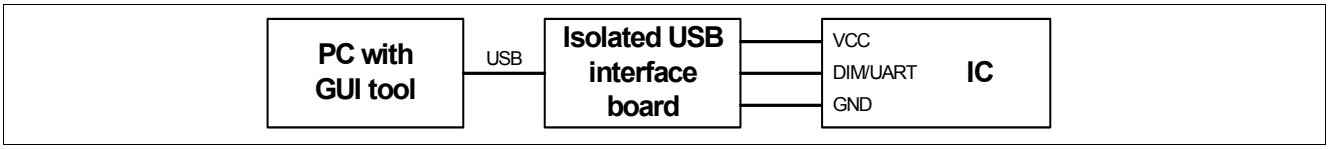

Figure 21 Setup for configuration of the IC

For project development, a graphic user interface called .dp Vision guides the designer through the configuration of parameters. Further information on .dp Vision can be found in the .dp Vision User Manual provided by Infineon.

For production and end user configuration, a simpler graphic user interface called XDP™ GUI is also available. The configurable parameters and configuration range of each parameter in the XDP™ GUI can be customized using the XDP™ GUI Builder software provided by Infineon. Please refer the user manual of this GUI Builder for more details.

The dimensioning of the application design(e.g. transformer design, BOM selection, IC parameterization) can be done easily with an excel tool named XDPL8105 system simulation & design creation tool. A XDPL8105 reference design with CDM10V is available from Infineon to demonstrate the features and performance. The design guide presents the dimensioning process while the reference design application note presents the board performance, fine tuning guide, debugging guide and frequently asked questions.

2.4.2 Overview configurable parameters and functions

The XDPL8105 provides a generic firmware version that includes all configurable parameters set to zero. The parameter values need to be specified by the user according to the target application. **Table 5** lists the configurable parameters. **Table 6** lists the non configurable parameters which the values are constant or adapted internally according to the configurable parameters settings.

Table 5 List of configurable parameters

Description	Parameter	Example	Configuration Range
Hardware configuration			
I_{out} set point (non-dimmed)	I_out_set	880 mA	Calculated by GUI

Table 5 List of configurable parameters (cont'd)

Description	Parameter	Example	Configuration Range
Transformer primary winding turns	N_p	58	> 0
Transformer secondary winding turns	N_s	15	> 0
Transformer auxiliary winding turns	N_a	15	> 0
Transformer nominal primary Inductance	L_p	0.544 mH	Calculated by GUI
Current sense resistor	R_{CS}	0.22 ohm	Calculated by GUI
Pin CS OCP1 limit during regulated mode	V_{OCP1}	0.49 V	Calculated by GUI
Pin ZCD series resistor	R_{ZCD_1}	56.2 kohm	Calculated by GUI
Pin ZCD shunt resistor	R_{ZCD_2}	2.00 kohm	Calculated by GUI
Vcc Voltage Supply Type	V_{CC_SUPPLY}	Wide	[External, Narrow, Narrow_24.9V, Wide]
Vcc capacitor total capacitance	C_{VCC}	15.0 uF	Calculated by GUI
Output capacitor maximum Voltage Rating	$V_{out\_cap\_rating}$	63 V	≥ 0
Pin HV series resistor	R_{HV}	66 kohm	Calculated by GUI
Gate driver peak source current	I_{GD_pk}	49 mA	30 mA to 118 mA (with few mA change per step)
Protections			
Auto restart time	$t_{auto\_restart}$	1 s	0.1 s to 25.5 s[1)]
Fast auto restart time	$t_{auto\_restart\_fast}$	0.4 s	0.1 s to 25.5 s[1)]
Output OVP / Open Reaction	$Reaction_{OVP\_Vout}$	Auto restart	[Auto restart, Latch mode]
Auto restart speed for output OVP	$Speed_{OVP\_Vout}$	Slow	[Slow, Fast]
Output OVP threshold	V_{outOV}	48.4 V	$V_{out\_dim\_min}$ to $V_{out\_cap\_rating}$
Enable output UVP / Short Protection	EN_{UVP_Vout}	Enabled	[Enabled, Disabled]
Timeout for short detection at startup	t_{start_max}	10.0 ms	Calculated by GUI
Enable Maximum Average output OCP	$EN_{Iout\_max\_avg}$	Enabled	[Enabled, Disabled]
Enable Maximum Peak output OCP	$EN_{Iout\_max\_peak}$	Enabled	[Enabled, Disabled]
Maximum peak Output OCP threshold	$I_{out\_max\_peak}$	1980 mA	Calculated by GUI
Auto restart speed for output OCP	$Speed_{OCP\_Iout}$	Slow	[Slow, Fast]
Enable Input OVP	EN_{OVP_In}	Enabled	[Enabled, Disabled]
Enable Input UVP	EN_{UVP_In}	Enabled	[Enabled, Disabled]
Input OVP threshold	V_{inOV}	329 V_{rms}[2)]	Calculated by GUI
Maximum startup input voltage	$V_{in\_start\_max}$	329 V_{rms}[2)]	$V_{in\_start\_min}$ to V_{inOV}
Minimum startup input voltage	$V_{in\_start\_min}$	72 V_{rms}[2)]	V_{inUV} to $V_{in\_start\_max}$
Input UVP threshold	V_{inUV}	62 V_{rms}[2)]	Calculated by GUI
Vcc OVP Reaction	$Reaction_{VCCP}$	Latch mode	[Auto restart, Latch mode]
Enable Debug mode	Debug_mode	Disabled	[Enabled, Disabled]
Temperature guard			

Table 5 List of configurable parameters (cont'd)

Description	Parameter	Example	Configuration Range
Overtemperature detection threshold	T_critical	119 °C	110°C to ($T_{J(max)}$ - 6°C)
Enable adaptive temperature protection	EN_ITP	Enabled	[Enabled, Disabled]
Temperature to start derating of I_{out}	T_hot	110 °C	0 °C to T_critical
Minimum I_{out} for adaptive temperature protection	I_out_red	220 mA	0 mA to I_out_set
Time step for each I_{out} derating	t_step	10 s	2 s to 20 s
Startup & shutdown			
Soft start timestep	t_ss	0.5 ms	Calculated by GUI
Minimum Vout when fully dimmed	V_out_dim_min	11.9 V	V_out_start to V_outOV
Vout to start constant current control loop	V_out_start	9.5 V	V_outUV to V_out_dim_min
Pin CS OCP1 limit after startup	V_start_OCP1	0.49 V	Calculated by GUI
Initial mode of operation	control_loop_init	DCM	[ABM, DCM, QRM]
Initial DCM frequency at startup	f_DCM_init	12 kHz	f_sw_min_DCM to f_sw_max
Initial number of ABM pulses at startup	N_ABM_init	100	Calculated by GUI
Control loop			
QRM PI regulator proportional coefficient	PI_KP_QRM	550	10 to 3000
QRM PI regulator integral coefficient	PI_KI_QRM	8	1 to 1000
DCM PI regulator proportional coefficient	PI_KP_DCM	17000	100 to 30000
DCM PI regulator integral coefficient	PI_KI_DCM	200	10 to 10000
ABM PI regulator proportional coefficient	PI_KP_ABM	64	1 to 600
ABM PI regulator proportional coefficient	PI_KI_ABM	32	1 to 200
Dimming			
Enable DImming	EN_DIM	Enabled	[Enabled, Disabled]
Pin DIM/UART voltage for minimum I_{out}	V_DIM_min	0.2 V	V_DIM_off to V_DIM_max
Minimum Iout when fully dimmed	I_out_dim_min	88 mA	Calculated by GUI
Dimming curve shape	C_DIM	Quadratic	[Linear, Quadratic]
Enable dim-to-off	EN_DIM_TO_OFF	Disabled	[Enabled, Disabled]
Pin DIM/UART voltage for dim-to-off	V_DIM_off	0.18 V	0.1 V to V_DIM_on
Pin DIM/UART voltage for dim-to-on	V_DIM_on	0.19 V	V_DIM_off to V_DIM_min
Enable Square Wave Output for pin SQW	EN_SQW	Disabled	[Enabled, Disabled]
Multimode			
Maximum switching frequency	f_sw_max	180.8 kHz	Calculated by GUI
Maximum on-time	t_on_max	11.3 us	Calculated by GUI
Minimum on-time	t_on_min	1.1us	1 us to t_on_max
Minimum demagnetization time	t_min_demag	3.0 us	2 us to 10 us
Minimum switching frequency in DCM	f_sw_min_DCM	12 kHz	3 kHz to 20kHz

Table 5 List of configurable parameters (cont'd)

Description	Parameter	Example	Configuration Range
Enable Active Burst Mode	EN_ABM	Disabled	[Enabled, Disabled]
Enhanced PFC			
Enhanced PFC compensation gain	C_EMI	0.1000 uF	≥ 0
Fine tuning			
ZCD propagation delay compensation	t_ZCDPD	410 ns	0 ns to 1000 ns
CS Propagation delay compensation	t_PDC	200 ns	0 ns to 1000 ns
Transformer coupling	T_coupling	1.020	0.000 to 2.000
Input voltage drop compensation	R_in	11.9 ohm	≥ 0
Switching period modulation attenuation	N_DCM_mod_gain	8	[0, 4, 8, 16, 32]
Temperature compensation for V_{DIM}	a_DIM	0mV/K	-8 mV/K to 8 mV/K

1) The auto-restart time has to be chosen sufficiently large enough to avoid a stepping up of the output voltage which would exceed the output overvoltage level.
2) The input voltage levels refer to AC RMS voltage. If a programmed XDPL8105 is operated with both AC or DC, the threshold for DC input voltage is 1.41 times the threshold for AC RMS input voltage.

Table 6 List of non-configurable parameters

Description	Parameter	Value	Notes
Hardware configuration			
Transformer primary leakage inductance	L_p_lk	L_p * 1% uH	
Output diode voltage drop	V_out_diode_drop	0.7 V	
Gate driver high voltage	V_GD	10.5 V	
Protections			
Output UVP / Short Reaction	Reaction_UVP_Vout	Auto restart	
Output UVP threshold (at steady state)	V_outUV	V_out_dim_min *50% V	
Steady state Output UVP blanking time	t_Vout_blank	1 ms	
Maximum Average output OCP Reaction	Reaction _Iout_max_avg	Auto restart	
Maximum Average Output OCP threshold	I_out_max_avg	I_out_set * 150% mA	
Maximum Peak output OCP Reaction	Reaction _Iout_max_peak	Auto restart	
Input OVP Reaction	Reaction_OVP_Vin	Latch mode	
Input UVP Reaction	Reaction_UVP_Vin	Auto restart	
Input OCP2 / Short Winding Reaction	Reaction_OCP2	Latch mode	
Vcc OVP Threshold	V_VCC_max	24 V or 24.9V	if VCC_SUPPLY = Narrow_24.9V, 24.9V. Otherwise, 24V
Hardware reaction for Firmware Protection (Watchdog, RAM parity)	Reaction_HW	Auto restart	

Table 6 List of non-configurable parameters (cont'd)

Description	Parameter	Value	Notes
Temperature guard			
Overtemperature Reaction	Reaction_TP	Latch mode	
Maximum startup temperature	T_start	T_hot -2°C or T_critical -2°C	if EN_ITP = enabled, T_hot -2°C, otherwise T_critical -2°C
I_{out} reduction in each derating step	I_out_step	I_out_set/80	
Startup & shutdown			
Number of soft start steps	n_ss	3	
Dimming			
Pin DIM/UART voltage for maximum I_{out}	V_DIM_max	1.72 V	
Square-wave frequency for SQW pin	f_SQW	160 kHz	
Square-wave voltage for pin SQW	V_SQW	7.5 V	
Multimode			
Minimum switching frequency in QRM	f_sw_min_QRM	20 kHz	
Enable DCM	EN_DCM	Enabled	
Fine tuning			
Spike blanking time for OCP2 trigger	t_CSOCP2	240 ns	
Leading edge blanking time	t_CSLEB	480 ns	
ZCD ringing suppression time	t_ZCDring	1200 ns	
Blanking time for CCM protection	t_CCM	10 ms	
Number of digital filter stages for V_{DIM}	N_DIM_Filter	6	

2.4.3 Debug mode support

If an unexpected system protection was triggered during testing, user can set parameter Debug_mode to “Enabled”, which allows the firmware status code readout from the IC to debug which protection was triggered.

For example in **Figure 22**, the firmware status code readout in the GUI shows a number of 0x0001 (in red colour), which the description shows that the output over-voltage protection has been triggered. The description of the status code will be shown automatically when the mouse pointer is hovered around the status code.

Note: if there is no protection being triggered, the firmware status code should be 0x0000 (in black colour)

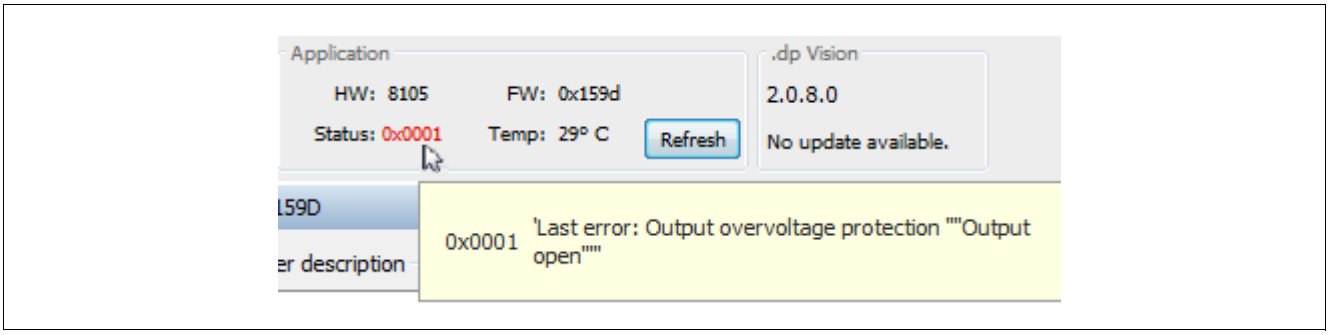

Figure 22 Firmware status code readout for debugging

Please kindly refer the application note for details on the necessary setup & procedures to read out the firmware status code in debug mode.