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XDPL8220 Digital PFC+Flyback Controller IC

XDP™ Digital Power

Data Sheet
Revision 1.0
Quality Requirement Category: Industrial

Features

- Universal AC input (90 - 305 VAC) or DC input (90 - 305 VDC)
- Applicable power range of 20 W to 150 W
- Small number of external parts optimizes ***Bill of Materials (BOM)*** and form factor
- High efficiency (> 90%)
- Multicontrol mode (***Constant Current (CC)***/***Constant Voltage (CV)***/***Limited Power (LP)***) reduces required product variety
- Important parameters can be configured after manufacturing
- Low harmonic distortion (***Total Harmonic Distortion (THD)*** < 15%)
- Low output ripple current
- Integrated startup cell ensures fast time to light (< 250 ms)
- Adaptive Temperature Protection
- Ambient operating temperature -40 °C to 85 °C
- Automatic switching between ***Quasi-Resonant Mode (QRM)*** and ***Discontinuous Conduction Mode (DCM)***
- Wide output voltage range
- ***Pulse Width Modulation (PWM)*** dimming control
- Output dimming by analog reduction of driving current down to 5%

For safe operation, the XDPL8220 contains a comprehensive set of protection features:

- Output overvoltage protection (open load)
- Output undervoltage protection (output short)
- VCC over- and undervoltage lockout
- Input over- and undervoltage protection
- Bus over- and undervoltage protection
- Overcurrent protection for ***Power Factor Correction (PFC)*** and ***Flyback (FB)*** stage

Applications

- Integrated ***Electronic Control Gear (ECG)*** for ***Light Emitting Diode (LED)*** luminaires

Description

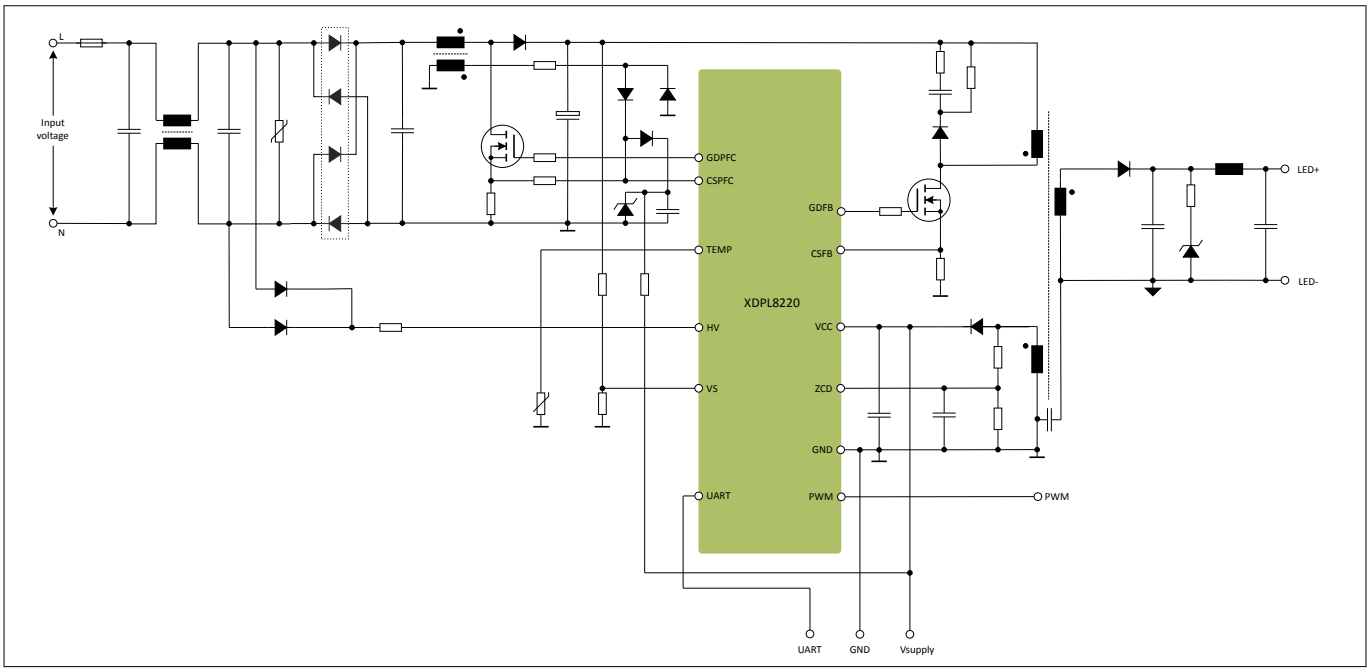

Figure 1 Typical Application for XDPL8220

Product Type	Package
XDPL8220	PG-DSO-16

Description

XDPL8220 is a highly integrated next-generation device combining a boundary mode ***PFC*** plus a quasi-resonant ***FB*** controller with primary-side regulation. The integration of these functions enables saving of external parts and optimizes performance by harmonized operation of the two stages.

XDPL8220 uses a constant on-time scheme with a ***THD*** improvement algorithm to provide a high power factor and excellent ***THD*** performance.

With its unique control scheme of ***CV***, ***CC*** and ***LP***, the ***LED*** driver designer is provided with a large degree of flexibility and can utilize the system hardware to its limits.

The on-chip ***One Time Programmable Memory (OTP)*** memory has an area for parameters that control the behavior of the circuit, e. g. the output current or the maximum output power. This enables the user of the device to create a platform concept with significantly fewer different hardware versions while still covering the same application range.

The two-stage approach reduces any variation in the output current (flicker) to a non-visible level. By separating the ***PFC*** from the power conversion part (***FB***), both stages operate in a more stable manner and require fewer margins, which has a positive influence on the cost.

Lighting requires more and more 24/7 operation, making it necessary to have a stand-by mode with short wake-up times and low power consumption. The power consumption of less than 100 mW of the XDPL8220-based systems defines the new standard for stand-by power in lighting ***ECG***s.

XDPL8220 enables adaptive temperature protection using either the internal sensor or an external ***Negative Temperature Coefficient Thermistor (NTC)***, or both.

Futureproof flexibility with application-oriented programmable operating windows enables management of ***LED*** generations and portfolio complexity .

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1 Functional Block Diagram

The functional block diagram shows the basic data flow from input pins via signal processing to the output pins.

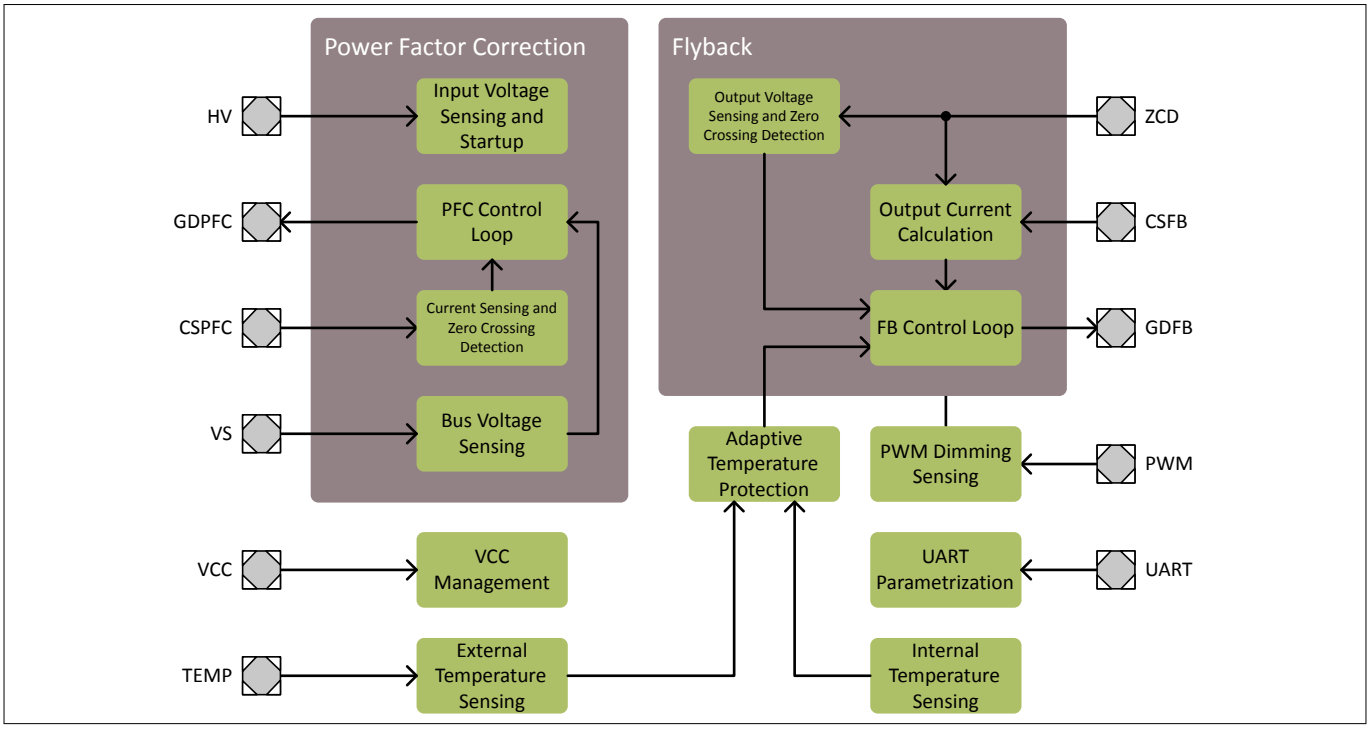

Figure 2 XDPL8220 Simplified Functional Block Diagram

2 Pin Configuration

Pin assignments and basic pin description information are shown below.

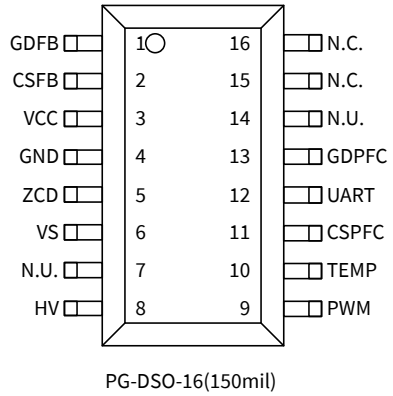

Figure 3 Pinning of XDPL8220

Table 1 Pin Definitions and Functions

Name	Pin	Type	Function
GDFB	1	O	Gate driver for ***FB***: The GDFB pin is an output for directly driving a power MOSFET of the ***FB*** stage.
CSFB	2	I	Current sensing for ***FB***: The CSFB pin is connected to an external shunt resistor and the source of the power MOSFET of the ***FB*** stage.
VCC	3	I	Voltage supply
GND	4	-	Power and signal ground
ZCD	5	I	Zero-crossing detection of the ***FB***: The ZCD pin is connected to an auxiliary winding of the ***FB*** stage for zero-crossing detection as well as primary-side output voltage and backup bus voltage sensing for safety.
VS	6	I	Bus voltage sensing
N.U.	7	-	Not used. Externally to be connected to GND.
HV	8	I	High voltage: The HV pin is connected to the rectified input voltage via an external resistor. An internal 600 V HV startup-cell is used to initially charge VCC. In addition, sampled high-voltage sensing is also used for synchronization with the input frequency.
PWM	9	I	***PWM*** dimming: The PWM pin is used as a dimming input.
TEMP	10	I	External temperature sensor: Measurement of external temperature using an ***NTC***.
CSPFC	11	I	Current sensing for ***PFC***: The CSPFC pin is connected to an external shunt resistor and the source of the power MOSFET of the ***PFC*** stage.

Table 1 Pin Definitions and Functions (continued)

Name	Pin	Type	Function
UART	12	I/O	***Universal Asynchronous Receiver Transmitter (UART)*** communication: The UART pin is used for the ***UART*** interface to support parameterization.
GDPFC	13	O	Gate driver for ***PFC***: The GDPFC pin is an output for directly driving a power MOSFET of the ***PFC*** stage.
N.U.	14	-	Not used. Externally to be connected to GND.
N.C.	15	-	Not connected.
N.C.	16	-	Not connected.

3 Functional Description

This chapter provides a summary of the integrated functions and features, and describes the relationships between them. The parameters and equations are based on typical values at T_A = 25 °C.

XDPL8220 is a digital dual-stage ***PFC*** and ***FB*** controller IC supporting ***PWM*** dimming functionality. Both stages use configurable multimode operation to select the best mode of operation for every operation condition. Multimode operation automatically switches between ***Quasi-Resonant Mode, switching in valley n (QRMn)*** and ***DCM***.

XDPL8220 features a comprehensive set of configurable protection modes to detect fault conditions.

XDPL8220 provides a high degree of flexibility in design-in of the application. A ***Graphic User Interface (GUI)*** tool supports users in the configuration of the operational and protection parameters.

3.1 PFC Controller Features

The ***PFC*** stage ensures high power quality by maximizing the power factor and minimizing harmonic distortion.

The ***PFC*** stage operates in ***Quasi-Resonant Mode, switching in valley 1 (QRM1)*** and ***QRMn***, to support low load conditions and ensure efficient operation.

The ***PFC*** stage is implemented as a boost converter. It drains a sinusoidal current from the single-phase line supply and provides stabilized ***Direct Current (DC)*** voltage at the internal bus voltage rail. The power factor of the single-phase line supply is almost one. Fluctuations in line voltage as well as voltage drops of short duration are compensated.

3.1.1 Shared CS/ZCD Function

The ***PFC*** stage makes use of combined CS/ZCD functionality at the CSPFC pin.

During the gate driver on-time the pin acts as a current sense (CS), while during the gate driver off-time the pin acts as a zero-crossing-detector (ZCD). The CS senses the on-time current and implements overcurrent limitation; the ZCD exploits the quasi-resonant function to minimize conduction losses.

The CSPFC pin is connected via a resistor divider composed of $R_{ZCD,1,PFC}$ and $R_{ZCD,2,PFC}$ and a set of diodes to an auxiliary winding of the ***PFC*** choke inductor. It is used for detecting the valleys of the quasi-resonant oscillation to turn on the ***PFC*** MOSFET based on the desired valley computed by the multimode ***PFC*** control. The diode D_1 allows positive voltage at the CSPFC pin as the valley detection is implemented by the internal hysteretic comparator with a positive reference of nominal THR_{HYS} for falling edges. The CSPFC pin senses the drain source current of the switching MOSFET. The CS voltage is measured after a programmable blanking time after turn-on of the switch. An appropriate current sensing resistor $R_{CS,PFC}$ is selected on the basis of the maximum current flowing in the switching MOSFET and the dynamic voltage range of the input pin CSPFC.

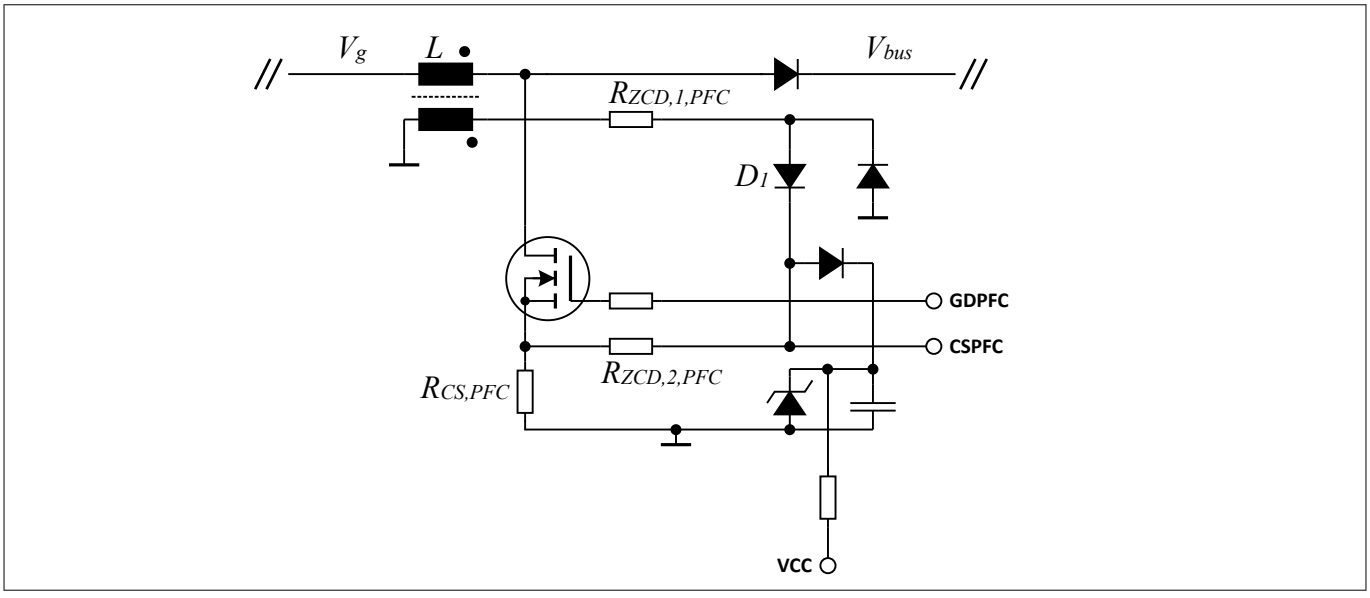

Figure 4 Shared CS/ZCD Schematic

3.1.2 Quasi-resonant Mode

The quasi-resonant mode maintains a high efficiency level.

For ***PFC*** operating in ***QRM1***, the main switch is turned on with a constant on-time for a line and load condition, while the off-time/demagnetization time varies within an ***Alternating Current (AC)*** half-cycle depending on the instantaneously rectified ***AC*** input voltage V_g. Subsequently, the switching frequency varies within each ***AC*** half-cycle with the lowest switching frequency at the peak of the ***AC*** input voltage and the highest switching frequency near the zero crossings of the input voltage. A new switching cycle starts immediately when the first QR valley is reached.

QRM1 is ideal for full-load operation, where the on-time is large. However, the on-time reduces at light loads, resulting in very high switching frequencies, particularly near the zero crossings of the input voltage. The high switching frequency will increase switching losses, resulting in poor efficiency at light loads. The ***PFC*** multimode control can lower the switching frequency by selecting further valleys to achieve QRM2 up to $N_{valley,max,PFC}$ operation. The switching frequency is limited within a defined range and the efficiency at light loads improves.

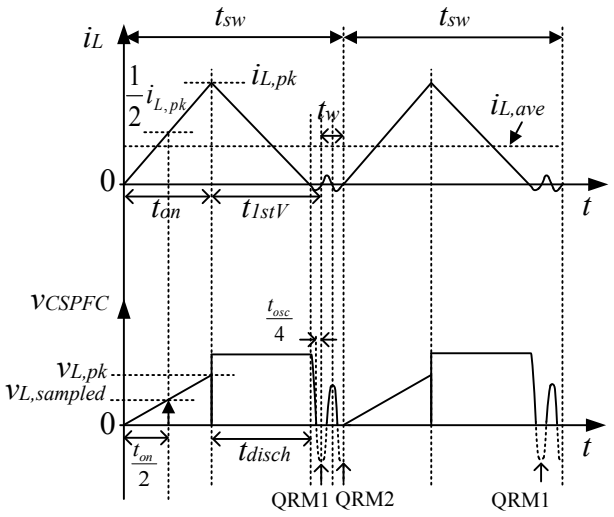

Figure 5 PFC QRM2 Waveforms

The equations for the quasi-resonant operation are shown below, where t_w is an additional delay in each switching cycle when selecting subsequent valleys after the first QR valley and n is the valley number in ***QRMn***.

$$i_{L,pk} = \frac{V_g \cdot t_{on}}{L}$$

$$t_{disch} = \frac{i_{L,pk} \cdot L}{V_{bus} - V_g}$$

$$t_{1stV} = t_{disch} + t_{osc}/2$$

$$t_w = t_{osc} \cdot (n-1)$$

$$t_{sw} = t_{on} + t_{1stV} + t_w$$

$$t_{off} = t_{1stV} + t_w$$

Equation 1

3.1.3 Bus Voltage Sensing

The bus voltage is measured at the VS pin.

The VS pin implements ***PFC*** bus voltage sensing for bus voltage regulation. The bus voltage is scaled down using a simple resistor divider. A capacitor could in certain cases be added at the pin to ground to filter high-frequency switching noise. The bus voltage sensing is a low leakage input and no additional measures are needed to reduce the current consumption.

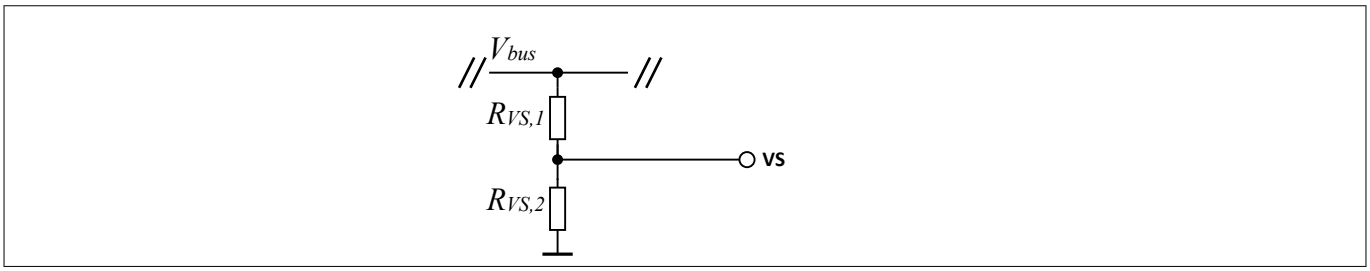

Figure 6 Bus Voltage Sensing Schematic

The ***Analog-to-Digital Converter (ADC)*** input at the VS pin utilizes two voltage ranges. The wider voltage range from 0 to V_{REF} results in lower resolution. The narrower voltage range from 5/6 V_{REF} to 7/6 V_{REF} gives better voltage resolution. Steady state operation therefore normally takes place in the high-resolution range and soft start operation in the low-resolution range.

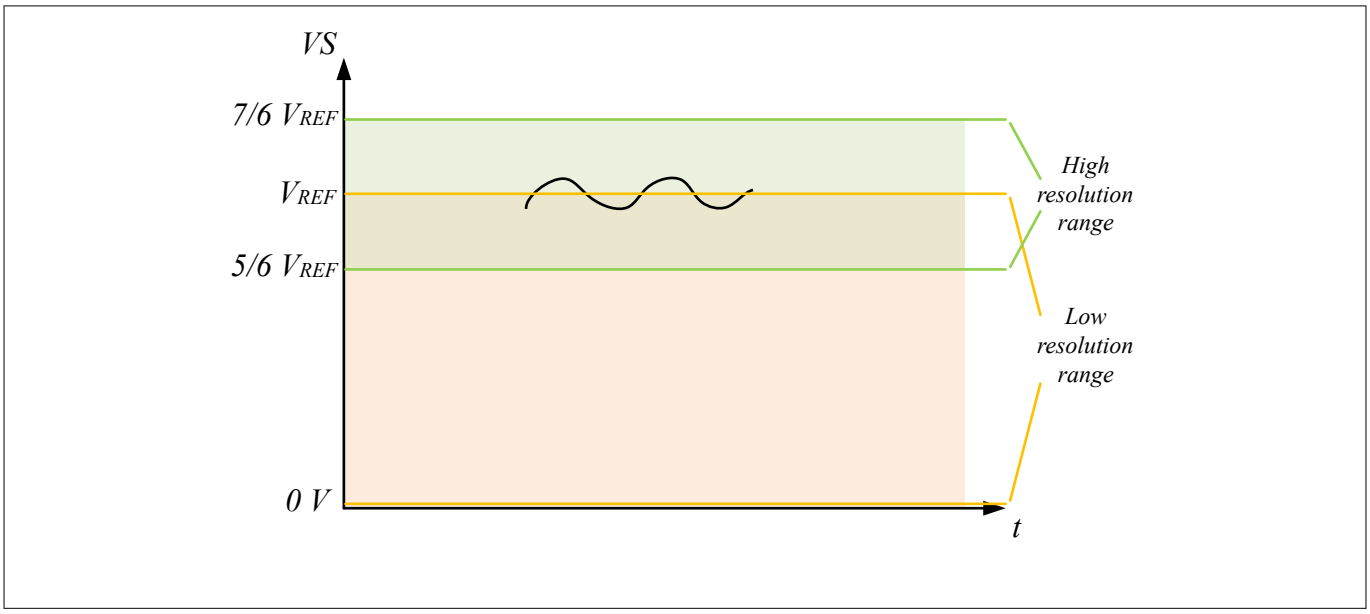

Figure 7 Sensing Ranges

3.1.4 Input Voltage Sensing

The input voltage is sensed using the HV pin.

The input voltage is used for protection, to generate ***AC*** zero-crossing signals and to detect the AC/DC source.

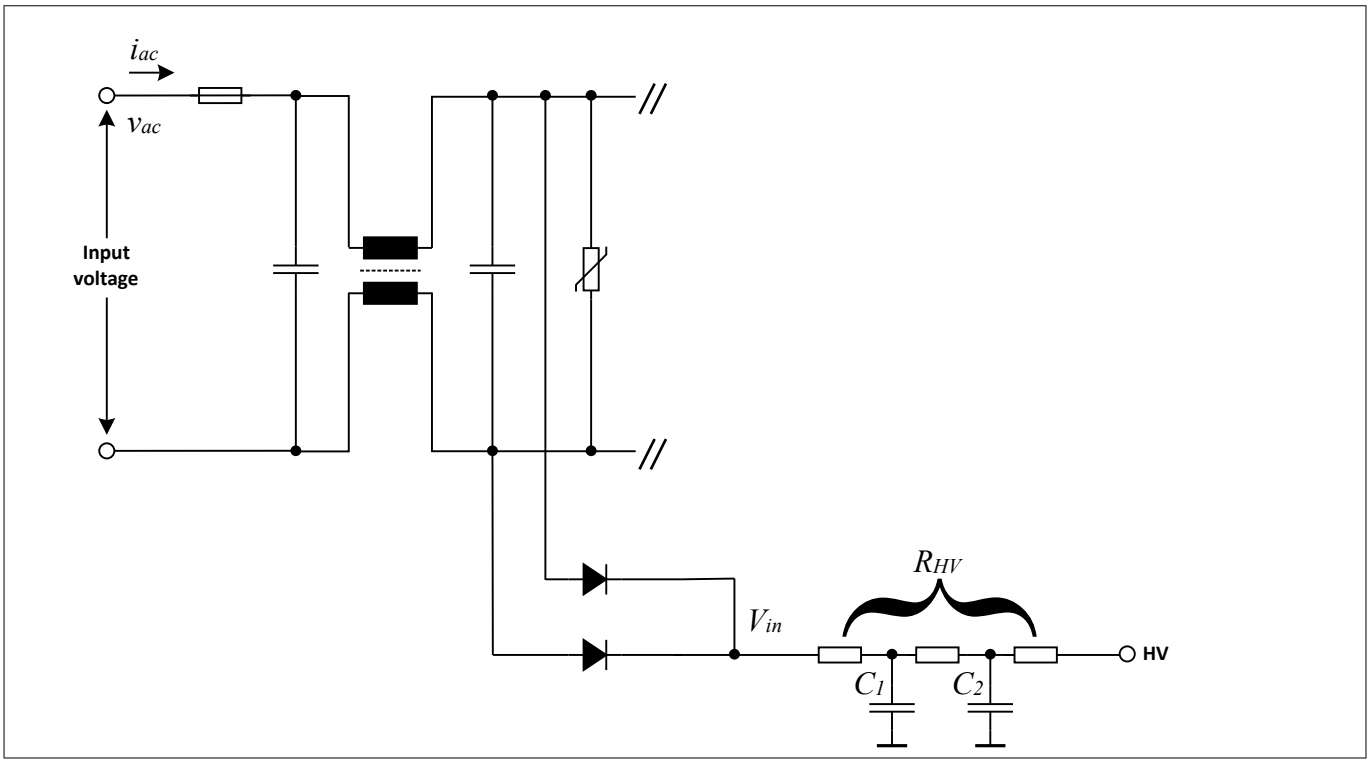

Figure 8 Input Voltage Sensing Schematic

The R_{HV} probing resistor is usually split into two, or three or more resistors for safety purposes. In fact in case of a resistor being shorted by damage, the high resistive path is maintained by the other resistors avoiding fire, shock to the user and further damage to the application.

A RC filter structure making use of the split resistors filters the unwanted noise for the high voltage input voltage measurement. The filtering effect is kept high due to the usage of the high impedance split resistors and the addition of small capacitance high voltage capacitors.

3.1.5 Control Scheme

The ***PFC*** bus voltage controller embeds a PIT1 controller that calculates a control output representing load and line conditions from the bus voltage error signal.

The bus voltage controller implements regulation during both soft start and steady states.

3.1.5.1 Startup

At system startup, the ***PFC*** initiates a soft start to minimize the switching stress for the power MOSFET, diode and inductor.

The soft start is executed when the bus voltage is higher than the $V_{bus,start,PFC}$ threshold. This is the brown-in condition. The soft start is aborted if the input under- or overvoltage protection fire. During soft start, the ***PFC*** stays in ***QRM1*** operation. Once the $V_{bus,stdy,entr,UV}$ threshold is reached, the steady state ***PFC*** operation starts.

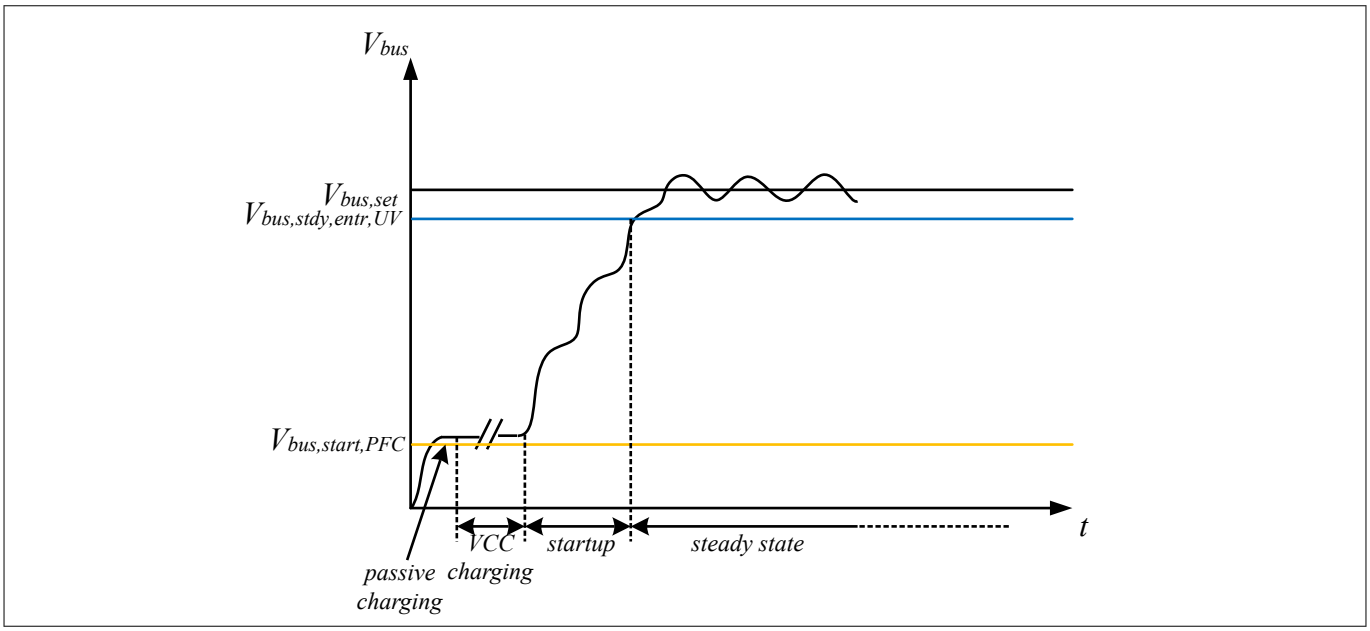

Figure 9 V_{bus} Soft Start and Regulation

3.1.6 Multimode Control Scheme

The multimode control scheme provides a ***PFC*** option to dynamically change the operating point by switching between the MOSFET V_{ds} voltage valleys while following a frequency law and applying ***THD*** optimization.

The multimode controller uses two different modes of operation:

- ***QRM1***: This operation maximizes the efficiency by switching on the 1st valley of the ***PFC*** ZCD signal. This ensures zero current switching with a minimum of switching losses.
- ***QRMn***: The controller will extend to the next switching valley after the 1st valley to control the bus voltage following a frequency law.

The multimode optimization consists of the following:

- Frequency law
- THD optimization

3.1.6.1 Frequency Law

The output of the ***PFC*** PIT1 bus voltage controller gives the desired on-time, which is constant within each ***AC*** half cycle. A ***PFC*** is used to emulate a resistive load r_e to the ***AC*** input such that i_{ac} follows v_{ac} in both wave shape and phase. The output of the ***PFC*** bus voltage controller $t_{on,des,PFC}$ is inversely proportional to the emulated resistive load r_e such that a smaller r_e or a higher $I_{ac,rms}$ will give a larger $t_{on,des,PFC}$. Thus, $t_{on,des,PFC}$ is different for the same load at different line voltages and is proportional to the RMS input current $I_{ac,rms}$.

The rule for selecting ***QRMn*** is based on the frequency law. A maximum switching frequency f_{swmax} and a minimum switching frequency f_{swmin} are defined for the complete $t_{on,des,PFC}/I_{ac,rms}$ range. The frequency law ensures that the switching frequency is within the desired frequency range. The frequency law is depicted in the figure below.

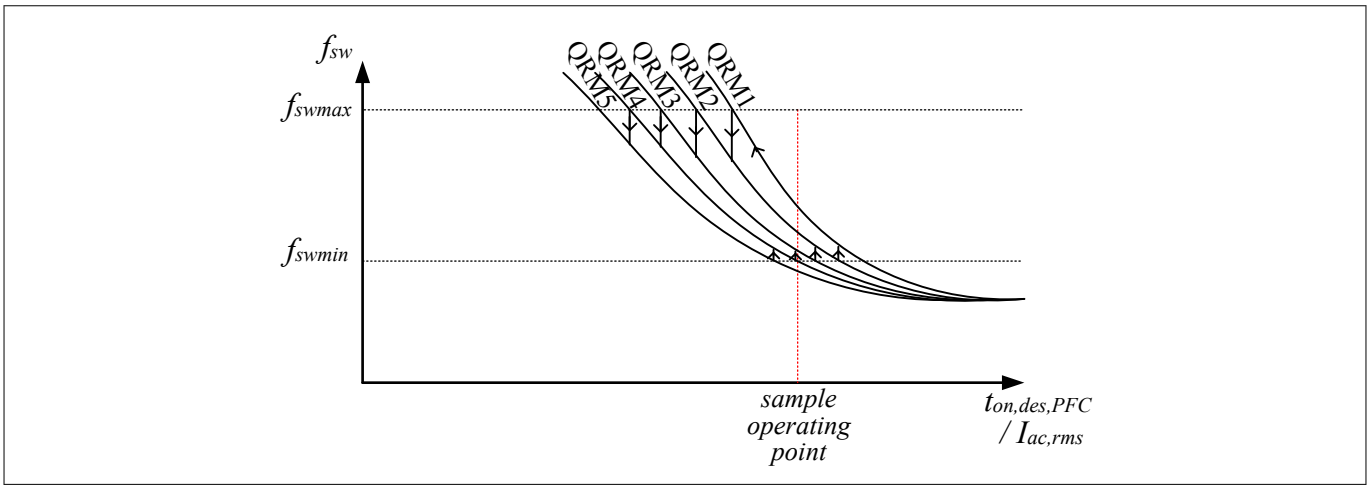

Figure 10 PFC Frequency Law

As long as the ***PFC*** controller operating mode fulfills the frequency law, the operating mode does not change. The QR-valley is increased when the highest frequency limit is reached. The QR-valley is decremented when the lowest frequency limit is reached.

To ensure good ZCD detection before the ZCD signal becomes too small in amplitude, only the first up to $N_{valley,max,PFC}$ valleys operations are supported.

3.1.6.2 THD Optimization

THD optimization reduces the ***THD*** in the case of light loads and in the case of high ***AC*** input voltages.

The selection of higher valleys helps to reduce the switching frequency but it also distorts the input current waveform with constant on-time control and thus affects the ***PFC THD*** performance. The multimode ***PFC*** control also consists of a ***THD*** optimization algorithm that optimizes the applied on-time in order to ensure good input current shaping and improved ***PFC THD*** performance.

3.1.7 Peak Current Limitation

The peak current through the switching MOSFET is read via the ***PFC*** shunt resistor $R_{CS,PFC}$ to limit the maximum current through the MOSFET, the choke, and freewheeling diode so as to avoid potential hard failure or lifetime stress.

The OCP causes the current to be limited to cases in which an overcurrent condition occurs. ***Overcurrent Protection Level 1 (OCP1)*** is implemented by hardware. If the voltage $V_{CS,PFC}$ across the shunt resistor exceeds the overcurrent threshold $V_{CS,OCP1,\ PFC}$ for longer than the blanking time $t_{blank,OCP1,PFC}$, the MOSFET is turned off. The MOSFET is turned on when ZCD occurs or the PFC maximum period time-out signal triggers the start of the next switching cycle. ***Overcurrent Protection Level 2 (OCP2)*** is a second-level overcurrent protection implemented by hardware. The ***OCP2*** overcurrent threshold is fixed. The ***OCP2*** blanking time is $t_{blank,OCP2,PFC}$.

3.1.8 Bus Undervoltage Protection

Undervoltage detection of the bus voltage V_{bus} is provided by measurement using the VS pin.

The bus voltage is compared to a configurable undervoltage protection threshold $V_{bus,UV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,Vbus,UV}$, the protection will be triggered.

3.1.9 Bus Overvoltage Protection

Overvoltage detection of the bus voltage V_{bus} is provided by the measurement using the VS pin.

The bus voltage is compared to a configurable overvoltage protection threshold $V_{bus,OVP1}$ in ***Firmware (FW)***. If a threshold is exceeded for longer than the blanking time $t_{blank,Vbus,OVP1}$, the gate driver stops. The gate driver operation is resumed when V_{bus} falls below $V_{bus,stdy,entr,OV}$.

$V_{bus,OVP2}$ is implemented in ***Hardware (HW)*** and it is fixed at a voltage which is represented as 2.8 V at the bus voltage sensing pin (VS). The HW permits a blanking time $t_{blank,Vbus,OVP2}$ to be programmed.

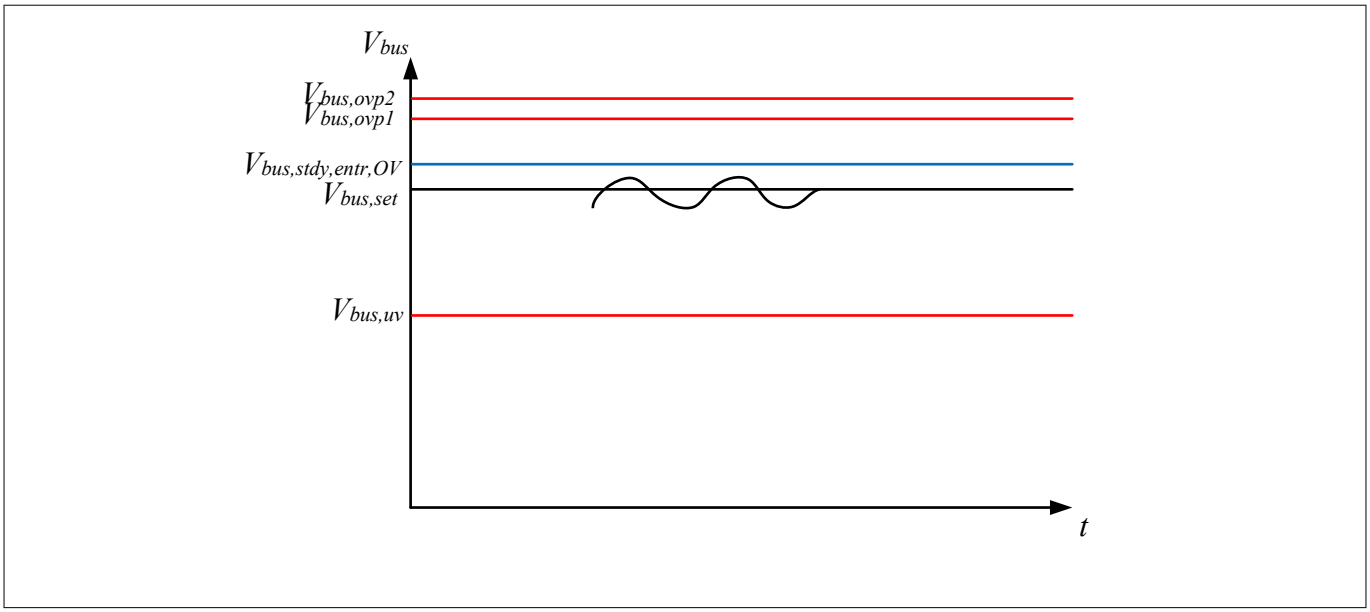

Figure 11 V_{bus} protections

3.1.10 Input Undervoltage Protection

Undervoltage detection of the input voltage V_{in} is provided by measurement using the HV pin.

Values of $V_{in,rms}$ are compared to a configurable input undervoltage protection threshold $V_{in,UV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,Vin,UV}$, the protection will be triggered. XDPL8220 features a configurable startup threshold $V_{in,start,min}$ to create hysteresis for flicker-free operation before the second stage starts switching. After startup checks when $t_{rms,reset,PFC}$ expires, the comparison is restored to the threshold value $V_{in,UV}$.

3.1.11 Input Overvoltage Protection

Overvoltage detection of the input voltage V_{in} is provided by measurement using the HV pin.

Values of $V_{in,rms}$ are compared to a configurable input overvoltage protection threshold $V_{in,OV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,Vin,OV}$, the protection will be triggered. XDPL8220 features a configurable startup threshold $V_{in,start,max}$ to create hysteresis for flicker-free operation before the second stage starts switching. After startup checks when $t_{rms,reset,PFC}$ expires, the comparison is restored to the threshold value $V_{in,OV}$.

Note: *In the csv file the input OVP shall be disabled by default.*

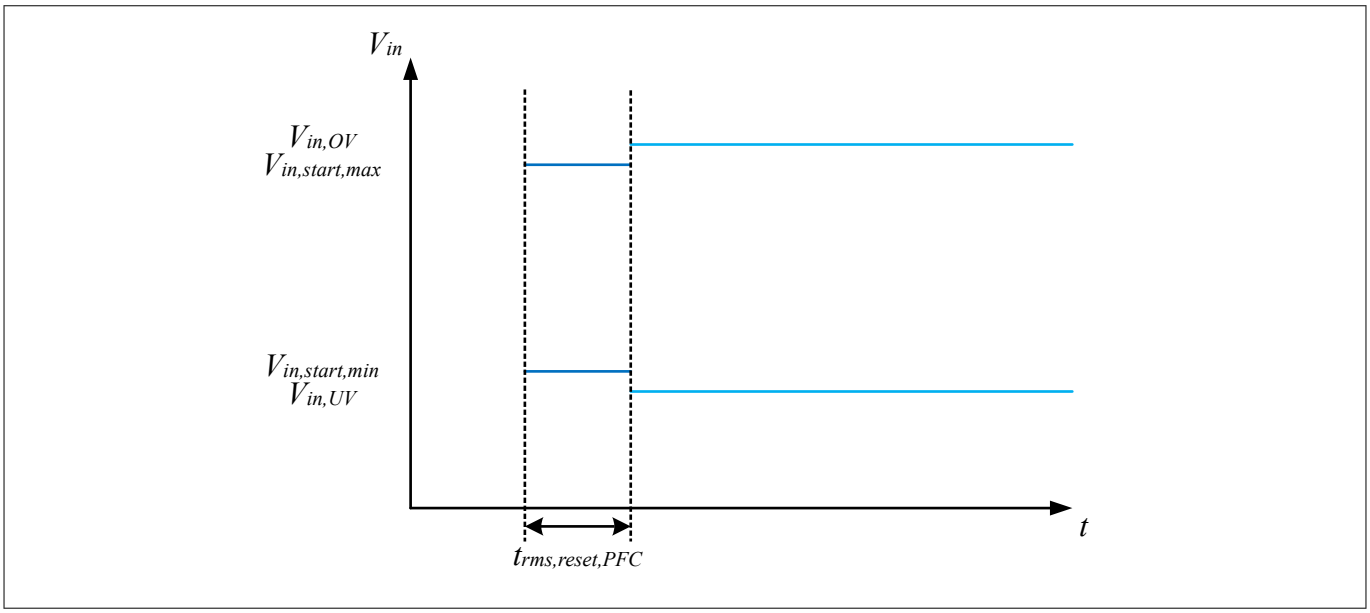

Figure 12 V_{in} protections

3.1.12 Other PFC Protections

CS Resistor Short Protection

The input circuit breaker (fuse) shall be chosen appropriately in order to protect in case of current-sense resistor short.

CS Resistor Open Protection

The external circuitry for shared CS/ZCD pulls the CSPFC pin high in case of CS resistor missing so that the OCP2 protection is triggered.

CSPFC Pin Short to GND Protection

In case of CSPFC pin short to ground the lack of quasi-resonant oscillations shall trigger the CCM Protection.

CCM Protection

Continuous conduction mode (CCM) operation may occur during ***PFC*** startup for a limited time. It is considered as a failure in the system only if CCM operation of the ***PFC*** converter is observed over a longer period of time. The ***PFC*** converter may run into CCM operation for a longer period due to a shorted bypass diode, a heavy load step that is out of specification or very low input voltage outside the normal operating range.

When CCM occurs, the magnetizing current in the ***PFC*** choke does not have the chance to decay to zero before the MOSFET turns on. No quasi-resonant oscillation will be seen at the ZCD signal before the maximum switching period time-out is reached that turns the MOSFET on. This turn-on event without ZCD oscillation is monitored to protect the ***PFC*** converter from continuous CCM operation. The CCM protection is implemented by firmware.

If any quasi-resonant oscillation is seen at the ZCD signal for longer than the blanking time $t_{blank,CCM,PFC}$, the protection is triggered.

Soft Start Failure

The soft start may take a long time, potentially never reaching steady state operation due to heavy loads or very low input voltages. If $t_{start,PFC}$ reaches $t_{start,max,PFC}$ before the soft start has ended, the protection is triggered.

3.2 Flyback Controller Features

The ***FB*** stage provides primary side control that avoids secondary side control feedback loop circuitry usually needed in isolated power converters. This approach supports a low part count to reduce costs.

The ***FB*** stage features multi-mode operation and it selects the best mode of operation based on operating conditions.

3.2.1 Primary Side Regulation

The ***FB*** in XDPL8220 provides primary side control of output current and output voltage. No external feedback components are necessary for the current control as the primary side regulation control loop is fully integrated.

Figure 13 shows typical current and voltage waveforms of the ***FB*** application operating in ***QRM1***.

In ***DCM***, the next switching cycle will not start at the first valley of V_{AUX}, but is instead delayed. As a consequence, the switching losses in ***DCM*** will be higher.

The primary peak current $I_{p,pk}$, the period of conduction of the output diode t_{demag} and the switching period $t_{sw,FB}$ are used to calculate the average output current.

The voltage signal V_{AUX} of the auxiliary winding of the transformer contains information on the reflected output voltage V_{out}. The reflected output voltage is measured at the ZCD pin using a resistor divider.

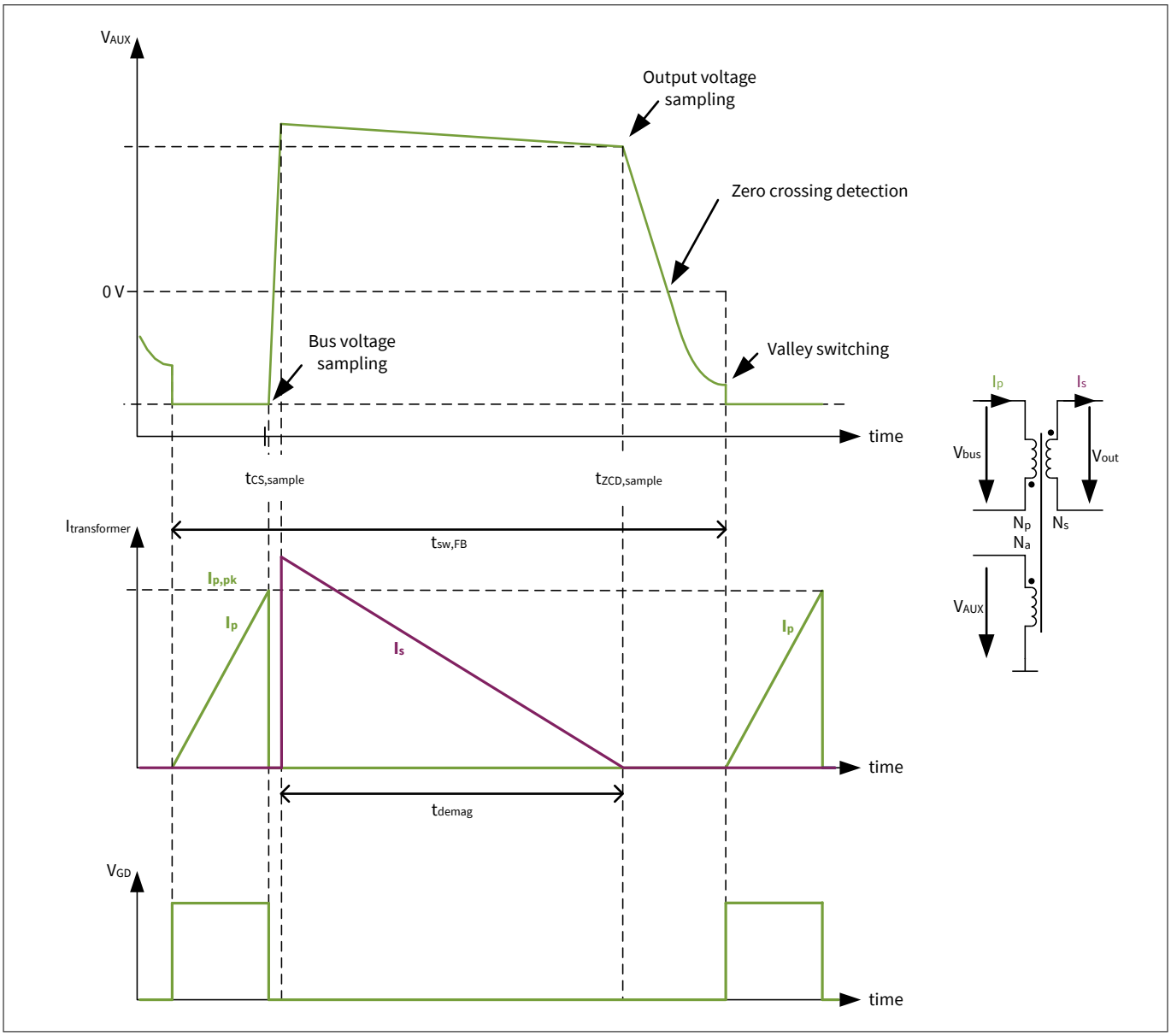

Figure 13 Typical Waveforms of a Flyback Converter

3.2.1.1 Primary Side Current Sensing

The primary side peak current $I_{p,pk}$ is controlled by the control loop using the $V_{CS,OCP1}$ level at the CSFB pin. This control scheme ensures suppression of any variation in the bus voltage.

Several delays exist from the time at which the ***OCP1*** level $V_{CS,OCP1}$ is exceeded at the CSFB pin until the gate switches off and the transformer current finally reaches its peak value. For a higher accuracy, the primary peak current $V_{CS,SH}$ is sampled a fixed time before turn-off of the gate. The primary side peak current is used to calculate the secondary side current and for protection. The propagation delay compensation parameter t_{PDC} allows optimization of the accuracy of the primary side peak current:

$$I_{p,pk} = \frac{V_{CS,SH}}{R_{CS,FB}} \cdot \frac{t_{on,FB} + t_{PDC}}{t_{on,FB} - t_{CSFB,offset}}$$

Equation 2

Note: *If an RC low pass filter is added in front of the CSFB pin, the related low pass filter delay has to be included in t_{PDC}.*

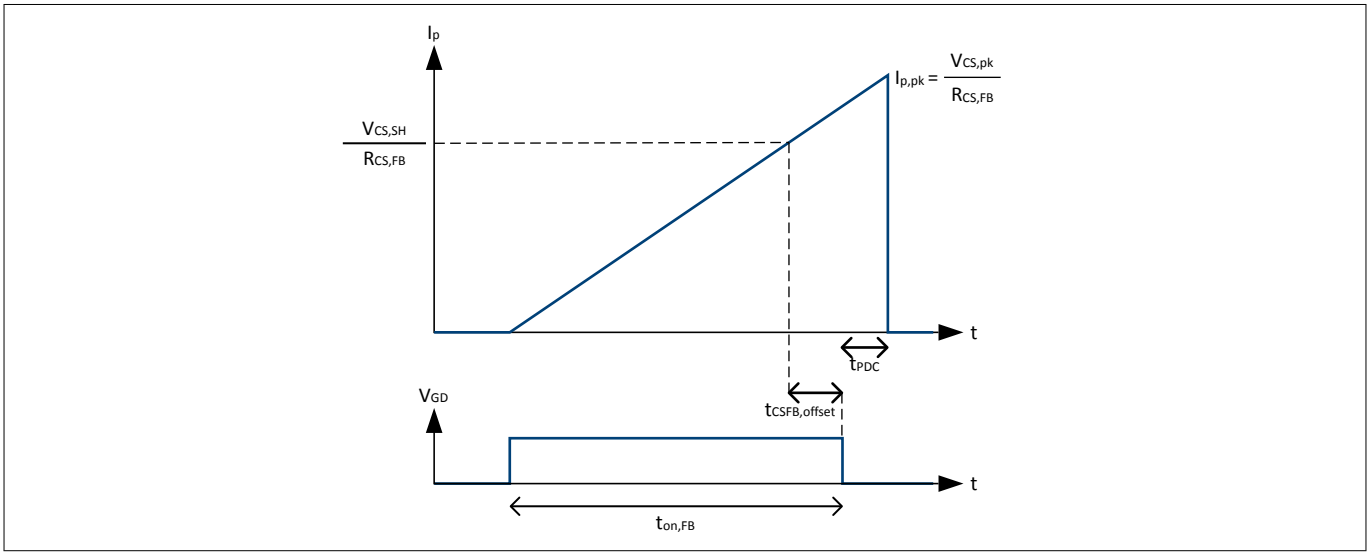

Figure 14 Propagation Delay Compensation for accurate Primary Peak Current Calculation

3.2.1.2 Primary Side Output Voltage Sensing

The output voltage is determined by measuring the reflected output voltage on the auxiliary winding. A resistor divider adapts the voltage to the operating range of the ZCD pin.

The output voltage is measured at the ZCD pin using the voltage $V_{ZCD,SH}$ at the end of the demagnetization time at the time $t_{ZCD,sample}$. The voltage measured at the ZCD pin, the dimensioning of the resistor dividers $R_{ZCD,FB,1}$ and $R_{ZCD,FB,2}$, transformer turns N_s and N_a as well as an offset $V_{out,offset}$ (caused by the secondary diode, for example) are used to calculate the output voltage V_{out} as follows:

$$V_{out} = V_{ZCD,SH} \frac{R_{ZCD,FB,1} + R_{ZCD,FB,2}}{R_{ZCD,FB,2}} \frac{N_s}{N_a} + V_{out,offset}$$

Equation 3

V_{out} is used for ***Primary Side Regulated (PSR)*** control loops in ***CV*** and ***LP*** modes as well as for output over- and undervoltage protections.

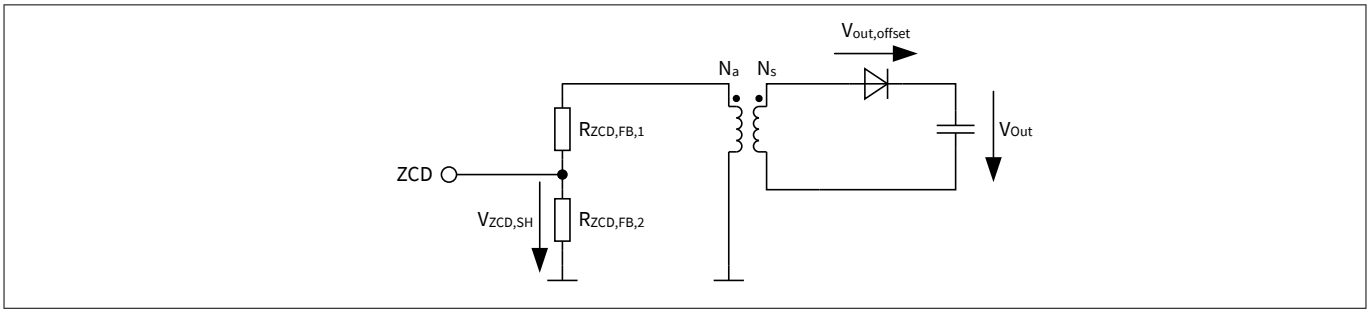

Figure 15 Primary Side Output Voltage Sensing using ZCD S&H

Note: *Any relation between VCC and ZCD in self-supplied applications can be decoupled – e.g. by adding a linear regulator for VCC.*

Attention: ***Please note that the time (t_{demag}) has to be longer than 2.0 µs to ensure that the reflected output voltage can be sensed correctly at the ZCD pin.***

3.2.1.3 Flyback Bus Voltage Sensing

The ***FB*** can sense the bus voltage using the reflection of bus voltage on the auxiliary winding while the gate is turned on. A resistor divider adapts the negative voltage to the operating range of the ZCD pin. This second measurement path is required to protect against component failures in the VS measurement path (open loop protection for the ***PFC*** stage).

The reflected bus voltage appears as a negative voltage at V_{AUX}. This negative voltage is internally clamped at the ZCD pin to the negative voltage V_{INPCLN}. The internal clamping current I_{ZCD} is measured at the end of the on-time at the time $t_{CS,sample}$. The measured clamping current of the ZCD pin, the dimensioning of the resistor dividers $R_{ZCD,FB,1}$ and $R_{ZCD,FB,2}$ as well as the number of transformer turns N_a and N_p are used to calculate the bus voltage $V_{bus,FB}$ as follows:

$$V_{\text{bus, FB}} = \left(\left(I_{\text{ZCD}} + \frac{V_{\text{INPCLN}}}{R_{\text{ZCD, FB, 2}}}\right) R_{\text{ZCD, FB, 1}} + V_{\text{INPCLN}}\right) \frac{N_p}{N_a}$$

Equation 4

$V_{bus,FB}$ is used for plausibility checks with the voltage V_{bus} as measured using the VS pin.

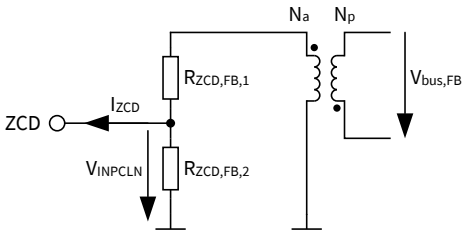

Figure 16 Voltage Sensing using ZCD Clamp Current

3.2.1.4 Output Current Calculation

The output current is calculated based on the primary side peak current and the timing of the switching cycle.

The output current I_{out} is calculated using the duration of conduction of the output diode t_{demag}, the switching period $t_{sw,FB}$ as well as the number of transformer turns N_p, N_s and the transformer coupling $K_{coupling}$. The following equation is valid both in ***QRM1*** and ***DCM***:

$$I_{\text{out}} = \frac{1}{2} I_{p,\text{pk}} \cdot \frac{N_p}{N_s} \cdot K_{\text{coupling}} \cdot \frac{t_{\text{demag}}}{t_{\text{sw, FB}}}$$

Equation 5

The coupling of the transformer can be approximated using the transformer primary inductance L_p and the transformer primary leakage inductance $L_{p,lk}$ as follows:

$$K_{\text{coupling}} \approx \frac{L_p}{L_p + L_{p,\text{lk}}}$$

Equation 6

The calculated current I_{out} is used for the control loop in the modes ***CC*** and ***LP***. The calculated current is also used for output overcurrent protection.

3.2.1.5 Output Control Scheme

The XDPL8220 includes three different control schemes for a ***CC***, ***CV*** or ***LP*** output.

Different use cases require the controller to operate according to different operation schemes:

- In the case of typical LED strings, the forward voltage of the LED string determines the output voltage of the driver. XDPL8220 operates in ***CC*** and drives a constant output current $I_{out,full}$ to the load. The forward voltage of the connected LED string has to be below a configurable maximum value $V_{out,set}$.
- In the case of LED loads including a power stage (e.g. Infineon BCR linear regulators or Infineon DC/DC buck ILD2111), XDPL8220 operates in ***CV***, ensuring a constant voltage $V_{out,set}$ to the load. The total output current drawn by the load has to be below a configurable maximum value $I_{out,full}$.
- In the case of a high output current setpoint $I_{out,full}$ and an overly long LED string which exceeds the configurable power limit $P_{out,set}$, XDPL8220 operates in ***LP*** to ensure that the power limit of the driver is not exceeded. The controller reduces the output current automatically, ensuring light output without any interruption even for overly long LED strings. The forward voltage of the connected LED string has to be below a configurable maximum value $V_{out,set}$.

For every update of the control loop, the control scheme is selected on the basis of the current operation conditions (output voltage V_{out} and output current I_{out}) and their distance to the three limiting setpoints ($V_{out,set}$, $P_{out,set}$ and $I_{out,full}$):

- For ***CC*** schemes, the internal reference current $I_{out,full}$ is weighted according to thermal management and a dimming curve to yield $I_{out,set}$. The calculated output current I_{out} is compared with the weighted reference current $I_{out,set}$ to generate an error signal for the output current.
- For ***CV*** schemes, the sensed output voltage V_{out} at the ZCD pin is compared to a reference voltage $V_{out,set}$ to generate an error signal for the output voltage.
- For ***LP*** schemes, the output current is limited to a maximum of $I_{out,set} = P_{out,set} / V_{out}$.

Out of these three schemes, for each step the most critical error is selected (see ***Figure 17***):

1. If any setpoint is exceeded, the largest error for power decrease is selected to bring the controller back to the desired operating point as quickly as possible.
2. If the current operating conditions are below all three setpoints, the smallest error for power increase is selected to avoid overshooting any setpoint.

The selected error signal is fed into a compensator to control the gate driver switching parameters (i.e. duty cycle and frequency) for the power MOSFET of the ***FB***.

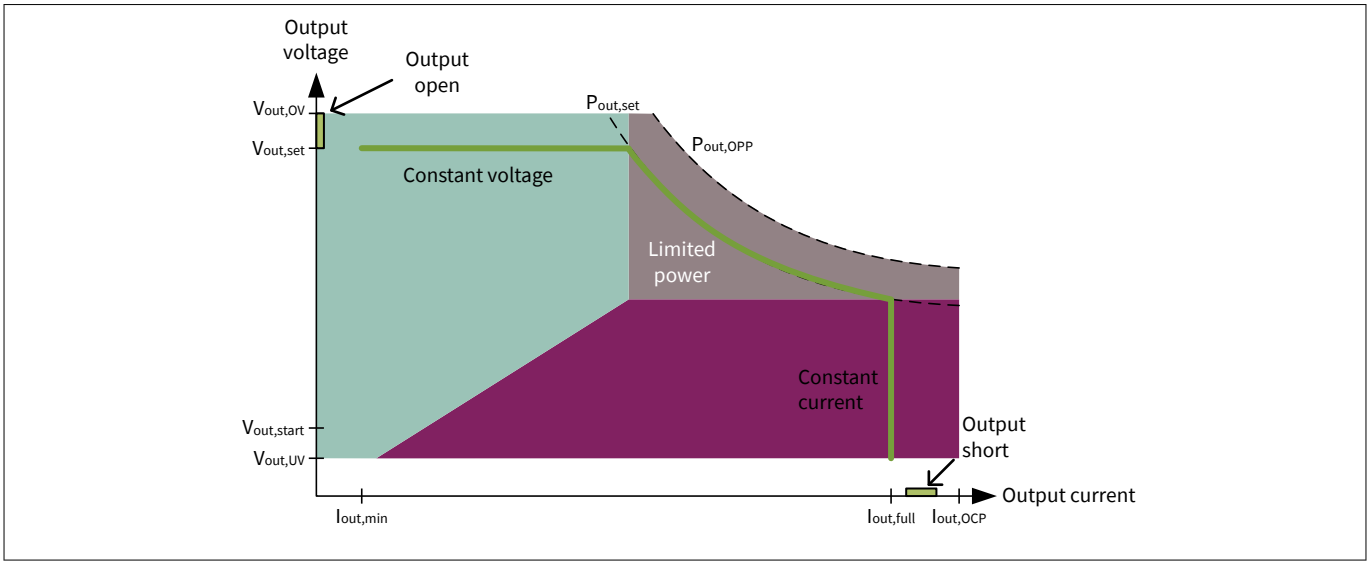

Figure 17 Control Scheme for CC/CV/LP Modes (Non-Dimmed)

In dimming cases, the output current setpoint $I_{out,set}$ is located between $I_{out,min}$ and $I_{out,full}$ and varies according to the sensed ***PWM*** duty cycle D_{DIM}. Dimming can be visualized by moving the vertical line for the output current setpoint in ***Figure 18*** from right to left.

Note: *An operation in limited power mode can cause dimmer dead-travel until the controller enters constant current mode.*

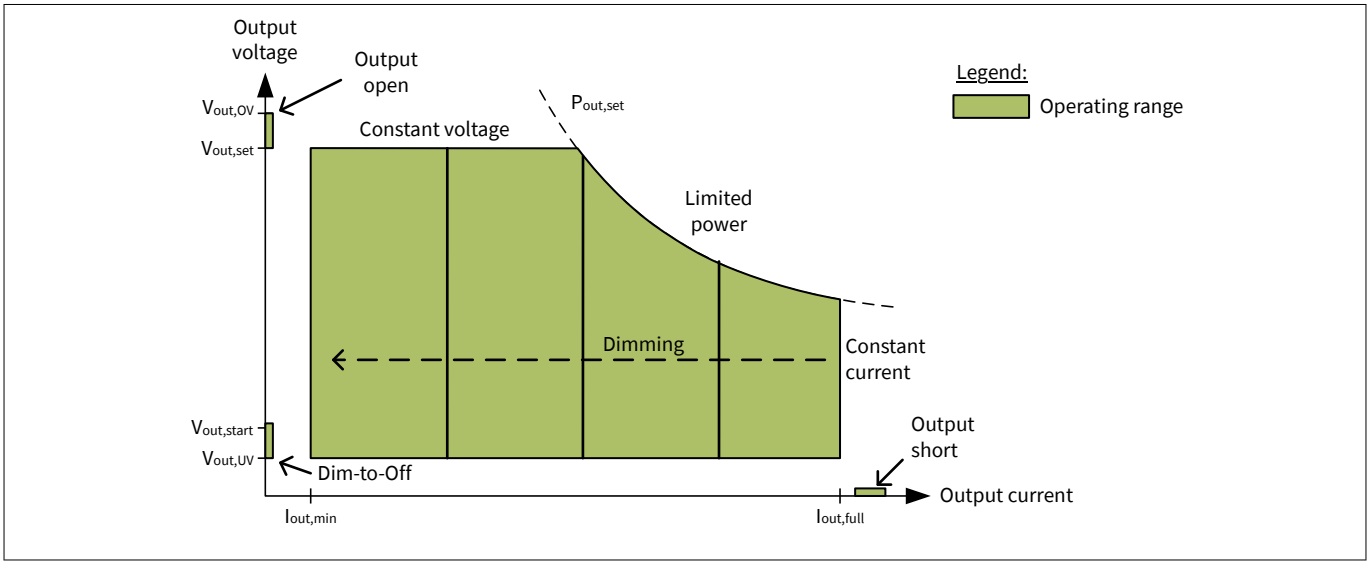

Figure 18 Control Scheme for CC/CV/LP Modes (including Dimming)

One or more of the output control schemes can be deactivated by configuration of the setpoints. Some examples are given below:

- The ***LP*** scheme is not active for $P_{out,set} > V_{out,set} * I_{out,full}$. For such a configuration, the controller will only select between a ***CC*** and ***CV*** scheme.
- The ***CV*** scheme is not active for $V_{out,set} = V_{out,OV}$ as the output overvoltage protection will be triggered.
- The ***CC*** scheme is not active for $I_{out,full} = I_{out,OC}$ as the output overcurrent protection will be triggered.

3.2.1.6 Multimode Scheme

The control loop of XDPL8220 uses two different switching modes. ***QRM1*** is optimized for high efficiency at high loads while ***DCM*** is used in light load conditions.

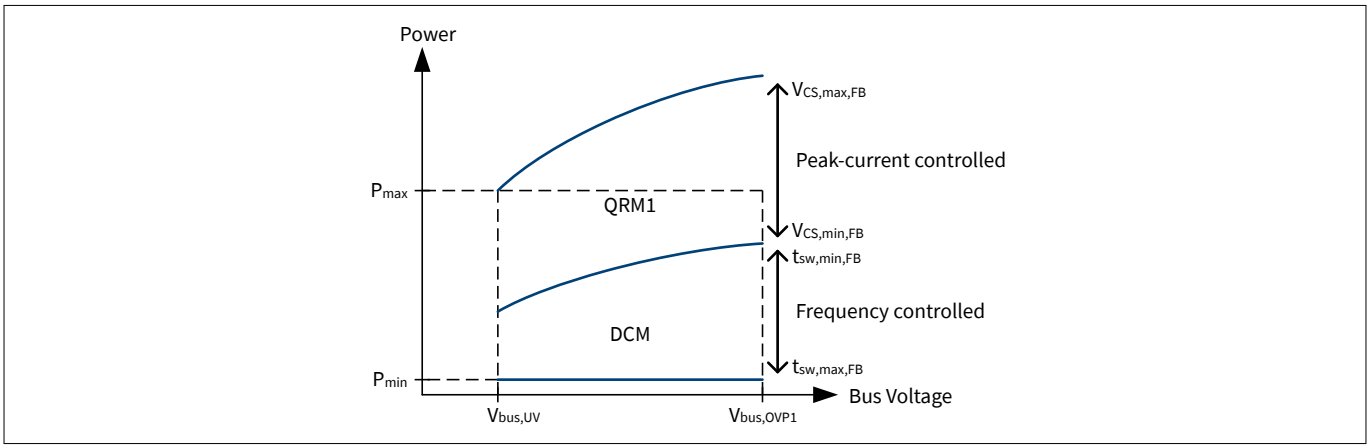

Figure 19 Flyback Multimode Operation Scheme

- ***QRM1***: This mode maximizes the efficiency by switching on the 1st valley of the V_{AUX} signal. This ensures zero current switching with a minimum of switching losses. The power is controlled by regulating the primary peak current using $V_{CS,OCP1}$.
- ***DCM***: This mode is used if $V_{CS,OCP1}$has reached its minimum value $V_{CS,min,FB}$. To allow lower output power, the controller extends the switching period later than the 1st valley .

The minimum power is limited by the transformer primary inductance L_p, maximum switching period $t_{sw,max,FB}$ and minimum primary peak current $I_{p,pk,min}$:

$$P_{min} = \frac{1}{2} \cdot L_p \cdot I_{p,pk,min}^2 \cdot \frac{1}{t_{sw,max,FB}}$$

Equation 7

The minimum primary peak current $I_{p,pk,min}$ is restricted by:

$$I_{p,pk,min} = t_{demag,min} \cdot \frac{N_p}{N_s} \cdot \frac{V_{out,OV}}{L_p}$$

Equation 8

Note: *If the load drops below the minimum load of P_{min}, the output voltage will rise up to the output overvoltage threshold $V_{out,OV}$ and trigger the protection. An auto-restart can be used to keep the output voltage close to $V_{out,OV}$ until the load increases again.*

3.2.2 Flyback Startup

After startup, the ***FB*** of the XDPL8220 initiates a soft start to minimize the switching stress for the power MOSFET and secondary diode.

The cycle-by-cycle current limit is increased in steps of $V_{CS,step}$ with a configurable duration $t_{softstart}$ for each step. After the final $V_{CS,OCP1,start}$ limit level has been reached, the output will be charged until the minimum output voltage $V_{out,start}$, which ensures self-supply has been reached. At this condition, ***Continuous Conduction Mode (CCM)*** protection as well as output undervoltage protection are activated and the control loop takes over. The starting point for the control loop is to operate in DCM at lowest switching frequency and shortest on-time. These switching parameters avoid any overshoot of output current for short LED string in dimmed conditions.

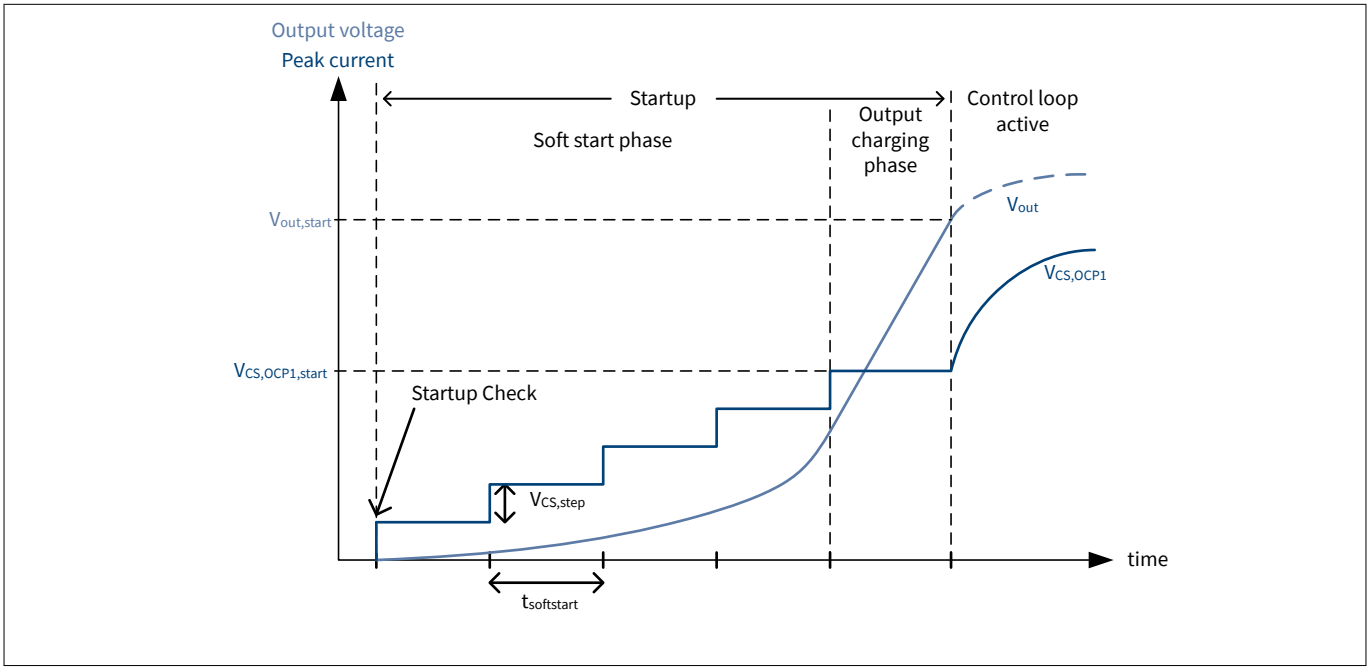

Figure 20 Flyback Startup Sequence

3.2.3 Protection Features

Protections ensure the operation of the controller under restricted conditions. Protections are triggered if fault conditions are present longer than the blanking times configured for each protection[3)]. The controller will react to a triggered protection as configured.

Attention: ***The controller may continue operation after exceeding protection thresholds because of blanking times. All protection thresholds have to be set with respect to tolerances, blanking times and worst case transients.***

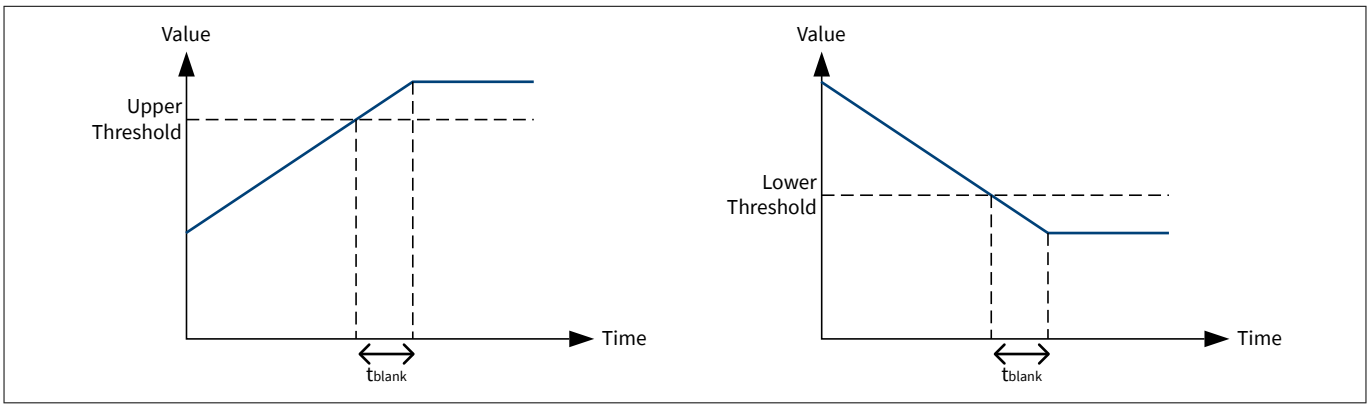

Figure 21 Blanking Times cause Excess of Threshold

3.2.3.1 Primary Overcurrent Protection

The primary side overcurrent protection implemented in hardware covers fault conditions like a short in the transformer primary winding or an open CS pin.

The primary side current is compared to a configurable overcurrent protection threshold $V_{CS,OCP2}$. If the threshold is exceeded for longer than the blanking time $t_{OCP2,FB}$, the protection will be triggered.

3.2.3.2 Output Undervoltage Protection

In the case of a short in the output, the output voltage may drop to a very low level. Detection of undervoltage in the output voltage V_{out} is enabled by measurement of the reflected voltage at the ZCD pin.

During operation, the output voltage is compared to a configurable undervoltage protection threshold $V_{out,UV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,UV}$, the protection will be triggered. This protection threshold $V_{out,UV}$ is disabled during startup.

During startup, the protection operates differently: In case the ***FB*** cannot charge the output voltage to $V_{out,start}$ during a timeout of $t_{start,max,FB}$, the protection will be triggered. This timeout starts when the ***FB*** is started.

Note: *The startup threshold $V_{out,start}$ has to be configured over and above the undervoltage threshold $V_{out,UV}$ to allow undershoots at startup which may occur, especially for resistive loads.*

3.2.3.3 Output Overvoltage Protection

In case of a open output, the output voltage may rise to a high level. Overvoltage detection of the output voltage V_{out} is provided by measurement at the ZCD pin.

The output voltage is compared to a configurable overvoltage protection threshold $V_{out,OV}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,OV}$, the protection will be triggered.

3 except VCC undervoltage protection

Note: *The blanking time $t_{blank,Vout,OV}$ should be set to the minimum value to minimize overshoots of the output voltage above the protection threshold.*

Note: *This protection is usually triggered if the output is open or the output load drops below the minimum load P_{min}.*

3.2.3.4 Output Overcurrent Protection

Overcurrent detection in the output current I_{out} is provided on the basis of the calculated output current.

The calculated output current is compared to a configurable overcurrent protection threshold $I_{out,OC}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,OC}$, the protection will be triggered.

3.2.3.5 Output Overpower Protection

Overpower detection in the output power P_{out} is provided on the basis of the calculated output power.

The calculated output power is compared to a configurable overpower protection threshold $P_{out,OP}$. If the threshold is exceeded for longer than the blanking time $t_{blank,out,OP}$, the protection will be triggered.

3.2.3.6 Other Flyback Protections

XDPL8220 includes additional protections to ensure the integrity and correct flow of the firmware.

- A hardware weak pull-up protects against an open CSFB pin.
- A firmware watchdog protects against the CSFB pin becoming shorted to GND.
- A firmware state monitor supervises correct operation of the flyback in ***QRM1*** or ***DCM***. A protection is triggered if the flyback enters ***CCM***.
- A firmware check ensures that the ***PFC*** has already boosted the bus voltage sufficiently before the ***FB*** starts.
- A firmware plausibility check ensures that the bus voltage measurement using the VS pin is correct.