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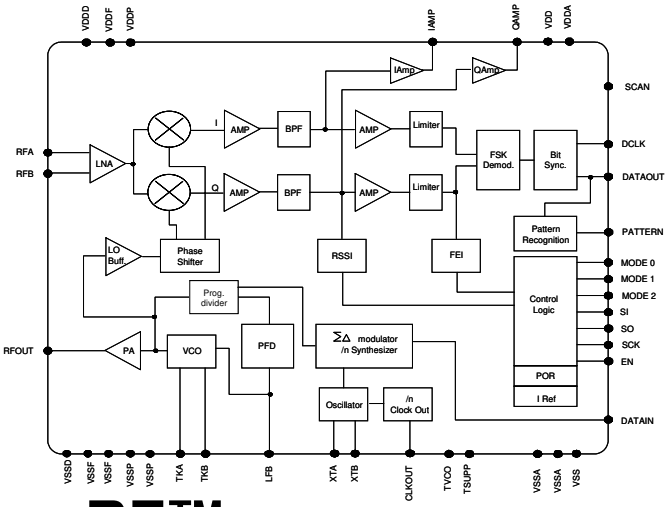

XE1202A TrueRF™

433 MHz / 868 MHz / 915 MHz

Low-Power, Integrated UHF Transceiver

GENERAL DESCRIPTION

The XE1202A TrueRF™ is a single chip transceiver operating in the 433, 868 and 915 MHz license free ISM (Industry Scientific and Medical) frequency bands. Its highly integrated architecture allows for minimum external components while maintaining design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The XE1202A TrueRF™ offers a wide range of channel bandwidths, without the need to modify the number or parameters of the external components. The XE1202A TrueRF™ is optimized for low power consumption whilst offering high RF output power and channelized operation suitable for both the European (ETSI-300-220) and the North American (FCC part 15) regulatory standards.

APPLICATIONS

Security systems
Voice and data over an RF link
Process and building control
Access control
Home automation
Home appliances interconnection

KEY PRODUCT FEATURES

Programmable RF output power: up to +15 dBm
High reception sensitivity: down to –116 dBm
Low power consumption: RX = 14 mA; TX = 62mA @15 dBm output power
Supply voltage down to 2.4 V
Data rates from 4.8 kbits/s to 76.8 kbits/s, NRZ coding
Channel filter bandwidths from 20 kHz to 400 kHz
On-chip frequency synthesizer with minimum frequency resolution of 500 Hz
Continuous phase 2-level FSK modulation
Incoming data pattern recognition
Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery
RSSI (Received Signal Strength Indicator) and FEI (Frequency Error Indicator)

ORDERING INFORMATION

Part number	Temperature range	Package
XE1202AI027TRLF	-40 °C to +85 °C	LQFP44

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The XE1202A TrueRF™ UHF Transceiver IC provides a single chip solution intended for use as a low cost FSK transceiver to establish a frequency-agile, half-duplex, bi-directional RF link, with non-return to zero data coding. The device is available in an LQFP44 package and is designed to provide a fully functional multi-channel FSK transceiver. It is intended for applications in the 433 and 868 MHz European bands and the North American 902-928 MHz ISM band. The single chip transceiver operates down to 2.4 V and provides low power consumption solutions for battery-operated and power sensitive applications. Thanks to the low external components count, the XE1202A is ideal for small size, low-cost UHF links. Its reference board has no tunable components, which facilitates high volume cost sensitive production.

The XE1202A TrueRF™ can easily be interfaced to a controller such as the XEMICS' XE8000 Series of ultra low-power microcontrollers. The XE1202A TrueRF™ serial control registers are programmed by the MCU and the MCU manages the communication protocol.

1 Functional Block Diagram

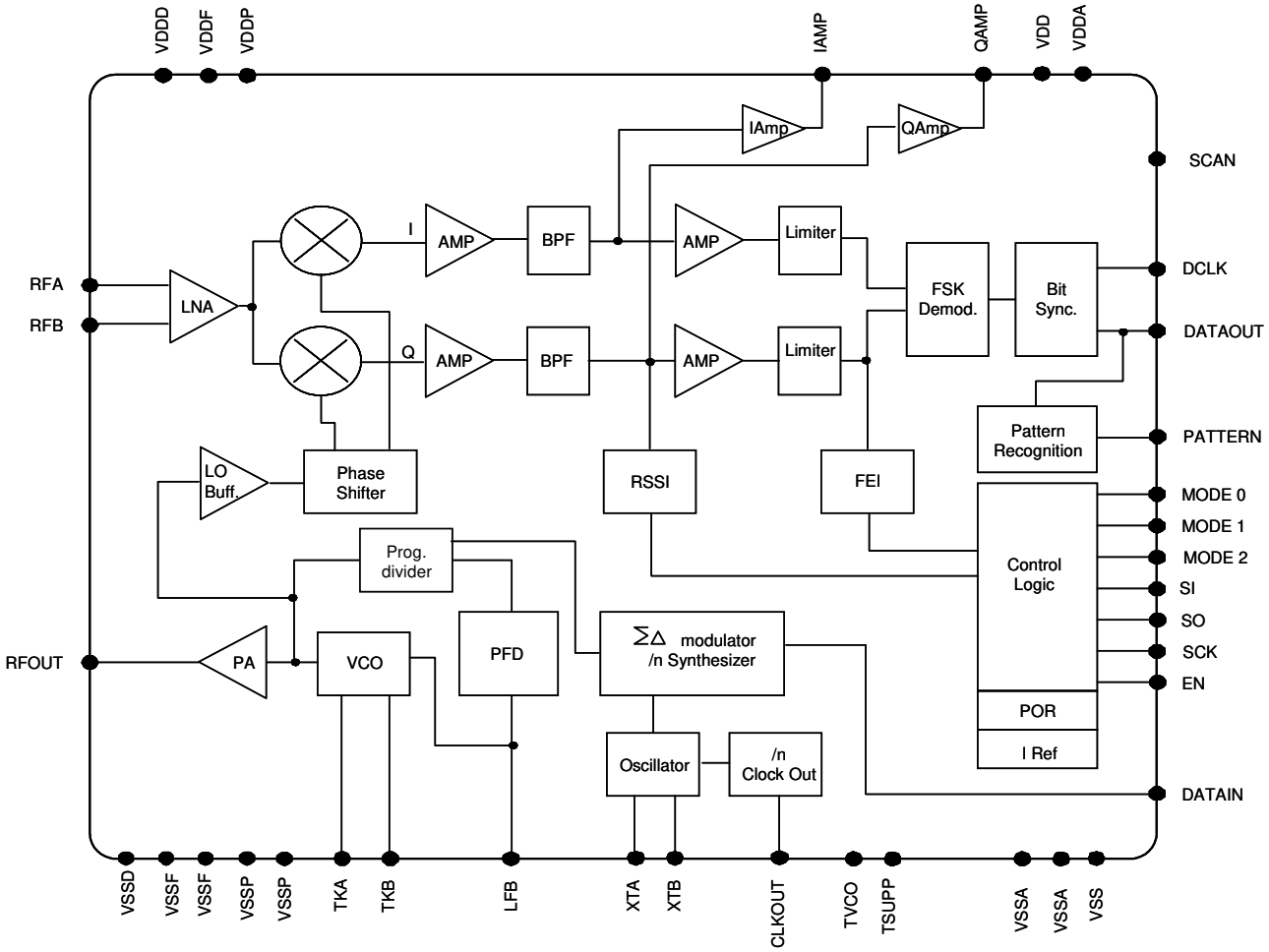

Figure 1: XE1202A TrueRF™ block diagram

2 Pin Description

PIN	NAME		DESCRIPTION
1	MODE(1)	In	Transmit/Receive/Standby/Sleep Mode Select
2	MODE(0)	In	Transmit/Receive/Standby/Sleep Mode Select
3	/EN	In	Chip Enable
4	VSSF		RF Analog Ground
5	RFA	In	RF Input
6	RFB	In	RF Input
7	VSSP	In	Power Amplifier Ground
8	VSSP	In	Power Amplifier Ground
9	RFOUT	Out	RF Output
10	VDDP		Power Amplifier Supply Voltage
11	VSSP		Power Amplifier Ground
12	VDD		RF Analog Supply Voltage
13	TKA	I/O	VCO Tank
14	TKB	I/O	VCO Tank
15	VSSF		RF Analog Ground
16	LFB	I/O	PLL Loop Filter
17	VDDD		RF Digital Supply Voltage
18	VSSD		RF Digital Ground
19	TSUPP		Test Circuit Supply Voltage (connected to VSS in normal operation)
20	SCAN	In	Scan Test Input (connected to VSS in normal operation)
21	OPT		(connected to VSS in normal operation)
22	TMOD[0]		(connected to VSS in normal operation)
23	TMOD[1]		(connected to VSS in normal operation)
24	VSSA		Analog Ground
25	XTA	I/O	Ref Xtal / Input of external clock
26	VSSA		Analog Ground
27	XTB	I/O	Reference Xtal
28	VDDA		Analog Supply Voltage
29	QAMP	Out	Buffered Q Output
30	IAMP	Out	Buffered I Output
31	TMOD[2]		(connected to VSS in normal operation)
32	TMOD[3]		(connected to VSS in normal operation)
33	TIBIAS		(connected to VSS in normal operation)
34	VDD		Digital Supply Voltage
35	SO	Out	Configuration Register Serial Output
36	SI	In	Configuration Register Serial Input
37	SCK	In	Configuration Register Serial Clock
38	CLKOUT	Out	Output clock at reference frequency divided by 4, 8, 16 or 32
39	VSS		Digital Ground
40	DCLK	Out	Recovered Received Data Clock
41	DATAOUT	Out	Received Data
42	DATAIN	In	Transmit Data
43	PATTERN	Out	Output of the pattern recognition block
44	MODE(2)	In	Transmit/Receive/Standby/Sleep Mode Select

Table 1: Pin Description

3 Electrical Characteristics

3.1 Absolute Maximum Operating Ranges

Stresses above those values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmax	Supply voltage	-0.4	3.9	V
ML	Receiver input level		-5	dBm
Tmax	Storage temperature	-55	125	°C

Table 2: Absolute Maximum Operating Ranges

The device is ESD sensitive and should be handled with precaution.

3.2 Specifications

3.2.1 Operating Range

Symbol	Description	Min.	Max.	Unit
VDD	Supply voltage	2.4 (*)	3.6	V
T	Temperature	-40	85	°C
CLop	Load capacitance on digital ports	-	25	pF

Table 3: Operating Range

(*) For narrow-band configurations (base-band filter bandwidths of 10, 20 and 40 kHz), the minimum operating supply voltage is 2.4 V. For 200 kHz base-band filter bandwidth setting the minimum operating supply voltage is 2.7 V.

3.2.2 Electrical Specifications

The table below gives the electrical specifications of the transceiver under the following conditions:
Supply Voltage = 3.3 V, temperature = 25 °C, 2-level FSK without pre-filtering, f_C = 434, 869 and 915 MHz, Δf = 5 kHz, Bit rate = 4.8 kbits/s, BW_{SSB} = 10 kHz, BER = 1 % (measured at the output of the bit synchronizer), LNA input and PA output matched to 50 Ω, environment as defined in section 6, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.2	1	µA
IDDST	Supply current in standby mode	Crystal oscillator (39 MHz) enabled	-	0.85	1.10	mA
IDDR	Supply current in receive mode		-	14	16.5	mA
IDDT	Supply current in transmitter mode	RFOP = 5 dBm RFOP = 15 dBm	- -	33 62	40 75	mA mA
RFS	RF sensitivity 869 / 915 MHz	A-mode B-mode	-	-116 -103	-113 -100	dBm dBm
	RF sensitivity 434 MHz	A-mode B-mode	-	-114 -100	-111 -98	dBm dBm
FDA	Frequency deviation	Programmable	- - - - -	5 10 20 40 100	- - - - -	kHz kHz kHz kHz kHz
CCR	Co-channel rejection		-13	-10	-	dBc

Symbol	Description	Conditions	Min	Typ	Max	Unit
IIP3	Input intercept point (from LNA input to base-band filter output)	$f_1 = f_{LO} + 1$ MHz, $f_2 = f_{LO} + 1.995$ MHz A-mode B-mode	 -36 -21	 -33 -18	 - -	 dBm dBm
BW	Base band filter bandwidth	Programmable	- - - -	10 20 40 200	- - - -	kHz kHz kHz kHz
ACR	Adjacent channel rejection 869 / 915 MHz	funw = f_{LO} + 65 kHz Pw=-107 dBm, A-mode	45	48	-	dBc
	Adjacent channel rejection 434 MHz	funw = f_{LO} + 65 kHz Pw=-102 dBm, A-mode	42	45	-	dBc
BR	Bit rate	Programmable	- - - - -	4.8 9.6 19.2 38.4 76.8	- - - - -	kbits/s kbits/s kbits/s kbits/s kbits/s
RFOP	RF output power	Programmable RFOP1 RFOP2 RFOP3 RFOP4	 -3 +2 +7 +12	 0 +5 +10 +15	 - - - -	 dBm dBm dBm dBm
FR	Synthesizer frequency range	Programmable Each range with its own external components	433 868 902	- - -	435 870 928	MHz MHz MHz
TS_BBR	Receiver baseband wake-up time (first step)	Crystal oscillator enabled	-	200	250	µs
TS_TR	Transmitter wake-up time	Frequency synthesizer enabled	-	100	150	µs
TS_FS	Frequency synthesizer wake-up time	Crystal oscillator enabled	-	200	250	µs
TS_BB2	Receiver RF Front-End wake-up time	Frequency synthesizer enabled RTParam_WBB=0	-	500	600	µs
TS_FSW	Frequency synthesizer switching time	Between 2 channels at 1 MHz channel spacing		100	150	µs
TS_RS	RSSI wake-up time (receiver operation in mode 100)	RSSI enabled during mode 010 0.5 ms before switching to mode 100 (see figure 8)	-	-	1.0	ms
		RSSI enabled during mode 100	-	-	1.5	ms
TS_RSM	RSSI measurement time		-	0.5	-	ms
TS_OS	Crystal oscillator wake-up time		-	0.3	0.5	ms

Symbol	Description	Conditions	Min	Typ	Max	Unit
TS_FE	FEI wake-up time (RTParam_Fsel = 1) FEI counting duration (RTParam_Fsel = 0)	Receiver enabled RTParam_Fsel = 1 RTParam_Fsel = 0	- -	- -	20/BR 4/BR	ms ms
FXTAL	Crystal oscillator frequency		-	39	-	MHz
FSTEP	Frequency synthesizer step	Exact step is XTAL / 77824	-	500	-	Hz
VTHR	Equivalent RSSI input thresholds	A-mode,low range:VTHR1 VTHR2 VTHR3 A-mode,high range:VTHR1 VTHR2 VTHR3	- - - - - -	-105 -100 -95 -90 -85 -80	- - - - - -	dBm dBm dBm dBm dBm dBm
FERR	FEI error threshold	Pw=-100 dBm, A-mode RTParam_Fsel = 1	-	0.5	-	-
SPR	Spurious emission in receiver mode	(1)	-	-65	-	dBm
VIH	Digital input level high	% VDD	75	-	-	%
VIL	Digital input level low	% VDD	-	-	25	%
VOH	Digital output level high	% VDD	75	-	-	%
VOL	Digital output level low	% VDD	-	-	25	%

Table 4: Electrical Specifications

SPR strongly depends on the design of the application board and the choice of the external components. Values down to -70 dBm can be achieved with careful design.

4 Description

The XE1202A TrueRF™ is a direct conversion (Zero-IF) half-duplex data transceiver. It includes a receiver, a transmitter, a frequency synthesizer and some service blocks. The circuit operates in the 3 ISM frequency bands (433 MHz, 868 MHz, 915 MHz) and uses 2-level FSK modulation/demodulation to provide a complete transmission link.

In a typical application, the XE1202A TrueRF™ is programmed by a microcontroller via the 3-wire serial bus, SI, SO, SCK to write to and read from the configuration registers.

The circuit consists of 5 main functional blocks:

The Receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream. The receiver is composed of a low-noise amplifier, down-conversion mixers, baseband filters, baseband amplifiers, limiters, demodulator and the bit synchronizer. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit stream DATAOUT and generates a synchronized clock, DCLK, which can be used to sample DATAOUT without requiring external signal processing. In addition, the receiver includes a Received Signal Strength Indicator (RSSI) function, a Frequency Error Indicator (FEI) function that provides an indication of local oscillator frequency error, and pattern recognition function to detect programmable reference words in the received bit stream. The bandwidth of the base-band filters, the frequency deviation of the expected incoming FSK signal as well as the bit rate of the received data are all programmable.

The Transmitter performs the modulation of the carrier by an input bit stream and the transmission of the modulated signal. Carrier modulation is achieved directly through the frequency synthesizer via a Sigma-Delta modulator. The frequency deviation and bit rate of the modulated carrier are programmable. An on-chip power amplifier then amplifies the signal. The output power can be programmed to one of 4 possible settings.

The Frequency Synthesizer generates the local oscillator (LO) signal for the receiver section as well as the continuous phase FSK (CPFSK) modulated signal for the transmitter section. The core of the synthesizer is implemented with a PLL structure. The frequency is programmable with a step size of 500 Hz in the 3 ISM frequency bands at 433, 868 and 915 MHz. This frequency synthesizer includes a crystal oscillator which provides the reference for the PLL. This reference frequency can be divided by 4, 8, 16 or 32 and available as CLKOUT to provide a clock signal for an external processor.

The Digital Interface provides internal control signals for the whole circuit according to the configuration register settings.

The Service Block provides the internal voltage and current sources and provides all the necessary functions for the circuit to work properly.

4.1 Detailed description

4.1.1 Receiver

The outputs of the receiver are the two signals DATAOUT and DCLK. When “RTParam_Bits” is set to “1” (see the Configuration register section below), the bit synchronizer is enabled, and the two output signals are the output NRZ demodulated data and the sampling clock, respectively. The function of the bit synchronizer is to remove the glitches from DATAOUT and to provide the output clock DCLK to sample the data. The value of DATAOUT is valid at the rising edge of DCLK.

To ensure correct operation of the bit synchronizer, the following three conditions must be satisfied:
the received data must start with a preamble of 24 bits for synchronization; this preamble must be a sequence of alternating “0” and “1”,
the received data must have at least one transition from “0” to “1” or from “1” to “0” every 8 bits,
the accuracy of the bit rate must be within ± 5 % of that programmed (assuming the reference Xtal oscillator is 39 MHz).

When “RTParam_Bits” is set to “0”, the bit synchronizer is turned off, and DATAOUT is the output of the demodulator. In this case DCLK is not used and its value is set “low”.

For guaranteed operation of the demodulator, the modulation index, β, of the modulated carrier should meet the following condition: $\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$

where Δf is the frequency deviation, and BR the bit rate.

Table 5 details typical sensitivity figures for different bit rates, frequency deviations and baseband filter bandwidths:

Bit rate [kbits/s]	Δf [kHz]	BW [kHz]	Sensitivity for 1 % BER [dBm]	
			mode A	mode B
4.8	5	10	-116	-103
	20	40	-117	-104
9.6	10	20	-115	-101
	20	40	-115.5	-102.5
19.2	20	40	-112.5	-99.5
	40	200	-109	-97.5
38.4	40	200	-107	-95
	100	200	-109	-97.5
76.8	100	200	-106.5	-95

Table 5: Sensitivity for 1 % BER

Figure 2 illustrates the typical BER curve under narrowband conditions:

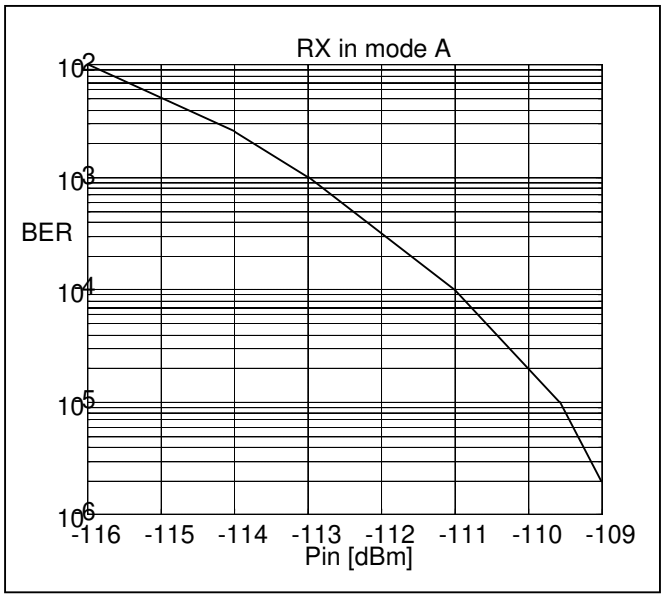

Figure 2: BER versus Rx input power with BR=4.8 kbits/s, Δf=5 kHz, BW=10 kHz

4.1.2 Receiver LNA modes

The receiver can be operated in two different modes that provide the highest sensitivity (for reception of weak signals) or the highest linearity (in areas of strong signals). The receiver mode is determined by the programming of the “RTParam_Rmode” register (see the Configuration register section below).
A-mode: high sensitivity mode (see RFS parameter)
B-mode: high linearity mode (see IIP3 parameter)

4.1.3 RSSI

When enabled, this function provides an RSSI (Received Signal Strength Indication) based on the signal at the output of the base-band filter. To enable the RSSI function, the bit "RTParam_RSSI" should be set to "1" (see the Configuration register section below). When enabled, the status of the RSSI is a 2-bit word stored in register "DataOut_RSSI", which can be read via the serial control interface. The contents of the register are defined in Table 6 below, where V_{RFFIL} is the differential amplitude of the equivalent input RF signal when the receiver is operated in A-mode. The thresholds VTHRi are the thresholds at the output of the base-band filter divided by the gain between the input of the receiver and this output.

DataOut_RSSI	Description
0 0	$V_{RFFIL} \leq$ VTHR1
0 1	VTHR1 < $V_{RFFIL} \leq$ VTHR2
1 0	VTHR2 < $V_{RFFIL} \leq$ VTHR3
1 1	VTHR3 < V_{RFFIL}

Table 6: RSSI status description

Two ranges, each of three VTHRi thresholds are defined and selected via the setting of the register "RTParam_RSSR", to provide an overall RSSI range of typically 25 dB.

The timing diagram of an RSSI measurement is illustrated by Figure 3 below. When the RSSI function has been activated the signal strength is periodically measured and the result is stored in the register "DataOut_RSSI" at each rising edge of DATAIN. TS_RS is the wake-up time required after the function has been enabled to ensure that a valid reading of RSSI is obtained. For a proper operation, the pulse length on DATAIN has to be higher than 8µs.

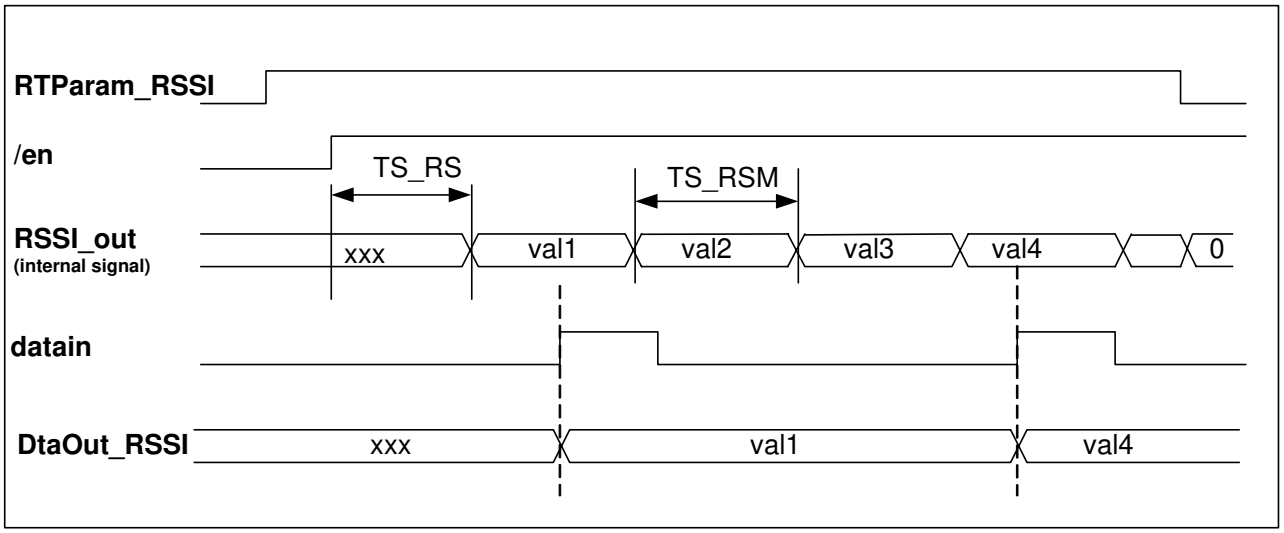

Figure 3: RSSI measurement timing diagram

For applications where a valid RSSI reading is required within as short a time frame as possible, enabling the RSSI during receiver mode 010 instead of 100 (see the definition of TS_RS in Table 4) allows a valid RSSI within 1 ms of valid data being received.

4.1.4 Frequency Error Indicator - FEI

When enabled, this function provides an indication of the frequency error of the local oscillator compared with the received carrier frequency. For guaranteed operation of the FEI function, the following two conditions should be satisfied.

The modulation index, b, of the modulated carrier should meet the following condition:

$$\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$$

where Δf is the frequency deviation and BR is the bit rate.

The bandwidth of the baseband filter (BBW) must be greater than the sum of the frequency offset and the received signal bandwith, as defined below:

$BBW > f_{OFFSET} + BW_{SIGNAL}$

where BBW is the baseband filter bandwidth defined by the RTParam_BW parameter (see the Configuration Registers section below), f_{OFFSET} is the difference between the carrier frequency and the LO frequency, and $BW_{SIGNAL}$is equal to $\left(\frac{BR}{2} + \Delta f\right)$.

The FEI function has two modes of operation, defined by the value set in the register “RTParam_Fsel” (see the Configuration register section below).

4.1.4.1 “RTParam_Fsel” = 1

With the “RTParam_FEI” bit set to “1” and the “RTParam_Fsel” bit set to “1”, the FEI uses frequency correlation to provide a 2-bit status word, which is stored in the register “DataOut_FEI”. The contents of this register are defined below in Table 7. The status of this register is provided in the following table, where f_{LO} is the internal local oscillator frequency, and f_{RF} is the carrier frequency of the received signal.

DataOut_FEI	Meaning
0 0	$\lvert f_{LO}-f_{RF} \rvert \leq f_{ERR}$
0 1	-
1 0	$(f_{LO}-f_{RF}) > f_{ERR}$
1 1	$(f_{LO}-f_{RF}) < -f_{ERR}$

Table 7: FEI status description

The value f_{ERR} = FERR * BR, where BR is the bit rate and FERR is a ratio given in the electrical specifications. As an example, for a bit rate of 4.8kbits/s and with FERR = 0.5, f_{ERR} is 2.4 kHz.

The FEI-Correlator function works properly only if the input signal is the preamble sequence defined under the Receiver section above, and if the frequency error to be detected is lower than 20 kHz.

The time diagram of an FEI measurement is similar to that of an RSSI measurement, and is illustrated in Figure 4 below. When the FEI is enabled, the frequency error is periodically measured and the result is stored in the register “DataOut_FEI” at each rising edge of DATAIN. TS_FE is the wake-up time required after the function has been enabled to obtain a valid result. For a proper operation, the pulse length on DATAIN has to be higher than 8µs.

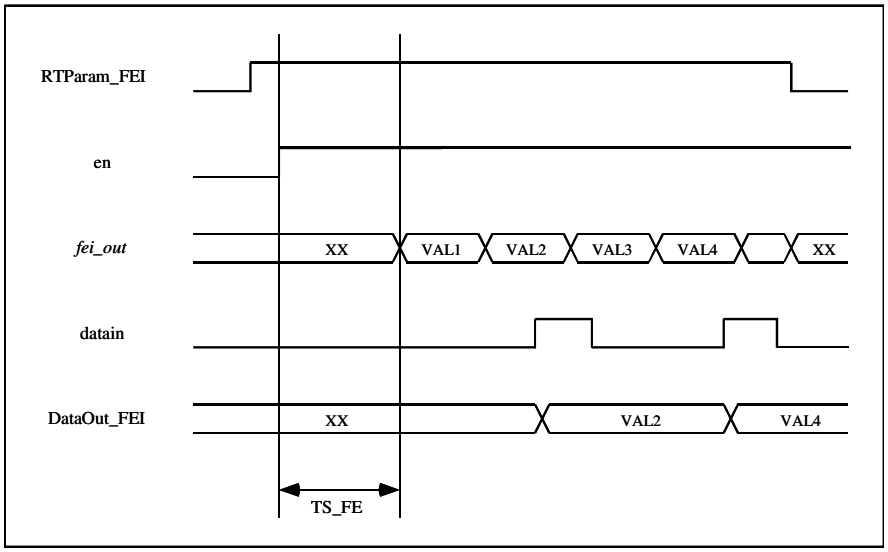

Figure 4: FEI measurement timing diagram when "RTParam_Fsel" = 1

4.1.4.2 "RTParam_Fsel" = 0

With the "RTParam_FEI" bit set to "1" and the RTParam_Fsel" bit set to "0", the FEI function uses over sampling of the signal at the output of the demodulator. When activated by the rising edge of DATAIN, this function provides an 8-bit word equivalent to the duty cycle of the demodulated preamble, stored in register "DataOut_FEI".

Each sample is used to control an up/down counter, when the sample is "1" the content of the counter is incremented, when the sample is "0" the content of the counter is decremented. As a consequence, the final 8-bit value of the counter stored in "DataOut_FEI" gives an indication of the duty cycle of the demodulated signal. The range of stored values is from -128 and +127. The further from 0 the value of DataOut_FEI, the higher the error on the LO frequency. If the stored value in "DataOut_FEI" is typically zero, then the duty cycle of the preamble is about 50 %, and the LO frequency is nominally correct.

Since this FEI uses the signal before the bit synchronizer, its value can vary from one measurement to another, due to the presence of jitter and glitches in the signal. If possible, it is advised to make 4-5 measurements and take the average value.

The timing diagram for this FEI measurement is illustrated in Figure 5 below. The FEI function is activated at the rising edge of the /EN signal when the RTParam_FEI bit is set to "1". Then, the internal FEI counter is activated at the rising edge of DATAIN. After a period TS_FE equal to the duration of 4 bits (see Electrical Specifications), the counter is stopped and the contents are stored in the register DataOut_FEI. For a proper operation, the pulse length on DATAIN has to be higher than 8µs.

The maximum delay between the rising edge of DATAIN and the first clock on the internal FEI counter is 1/(16*BR), where BR is the bit rate.

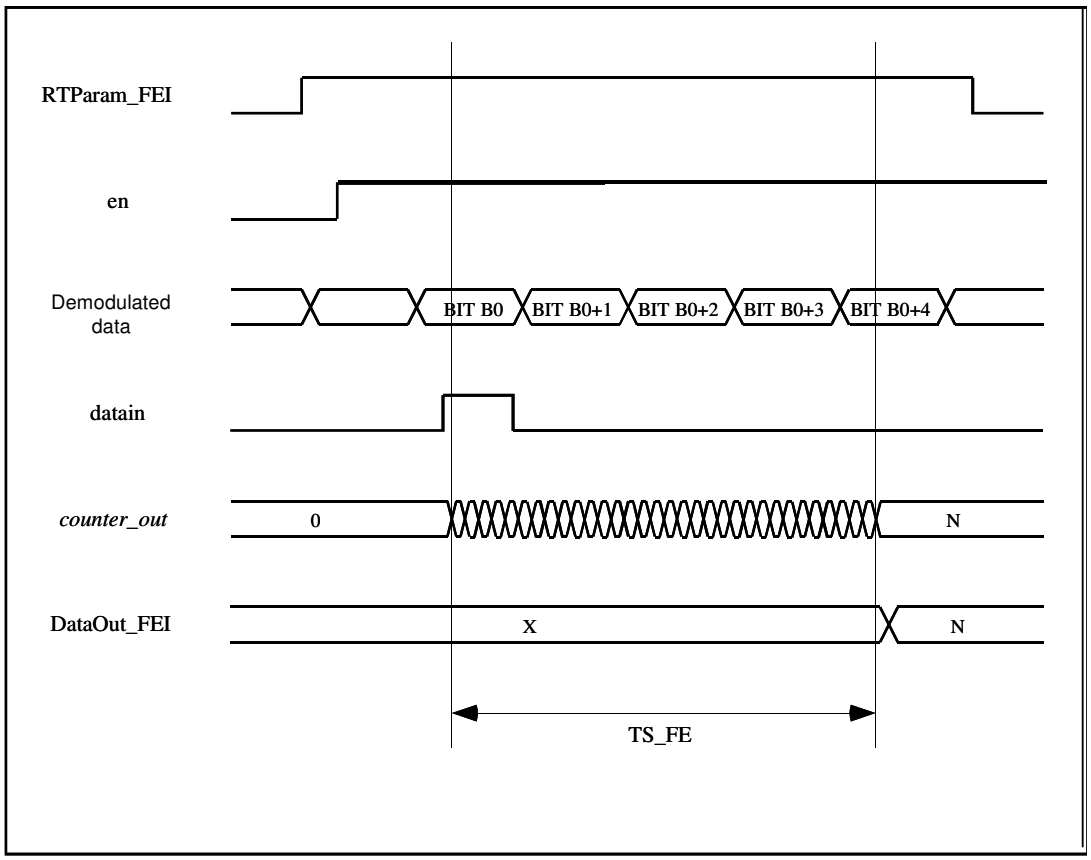

Figure 5: Timing diagram of an FEI measurement when "RTParam_Fsel" = 0
(the number of transitions on "counter_out" is for illustration only)

4.1.5 Transmitter

The output power of the power amplifier is programmable on four values with the register "RTParam_Tpow" (see the Configuration register section below), as shown in the table below, where RFOP values are given in Electrical Specifications section.

RTParam_Tpow	Output power
0 0	RFOP1
0 1	RFOP2
1 0	RFOP3
1 1	RFOP4

Table 8: output power settings

The degree of filtering of the baseband data prior to the modulation of the LO carrier frequency is programmable via the RTParam_Filter register:

- the input bit stream is directly applied to the frequency synthesizer without any pre-filtering (RTParam_Filter=0)
- the input bit stream is pre-filtered before being applied to the frequency synthesizer; with this filtering, each edge of the bit stream is linearly smoothed with a staircase transition (RTParam_Filter=1)

This is illustrated in Figure 6, where DATAIN is the input bit stream to be transmitted:

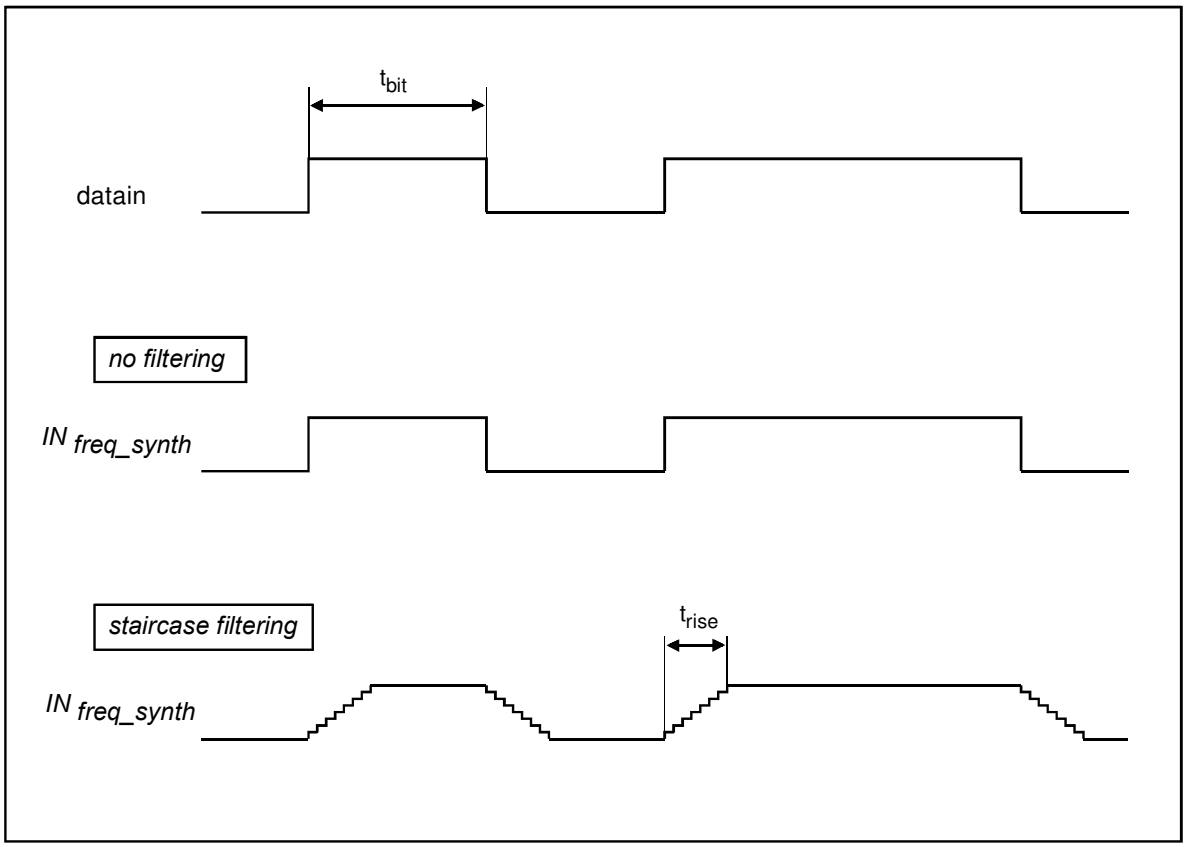

Figure 6: Modulation without and with pre-filtering

The characteristic of the smoothing filter is the ratio t_{rise}/t_{bit}. The value of this ratio is programmable with the register "RTParam_Stair", as illustrated in Table 9:

FSParam_Stair	t_{rise}/t_{bit}
0	10 %
1	20 %

Table 9: Smoothing filter

4.1.6 Pattern recognition

XE1202A TrueRF™ includes a pattern recognition function. When "ADParam_Pattern" (see the Configuration register section below) is set to "1" pattern recognition is enabled, providing that the bit synchronizer is also enabled. With the pattern recognition function enabled, the demodulated data is compared with a pattern stored in the "Pattern" register. The length of this pattern can be 8, 16, 24, or 32 bits, as defined by "ADParam_Psize". When comparing the streams 0, 1, 2, or 3 errors, as defined by "ADParam_Psize" can be allowed to detect a match. The PATTERN output is driven by the output of this comparator. It is "high" when a match is detected, otherwise "low".

When the feature is disabled, the PATTERN output is set to "low".

4.1.7 Frequency synthesizer

The exact frequency step of the frequency synthesizer can be obtained from the following equation:

FSTEP = FXTAL / 77 824.

As an example, if FXTAL is exactly 39 MHz, FSTEP = 501.13 Hz.

When the “RTParam_Clkout” bit is set high, FXTAL is frequency divided by 4, 8, 16, or 32, depending on the value of register “ADParam_Clkfreq” (see the Configuration register section below), and made available as CLKOUT, for use as clock signal for an MCU or external circuitry. If the reference frequency is 39 MHz, the available output frequency of CLKOUT is 1.22, 2.44, 4.87, or 9.75 MHz, respectively. When the XE1202A TrueRF™ is in Sleep Mode (MODE[2:0] = 000), CLKOUT is disabled.

5 Serial Interface Definition, Principles of Operation

5.1 Serial Control Interface

5.1.1 General description

A 3-wire bi-directional bus (SCK, SI, SO) is used to program the XE1202A TrueRF™ and read data from it. SCK and SI are input signals, for example generated by a microcontroller. SO is an output signal controlled by the XE1202A TrueRF™. In write mode, at the falling edge of the SCK signal, the logic data on the SI line is written into an internal shift register. In read mode, at the rising edge of the SCK signal, the data on the SO line becomes valid and should be sampled at the next falling edge of SCK.

The signal /EN must be low during the complete write and read sequences. In write mode the actual content of the configuration register is updated at the rising edge of the /EN signal. Before this, the new data is stored in temporary registers whose content does not affect the transceiver settings.

5.1.2 Write sequence

The time diagram of a write sequence is illustrated in Figure 7 below. This sequence is initiated when a Start condition is detected, defined by the SI signal being set to “0” during a period of SCK. The next bit is a read/write (R/W) bit which should be “0” to indicate a write operation. The next 5 bits are the address of the control register A[4:0] to be accessed, MSB first. Then the next 8 bits contain the data to be written in the register. The sequence ends with 2 stop bits set to “1”. The data on SI should change at the rising edges of SCK, and is sampled at the falling edge of SCK. After the 2 stop bits, the data transfer is terminated, even if the SI line stays at “1”. After this the SI line should be at “1” for at least one clock cycle on SCK before a new write or read sequence can start. This mode of operation allows data to be written to multiple registers without the need to alter the status of EN.

The maximum frequency of SCK is 1 MHz. The minimum clock pulse width is 0.5us. Set-up and hold time for SI on the falling edge of SCK is 200 ns, over the operating supply and temperature range.

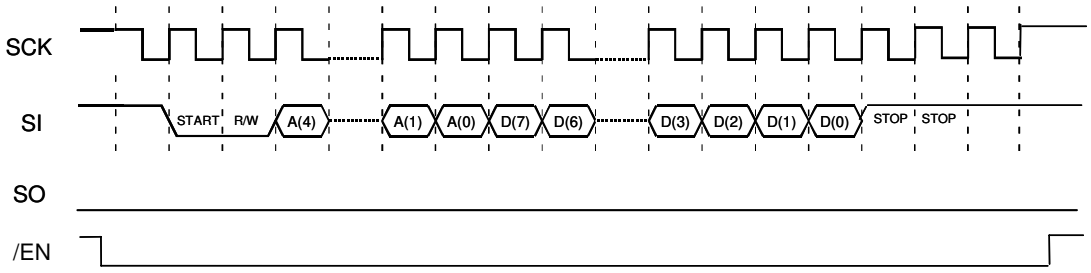

Figure 7: Write sequence into configuration register

5.1.3 Read sequence

The time diagram of a read sequence is illustrated in Figure 8. The sequence is initiated when a Start condition is detected, defined by the SI signal being set to “0” during a period of SCK. The next bit is a read/write (R/W) bit which should be “1” to indicate a read operation. The next 5 bits are the address of the control register A[4:0] to be accessed, MSB first. The data from the register is then output on the SO pin.

The data becomes valid at the rising edges of SCK and should be sampled at the falling edge of SCK. After this the data transfer is terminated. The SI line must stay high for at least one clock cycle on SCK to start a new write or read sequence. The maximum current drive on SO is 2 mA for a supply voltage of 2.7 V, and the maximum load is CLop, as defined in the Electrical Specifications.

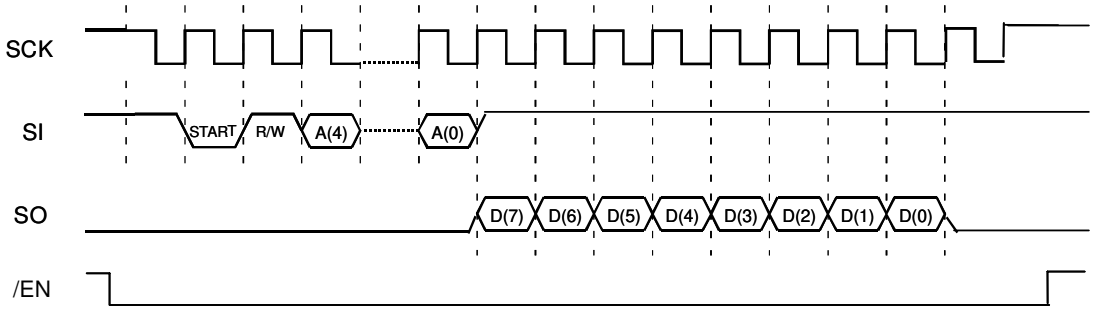

Figure 8: Read sequence into configuration register

When the serial interface is not used for read or write operations, both SCK and SI should be set to “1”.
Note that except in read mode, SO is set to “0” and cannot be configured in a high-impedance mode.

5.2 Configuration and Status registers

XE1202A TrueRF™ has a series of configuration registers programmable through the serial control interface described above. Their details are listed in Table 10 below. The size of these registers is 1, 2, 3, or 4 bytes. Their byte address is a 5 bit address, A[4:0]. In addition, there is one register, DataOut, from which users can read various transceiver status information.

Name	Size	Byte Address	Description
RTParam	2 x 8 bit	00000 00001	Receiver and transmitter parameters registers
FSParam	3 x 8 bit	00010 00011 00100	Frequency parameters
DataOut	1 x 8 bit	00101	Transceiver data register
ADParam Pattern	2 x 8 bit 4 x 8 bit	00110 00111 01000 01001 01010 01011	Additional parameters Reference pattern for the “pattern recognition” function

Table 10: Configuration registers

All the bits that are referred to as “reserved” in this section should be set to “0” during write operations.

5.2.1 RTParam configuration register

Name	Bits	Byte Address	Description
RTParam_Rmode	7	00000	Receiver modes: 0 -> A-mode (high sensitivity) 1 -> B-mode (high linearity)
RTParam_Bits	6	00000	Bit synchronizer on/off: 0 -> off; 1 -> on
RTParam_RSSI	5	00000	RSSI on/off: 0 -> off; 1 -> on
RTParam_FEI	4	00000	FEI on/off: 0 -> off; 1 -> on

Name	Bits	Byte Address	Description
RTParam_BW	3-2	00000	Bandwidth of the BB filter: 0 0 -> 10 kHz 0 1 -> 20 kHz 1 0 -> 40 kHz 1 1 -> 200 kHz
RTParam_Tpow	1-0	00000	Transmitter output power: 0 0 -> 0 dBm 0 1 -> 5 dBm 1 0 -> 10 dBm 1 1 -> 15 dBm
RTParam_Osc	7	00001	Source for the reference frequency: 0 -> on-chip crystal oscillator 1 -> external signal
RTParam_WBB	6	00001	Receiver wake-up type selection 0 -> “Boost” power up sequence 1 -> Standard power-up sequence
RTParam_Filter	5	00001	Pre-filtering of bit stream in transmitter mode: 0 -> no filtering; 1 -> filtering
RTParam_Fsel	4	00001	FEI mode: 0 -> FEI_Demodulator 1 -> FEI_Correlator
RTParam_Stair	3	00001	Rise and fall time when RTParam_Filter = 1: 0 -> 10 % of bit duration 1 -> 20 % of bit duration
RTParam_Modul	2	00001	Modulation switch: 0 -> modulation enabled; 1 -> modulation disabled
RTParam_RSSR	1	00001	RSSI range: 0 -> low range; 1 -> high range
RTParam_Clkout	0	00001	CLKOUT enable: 0 -> CLKOUT disabled 1 -> CLKOUT enabled (equal to FXTAL divided by 4, 8, 16 or 32)

Table 11: RTParam configuration register

5.2.2 FSParam configuration register

Name	Bits	Byte Address	Description
FSParam_Band	7-6	00010	Frequency band: 0 0 -> not valid 0 1 -> 433 – 435 MHz 1 0 -> 868 – 870 MHz 1 1 -> 902 – 928 MHz
FSParam_Dev	5-3	00010	Frequency deviation: 0 0 0 -> 5 kHz 0 0 1 -> 10 kHz 0 1 0 -> 20 kHz 0 1 1 -> 40 kHz 1 0 0 -> 100 kHz
FSParam_BR	2-0	00010	Bit rate: 0 0 0 -> 4.8 kbits/s 0 0 1 -> 9.6 kbits/s 0 1 0 -> 19.2 kbits/s 0 1 1 -> 38.4 kbits/s 1 0 0 -> 76.8 kbits/s others -> not valid
FSParam_Freq	7-0 7-0	00011 00100	LO frequency in 2's-complement representation: 00…0 -> f_{LO} = middle of the range 0X…X -> f_{LO} = higher than the middle of the range 1X…X -> f_{LO} = lower than the middle of the range MSB = bit 7 of byte at pos. 00011 LSB = bit 0 of byte at pos. 00100 See example below

Table 12: FSParam configuration register

Table 13 below provide an example of LO frequency setting in FSParam_Freq:

Byte Address 00011 Bit 7 Bit 0	Byte Address 00100 Bit 7 Bit 0	LO frequency Note: FXTAL = 39.0 MHz
00000000	00000000	F0, where F0 depends on the selected frequency band (see FSParam_Band) F0 = 434.0 MHz for the 433-435 MHz band F0 = 869.0 MHz for the 868-870 MHz band F0 = 915.0 MHz for the 902-928 MHz band
00000000	00000001	F0 + 500 Hz
00000000	00000010	F0 + 2 * 500 Hz
11111111	11111111	F0 – 500 Hz
11111111	11111110	F0 – 2 * 500 Hz

Table 13: LO Frequency setting

5.2.3 DataOut register

Name	Bits	Byte Address	Description
DataOut_RSSI	7-6	00101	RSSI output: 0 0 -> lowest level 0 1 -> 2nd level 1 0 -> 3rd level 1 1 -> highest level
DataOut_FEI When RTParam_Fsel = 0	7-0	00101	FEI output: Output of the up/down counter in 2's-complement representation MSB = bit 7
DataOut_FEI When RTParam_Fsel = 1	5-4	00101	FEI output: 0 0 -> frequency OK 1 0 -> frequency too low 1 1 -> frequency too high

Table 14: DataOut register

5.2.4 ADParam configuration register

Name	Bits	Byte Address	Description
ADParam_Pattern	7	00110	Pattern recognition enable: 0 -> Disabled 1 -> Enabled
ADParam_Psize	6-5	00110	Size of reference pattern recognition word: 0 0 -> 8 bits 0 1 -> 16 bits 1 0 -> 24 bits 1 1 -> 32 bits
ADParam_Ptol	4-3	00110	Number of tolerated errors for the pattern recognition: 0 0 -> 0 error 0 1 -> 1 error 1 0 -> 2 errors 1 1 -> 3 errors
ADParam_Clkfreq	2-1	00110	Frequency of CLKOUT: 0 0 -> 1.22 MHz (div. ratio: 32) 0 1 -> 2.44 MHz (div. ratio: 16) 1 0 -> 4.87 MHz (div. ratio: 8) 1 1 -> 9.75 MHz (div. ratio: 4)
ADParam_IQA	0	00110	IQ amplifiers enable: 0 -> Disabled 1 -> Enabled
ADParam_Res1	7	00111	Reserved. Should be set to "0"
ADParam_Invert	6	00111	Inversion of the Rx output data: 0 -> non-inverted data 1 -> inverted data

Name	Bits	Byte Address	Description
ADParam_RegBW	5	00111	Baseband filter bandwidth regulation: 0 -> Enabled 1 -> Disabled
ADParam_Regfreq	4	00111	Periodicity of baseband filter bandwidth regulation: 0 -> only at start-up of the receiver 1 -> every 60 seconds whilst receiver enabled
ADParam_Regcond	3	00111	Regulation process of the baseband filter bandwidth according to the selected bandwidth: 0 -> regulation restarted each time the bandwidth is changed 1 -> no regulation when bandwidth is changed
ADParam_WBBcond	2	00111	Boosting process of the baseband filter according to the selected bandwidth: 0 -> boosting restarted each time the bandwidth is changed 1 -> no boosting when bandwidth is changed
ADParam_Xsel	1	00111	Selection of the XOSC load capacitance mode: 0 -> CLop + C0 = 15 pF 1 -> CLop + C0 = 11 pF (low-current mode)
RESERVED	0	00111	RESERVED

Table 15: ADParam configuration register

5.2.5 Pattern register

The pattern register may be used to automatically detect the reception of a user-defined pattern and asserts the PATTERN signal for one bit duration. In this register, a reference pattern length of 8, 16, 24, or 32 bits (see ADParam_Psize parameter) may be defined. The first byte of the pattern is always stored at byte address A[4:0] (= 01000). If defined, the second and subsequent byte(s) are stored at address A[4:0] = 01001, and so on.

The MSB of the reference pattern is always bit 7 of the address 01000 and the LSB is bit 0 of address 01000, 01001, 01010, or 01011 if the pattern length is 8, 16, 24, or 32 bits, respectively.

Comparing the demodulated data, the first bit received of the last word (or second, third or fourth from last word, depending upon the value stored in the ADParam_Psize register) is compared with bit 7 (the MSB) of byte address 01000. The last bit received is compared with bit 0 (the LSB) in the Pattern register.

Name	Bits	Byte Address	Description
Pattern	7-0	01000 01001 01010 01011	1st byte of the reference pattern 2nd byte 3rd byte 4th byte

Table 16: Pattern register addresses

Table 17 below shows an example of pattern recognition with a 32-bit pattern:

Byte Address 01000 Bit 7 Bit 0	Byte Address 01001 Bit 7 Bit 0	Byte Address 01010 Bit 7 Bit 0	Byte Address 01011 Bit 7 Bit 0
10010011	10101010	10010011	10101010
101 10010011	10101010	10010011	10101010
	previous bits from demodulator		last bit received

Table 17: Pattern recognition example (32-bit)

Table 18 below shows an example of pattern recognition with an 8-bit pattern.

Byte Address 01000 Bit 7 Bit 0	Byte Address 01001 Bit 7 Bit 0	Byte Address 01010 Bit 7 Bit 0	Byte Address 01011 Bit 7 Bit 0
10010011	xxxxxxxx	xxxxxxxx	xxxxxxxx
101 10010011			
previous bits from demodulator	last bit received		

Table 18: Pattern recognition example (8-bit)

5.2.6 Supplementary configuration

Configuration settings to optimize device performance under certain operation conditions are described in Table 19 below:

Name	Bits	Byte Address	Description
TParam_BW	2	10011	Bandwidth decoding map: Baseband filter bandwidth (RTParam_BW): 0 -> default values: RTParam_BW(1:0) = 00 => 10 kHz RTParam_BW(1:0) = 01 => 20 kHz RTParam_BW(1:0) = 10 => 40 kHz RTParam_BW(1:0) = 11 => 200 kHz 1 -> new values: RTParam_BW(1:0) = 00 => 14.3 kHz RTParam_BW(1:0) = 01 => 28.5 kHz RTParam_BW(1:0) = 10 => 66.7 kHz RTParam_BW(1:0) = 11 => 100 kHz
TParam_HPF	5-3	10110	Cut-off frequency of the HPF stages allowing to cancel the DC and low-frequency offsets in the baseband circuit: 0 0 0 -> 660 Hz (default value) 0 0 1 -> 1.48 kHz 0 1 0 -> 1.75 kHz 0 1 1 -> 1.96 kHz 1 0 0 -> 2.55 kHz 1 0 1 -> 3.34 kHz 1 1 0 -> 5.11 kHz 1 1 1 -> 10.2 kHz

Table 19: Supplementary configuration

Using TParam_BW allows intermediate bandwidths to be accessed; these additional bandwidths can be selected to optimize the sensitivity and the selectivity of the applications for which the signal bandwidth is different from the 4 default filter bandwidths.

The wake-up time of the receiver may be reduced by increasing the cut-off frequency of the HPF stages. This is accomplished by changing the value of TParam_HPF.

Note that the selected cut-off frequency should be less than (Δf – (BR/2)) to avoid sensitivity degradation.

5.3 Operating Modes

The XE1202A TrueRF™ has 4 main operating modes as set by the MODE[2:0] inputs as illustrated in Table 20 below. Switching between modes is only possible when the /EN signal is low. The actual change will be applied to the transceiver upon the rising edge of the /EN signal.

Over the operating supply and temperature range, set-up and hold time for MODE[2:0] on the rising edge of /EN is 200 ns, while the negative pulse duration on /EN is 2 µs minimum. Please refer to Figure 9:

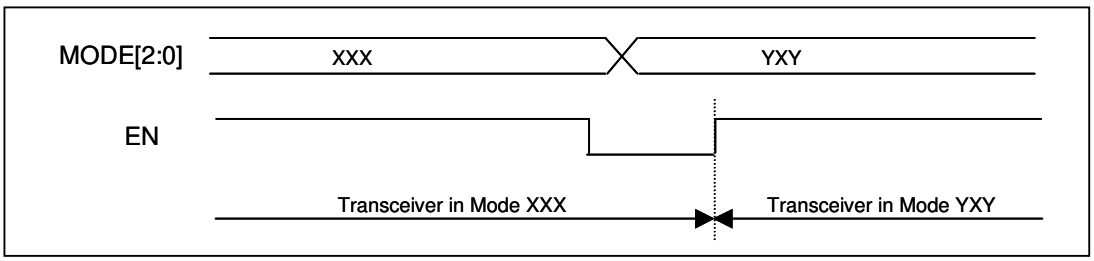

Figure 9: Switching mode sequence

Name	MODE(2:0)	Description
Sleep mode	0 0 0	-
Standby mode	0 0 1	Xtal oscillator enabled
Receiver mode	1 0 0	Xtal oscillator, Frequency synthesizer, Receiver enabled
Transmitter mode	1 1 1	Xtal oscillator, Frequency synthesizer, Transmitter enabled

Table 20: XE1202A Main operating modes

Three additional operating modes are defined and should be used when the transceiver is switched from the standby mode to the receiver or transmitter mode. These additional operating modes are illustrated in Table 21 below.

Name	MODE(2:0)	Description
Receiver mode	0 1 0	Xtal oscillator, Baseband enabled (first step)
	0 1 1	Xtal oscillator, Frequency synthesizer, Baseband enabled (first step)
Transmitter mode	1 1 0	Xtal oscillator, Frequency synthesizer enabled

Table 21: XE1202A Additional operating modes

The power up sequence from sleep to receiver mode is selected by setting the RTParam_WBB parameter to “0”. The sequence is described in Table 22 below:

Received data valid

Mode = 000	Mode = 001	Mode = 010	Mode = 011	Mode = 100	Mode=001
- Sleep	- Xtal oscillator enenabled	- Baseband - Xtal oscillator enabled	- Frequency synthesizer - Baseband - Xtal oscillator enabled	- RF Front End - Frequency synthesizer - Baseband - Xtal oscillator enabled	- Xtal oscillator enabled
	≥TS_OS	≥TS_BBR	≥TS_FS	≥TS_BB2	

Table 22: Power up sequence from Standby to Receive Mode

The typical current consumption values during the power-up sequence from Standby to Receive Mode are shown in Table 23 as follows:

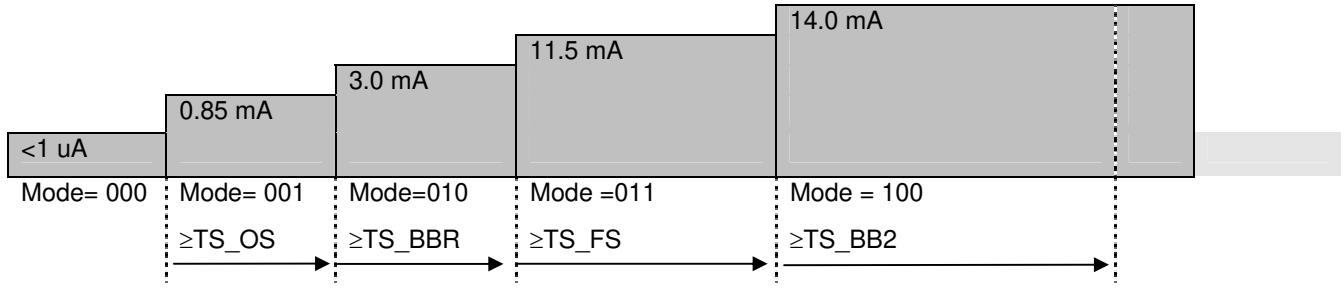

Table 23: Typical current consumption profile during the power up sequence from Standby to Receive Mode

The power up sequence from sleep to transmit mode is described in Table 24:

Mode = 000	Mode = 001	Mode = 110	Mode =111	Mode=001
- Sleep	- Xtal oscillator enabled	- Frequency synthesizer - Xtal oscillator enabled	- Power Amplifier - Frequency synthesizer - Xtal oscillator enabled	- Xtal oscillator enabled
	≥TS_OS	≥TS_FS	≥TS_TR	

Transmission

Table 24: Standard power up sequence from Standby to Transmit Mode

5.4 Transmitted Data Interface

When in transmit mode (MODE[2:0] = 111), the DATAIN signal is used as input for the on-chip modulator. DATAIN is not sampled, so the bit duration should match the bit rate setting of the receiver. Whenever XE1202A TrueRF™ are used on both sides of the communication link, the bit rate should be one of those defined in Table 4 (BR). In this case the bit rate error should be less than 5 % compared to the specified value.

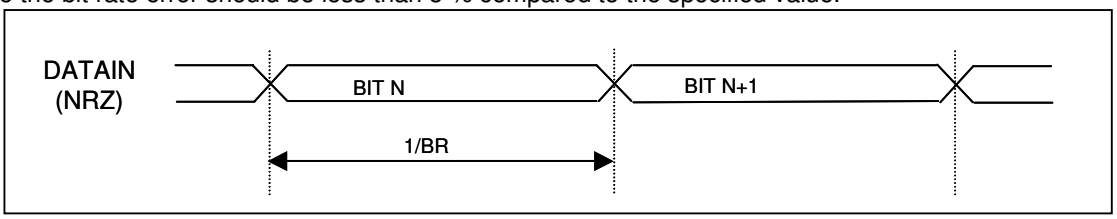

Figure 10: DATAIN timing

5.5 Received Data Interface

The outputs of the receiver are the two signals DATAOUT and DCLK. When the bit “RTParam_Bits” is “1”, the bit synchronizer is turned on, and the two output signals are respectively the output NRZ bit stream and the sampling clock. The value of DATAOUT is valid at the rising edge of DCLK (see Figure 11 on next page):

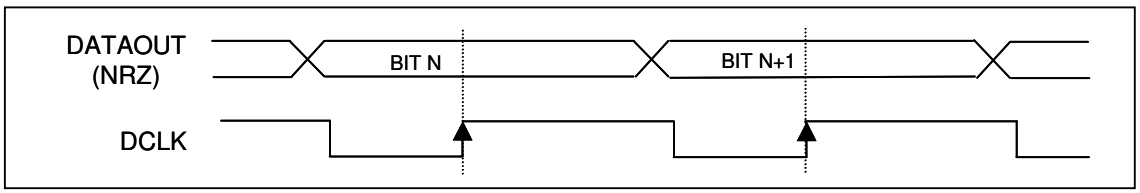

Figure 11: DATAOUT timing

When "RTParam_Bits" is "0", the bit synchronizer is turned off, and the signal DATAOUT is the output of the demodulator. In this case DCLK is not used and its value is set to "low". The maximum current drive on DATAOUT and DCLK is 2 mA @ 2.7 V, the maximum load is CLop.

5.6 Pattern Recognition Interface

When this feature is enabled, the incoming NRZ bit stream is compared with a pattern stored in the "Pattern" register. The PATTERN output (active-low) is driven by the output of this comparator and is synchronized by DCK. It is asserted when a match is detected, otherwise negated (please see Figure 12, below). Changes occur at the rising edge of DCK.

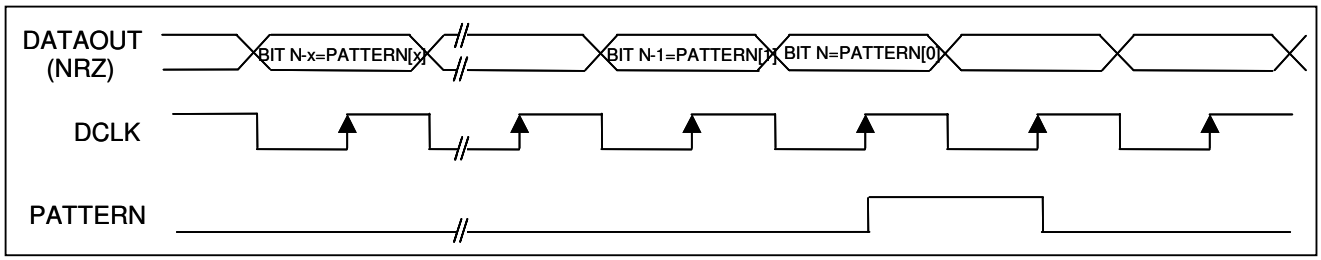

Figure 12: Pattern Recognition timing

When the feature is disabled, the PATTERN output is always negated. The maximum current drive on PATTERN is 2 mA @ 2.7 V, the maximum load is CLop.

5.7 Clock Output Interface

CLKOUT is a clock signal at 1.22, 2.44, 4.87, or 9.75 MHz, depending on user-programming. When the XE1202A TrueRF™ is in Sleep Mode (MODE[2:0] = 000) or when "RTParam_Clkout" is low, this clock is disabled.

5.8 Default settings at power-up

Upon power-up all RTParam, FSParam, ADParam and Pattern registers are set to 00H.

At power-up, the XE1202A TrueRF™ is in Standby mode, which means that the Xtal oscillator is enabled; additionally a clock signal at 1.22 MHz (reference frequency divided by 32) is present at CLKOUT. However, internally, RTParam_Clkout is low, which means that if the configuration register remains unaltered, the clock signal at CLKOUT will be disabled on the first rising edge of /EN; in addition, at the first rising edge of /EN, the circuit will be put in the mode corresponding to the status of the signals at MODE(2:0) inputs. Thus, to keep the circuit in Standby mode and the clock signal present on CLKOUT, RTParam_Clkout has to be set high during the first communication through the 3-wire bus, and the MODE(0) has to be set high before the first rising edge of /EN.