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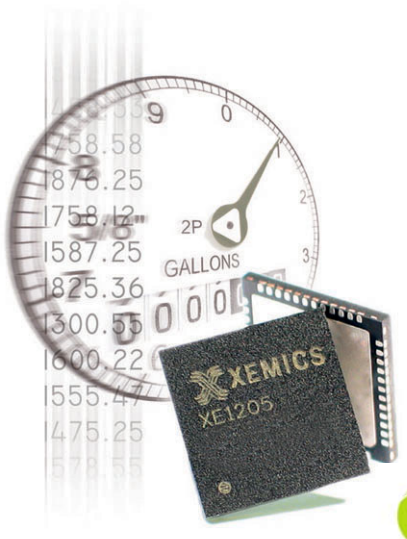

trueRF™

XE1205

180 MHz – 1GHz

Low-Power, High Link Budget Integrated UHF Transceiver

GENERAL DESCRIPTION

The XE1205 is an integrated transceiver operating in the 433, 868 and 915 MHz license-free ISM (Industrial, Scientific and Medical) frequency bands; it can also address other frequency bands in the 180-1000 MHz range. Its highly integrated architecture allows for minimum external components while maintaining design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The XE1205 offers the unique advantage of narrow-band and wide-band communication, this without the need to modify the number or parameters of the external components. The XE1205 is optimized for low power consumption while offering high RF output power and channelized operation suited for both the European (ETSI EN 300-220-1) and the North American (FCC part 15) regulatory standards. TrueRF™ technology enables a low-cost external component count (elimination of the SAW filter) whilst still satisfying ETSI and FCC regulations.

APPLICATIONS

- Narrow-band and wide-band security systems
- Voice and data over an RF link
- Process and building control
- Access control
- Home automation
- Home appliances interconnection

KEY PRODUCT FEATURES

- Programmable RF output power: up to +15 dBm
- High Rx sensitivity: down to -121 dBm at 1.2 kbit/s, -116 dBm at 4.8 kbits.
- Low power: RX=14 mA; TX = 62 mA @ 15 dBm
- Can accommodate 300-1000 MHz frequency range
- Wide band operation: up to 304.7 kbit/s, NRZ coding
- Narrow band operation: 25 kHz channels for data rates up to 4.8 kbit/s, NRZ coding; optional transmitter pre-filtering to enable adjacent channel power below -37 dBm at 25 kHz
- On-chip frequency synthesizer with minimum frequency resolution of 500 Hz
- Continuous phase 2-level FSK modulation
- Incoming data pattern recognition
- Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery
- FEI (Frequency Error Indicator) with built-in AFC
- RSSI (Received Signal Strength Indicator)
- 16-byte FIFO for transmit / receive data buffering and transfer via SPI bus

ORDERING INFORMATION

Part number	Temperature range	Package
XE1205I074TRLF[1]	-40 °C to +85 °C	VQFN48

(1) TR refers to tape & reel.
LF refers to Lead Free package.
This device is WEEE and RoHS compliant

TABLE OF CONTENTS

The XE1205 single-chip solution is an integrated circuit intended for use as a low cost FSK transceiver to establish a frequency-agile, half-duplex, bi-directional RF link, with non-return to zero data coding. The device is available in a VQFN 48 package and is designed to provide a fully functional multi-channel FSK transceiver. It is intended for applications in the 433 MHz and 868 MHz European bands and the North American 915 MHz ISM band. The single chip transceiver operates down to 2.4V. Its ability to operate with 25 kHz channel spacing makes it compliant with requirements of ETSI EN300 220-1 and makes the XE1205 ideal for automatic meter reading and alarms.

1 NON-CONFORMANCE

Please note early version lot codes whose date-codes start with N3K, N4K and N5K (except N5K3760, N5K3760A, N5K3760B and N5K6993) exhibit a non-conformance to specification. The non-conformance affects the FIFO buffer described in section 5.2.5. Please use the FIFO in this product only in conjunction with the Technical Note TN1205.01 (available www.semtech.com). All other date-codes are in conformance with the specification.

2 FUNCTIONAL BLOCK DIAGRAM

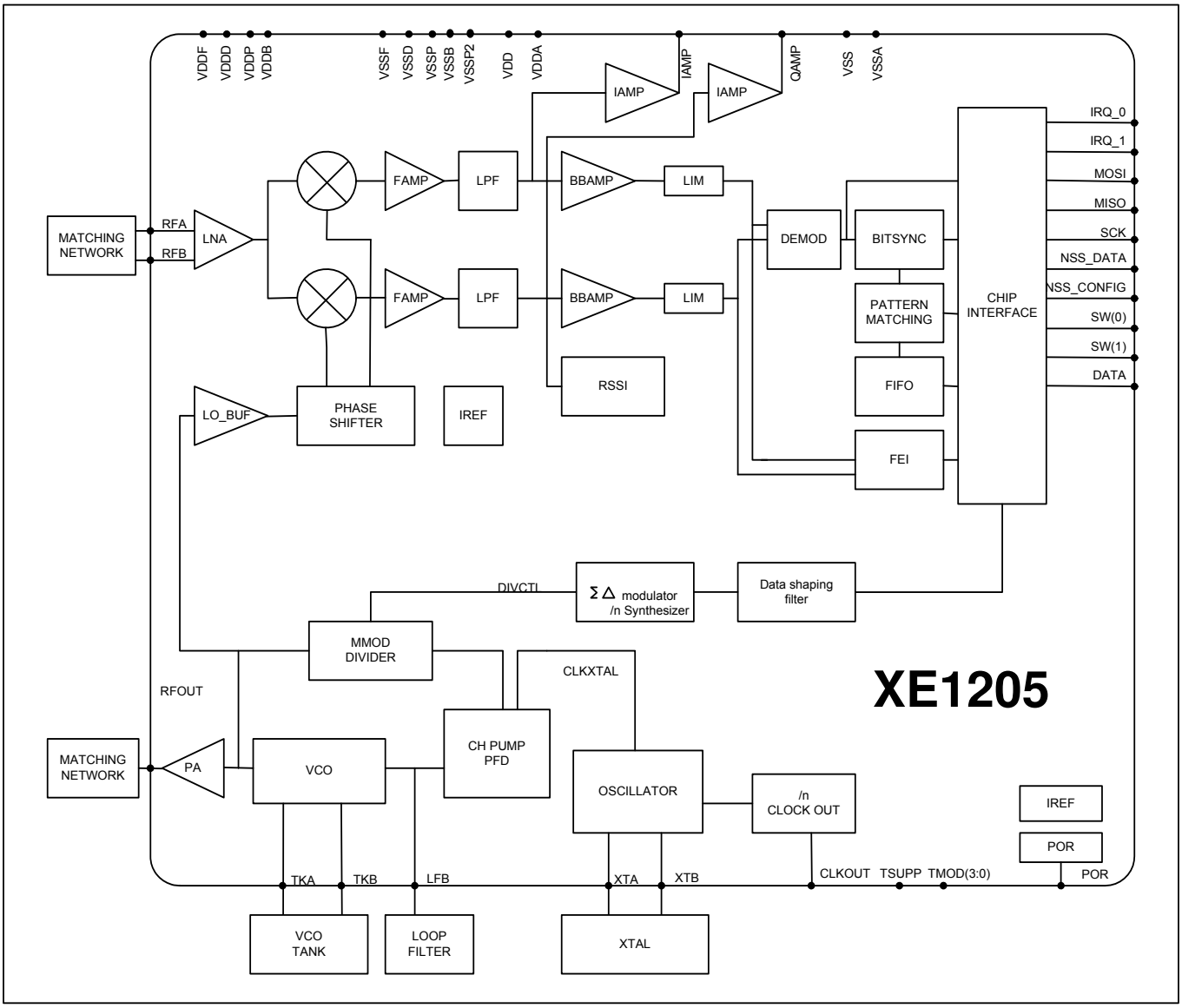

Figure 1: XE1205 block diagram.

3 PIN DESCRIPTION

PIN	NAME		DESCRIPTION
0	EPAD		Pad below package (should be grounded)
1	SW(0)	I/O	Transmit/Receive/Stand-by/Sleep Mode Select
2	SW(1)	I/O	Transmit/Receive/Stand-by/Sleep Mode Select
3	NC		Not connected (should be grounded)
4	NC		Not connected (should be grounded)
5	RFA	I	RF Input
6	RFB	I	RF Input
7	VSSP2		Power Amplifier Ground
8	VSSP2		Power Amplifier Ground
9	RFOUT	O	RF Output
10	VDDP		Power Amplifier Supply Voltage
11	VSSP		Power Amplifier Ground
12	VDDF		Second HF Analog Supply voltage
13	VSSF		Second HF Analog Ground
14	TKA	I/O	VCO Tank
15	VSSF		Second HF Analog Ground
16	TKB	I/O	VCO Tank
17	VSSF		Second HF Analog Ground
18	LFB	I/O	PLL Loop Filter
19	VDDD		HF Digital Supply Voltage
20	VSS		LF Digital Ground
21	NSS_CONFIG	I	SPI SELECT CONFIG
22	NSS_DATA	I	SPI SELECT DATA (DATA_IN in continuous mode)
23	VDD		LF Digital Supply Voltage
24	IRQ_0	O	Interrupt (refer to chapter 5.2.5 for mapping options)
25	IRQ_1	O	Interrupt(refer to chapter 5.2.5 for mapping options)
26	DATA	I/O	Data input and output (output only in continuous mode)
27	CLKOUT	O	Output clock at reference frequency divided by 2, 4, 8, 16, 32
28	MISO	O	SPI Master Input Slave Output
29	MOSI	I	SPI Master Output Slave Input
30	SCK	I	SPI CLOCK
31	XTA	I/O	Ref Xtal / Input of external clock
32	VSSA		LF analog ground
33	XTB	I/O	Reference Xtal
34	VDDA		LF Analog Supply Voltage
35	POR	I/O	Not used (should not be connected)
36	NC		Not connected (should be grounded)
37	TIBIAS	I/O	Test pin (should be grounded in normal operation)
38	TSUPP		Test pin (should be grounded in normal operation)
39	VDDA		LF Analog Supply Voltage
40	VSSA		LF analog ground
41	QAMP	O	Output of Q-Ch low-pass filter
42	IAMP	O	Output of -ChI low-pass filter
43	TMOD(3)	I/O	Test pin (should be grounded in normal operation)
44	TMOD(2)	I/O	Test pin (should be grounded in normal operation)
45	TMOD(1)	I/O	Test pin (should be grounded in normal operation)
46	TMOD(0)	I/O	Test pin (should be grounded in normal operation)
47	NC		Not connected (should be grounded)
48	NC		Not connected (should be grounded)

Table 1: Pin description

4 ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM OPERATING RANGES

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmax	Supply voltage	-0.5	3.9	V
Tmr	Storage temperature	-55	125	°C
ML	Receiver input level		5	dBm

Table 2: Absolute Maximum Operation Ranges

The device is ESD sensitive and should be handled with precaution.

4.2 SPECIFICATIONS

4.2.1 Operating Range

Symbol	Description	Min.	Max.	Unit
VDDop	Supply voltage	2.4	3.6	V
Trop	Temperature	-40	85	°C
Clop	Load capacitance on digital ports	-	25	pF

Table 3: Operating Range

4.2.2 Electrical Specifications

The table below gives the electrical specifications of the transceiver under the following conditions:
Supply Voltage = 3.3V, temperature = 25 °C, 2-level FSK without pre-filtering, fc = 915 MHz, Δf = 5 kHz,
Bit rate = 4.8 kbit/s, BW_{SSB} = 10 kHz, BER = 0.1% (at the output of the bit synchronizer), matched impedances, environment as defined in section 8, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.2	1	uA
IDDST	Supply current in standby mode	Quartz oscillator (39 MHz) enabled	-	0.85	1.10	mA
IDDR	Supply current in receiver mode		-	14	16.5	mA
IDDT	Supply current in transmitter mode	RFOP = 5 dBm RFOP = 15 dBm	- -	33 62	40 75	mA mA
RFS	RF sensitivity	Mode A Mode B	- -	-116 -102	-113 -99	dBm dBm
RFS_12	RF sensitivity at 1.2 kbit/s	Mode A Mode B	- -	-121 -107	-118 -104	dBm dBm
FDA	Frequency deviation	Programmable	1	-	255	kHz
CCR	Co-channel rejection		-13	-10	-	dBc
IIP3	Input intercept point (from LNA input to base-band filter output)	funw = f_{LO} + 1 MHz and f_{LO} + 1.995 MHz Mode A Mode B	 -37 -21	 -33 -18	 - -	 dBm dBm
BW	Base band filter bandwidth (SSB)	Programmable (1)	- - - -	10 20 40 200	- - - -	kHz kHz kHz kHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
ACR_25	Receiver adjacent channel rejection ratio at 25 kHz	funw = f_{LO} + 25 kHz single tone Pw=-110 dBm, mode A BW (SSB) = 10 kHz BW (SSB) = 8 kHz (2)	 - -	 20 30	 - -	 dBc dBc
ACR_50	Receiver adjacent channel rejection ratio at 50 kHz	funw = f_{LO} + 50 kHz single tone Pw=-110 dBm, mode A	-	40	-	dBc
BR	Bit rate	Programmable	1.2	-	304.7(4)	kbit/s
RFOP	RF output power	Programmable RFOP1 RFOP2 RFOP3 RFOP4	 -3 +2 +7 +12	 0 +5 +10 +15	 - - - -	 dBm dBm dBm dBm
ACP	Transmitter adjacent channel power (measured at 25 kHz offset)	Pre-filter enabled (RFOP3 mode) Measurement conditions as defined by EN 300 220-1 V1.3.1	-	-	-37	dBm
FR	Synthesizer frequency range	Programmable	433 863 902	- - -	435 870 928	MHz MHz MHz
TS_SRE	Receiver wake-up time	Quartz oscillator enabled	-	700	850	us
TS_STR	Transmitter wake-up time	Quartz oscillator enabled	-	250	350	us
TS_FS	Frequency synthesizer wake-up time	Quartz oscillator enabled	-	200	250	us
TS_RE	Receiver wake-up time	Frequency synthesizer enabled	-	500	600	us
TS_TR	Transmitter wake-up time	Frequency synthesizer enabled	-	100	150	us
TS_RFSW	Receiver recovery time when switching between 2 channels	Between 2 channels at 1 MHz from each other	-	700		us
TS_TFSW	Transmitter recovery time when switching between 2 channels	Between 2 channels at 1 MHz from each other	-	150	250	us
TS_RSSI	RSSI wake-up time	Receiver enabled	-	-	1.5	ms
TS_OS	Quartz oscillator wake-up time	Fundamental 3rd overtone	- -	1 7	2 -	ms ms
TS_FEI	FEI wake-up time	Receiver enabled	-	2/BR	-	ms
XTAL	Quartz oscillator frequency	Fundamental or third harmonic	-	39	-	MHz
FSTEP	Frequency synthesizer step	Exact step is XTAL / 77'824	-	500	-	Hz
VTHR	Equivalent input thresholds of the RSSI	Mode A(5), low range:VTHR1 VTHR2 VTHR3 Mode A, high range:VTHR1 VTHR2 VTHR3	- - - - - -	-110 -105 -100 -95 -90 -85	- - - - - -	dBm dBm dBm dBm dBm dBm
SPR	Spurious emission in receiver mode	(3)	-	-65	-	dBm
VIH	Digital input level high	% VDD	75	-	-	%
VIL	Digital input level low	% VDD	-	-	25	%
VOH	Digital output level high	% VDD	75	-	-	%
VOL	Digital output level low	% VDD	-	-	25	%

Table 4: Electrical Specifications

(1) Additional bandwidths can be selected with special settings described in section 7.2.8.
(2) With additional bandwidth configuration register settings as described in sections 5.2.6 and 7.2.8.
(3) SPR strongly depends on the design of the application board and the choice of the external components. Values down to -70 dBm can be achieved with careful design.
(4) 304.7 kbit/s achievable with additional register settings as described in section 6. The 304.7kpbs max bit rate is guaranteed by validation. The max bit rate guaranteed by production test is 152.3 kbit/s
(5) RSSI also available in mode B with higher thresholds as described in section 5.2.3.4

5 DESCRIPTION

The XE1205 is a direct conversion (Zero-IF) half-duplex data transceiver. It includes receiver, transmitter, frequency synthesizer and control logic. The circuit is intended primarily for operation in the following three ISM frequency bands 433 MHz, 868 MHz, and 915 MHz with a same 39MHz reference crystal and uses 2-level FSK modulation.

Operation of the XE1205 over the frequency range 180 MHz - 1000 MHz beyond the ISM bands described above can be achieved by modifying the reference oscillator crystal frequency. Please contact Semtech for more details.

The XE1205 is programmed by a microcontroller through the 3-wire fully-compatible SPI serial bus (MOSI, MISO, and SCK) to write to and read from the configuration registers.

The circuit consists of the following main functional blocks:

The receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream. The receiver comprises a low-noise amplifier, down-conversion mixers, baseband filters, baseband amplifiers, limiters, demodulator and bit synchronizer. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit stream DATAOUT and synchronized clock DCLK. This may be easily used to sample the DATAOUT signal with minimal external processor overhead. In addition, the receiver includes a Received Signal Strength Indicator (RSSI) function and a Frequency Error Indicator (FEI) function that provides an indication of the local oscillator frequency error. A pattern recognition function may be used to detect a user-programmable reference word in the incoming bit stream. The bandwidth of the base-band filters, the frequency deviation of the expected incoming FSK signal as well as the bit rate of the received data signal are all user-programmable. The receiver also embeds an automatic frequency offset cancellation to compensate local oscillator drifts due to XTAL.

The transmitter performs the modulation of the carrier by an input baseband data signal and the transmission of the modulated signal. The frequency synthesizer is modulated directly. The modulated signal is then amplified by the on-chip RF power amplifier. The output power is user-programmable to one of four possible values. The frequency deviation and the bit rate for the transmit signal are the same as those programmed for the receiver section. User-defined pre-filtering should be enabled to ensure compliance with the requirements of ETSI EN 300 220-1 regarding transmission at 25 kHz channel spacing.

The frequency synthesizer generates the local oscillator (LO) signal for the receiver section as well as the FSK modulated signal for the transmitter section. The core of the synthesizer is implemented with a PLL structure. The frequency is user-programmable with a frequency resolution of approximately 500 Hz in the 433 MHz, 868 MHz and 915 MHz ISM frequency bands. This section includes a crystal oscillator whose signal is the reference for the PLL. This reference frequency is divided by 2, 4, 8, 16, or 32 and is made available at the CLKOUT pin to serve as a clock signal for an external processor.

The control block generates the control signals according to the setting in its set of configuration registers.

The service block performs all the necessary functions for the circuit to work properly, including the internal voltage and current sources.

5.1 DATA OPERATION MODES

The XE1205 is user-programmable between two modes of operation:

Continuous mode: each bit transmitted or received is accessed directly at the DATA input/output pin.

Buffered mode: a 16-byte FIFO is used to store each data byte transmitted or received. This data is written to/read from the FIFO via the SPI bus. It reduces processor overhead.

5.2 RECEIVER SECTION

The XE1205 is set to receive mode when MCParam_Select_mode is low by setting MCParam_Chip_mode(1:0) to “01”. If MCParam_Select_mode is high the XE1205 is set to receive mode by setting SW(1:0) to “01”.

5.2.1 LNA & Receiver modes

The LNA of the receiver has two programmable operation modes: the high sensitivity mode, Mode A, for reception of weak signals; and the high linearity mode, Mode B, for strong signals. The operation mode is defined by the value of the Rmode bit in RXParam_Rmode configuration register.

Mode A: High sensitivity mode, RFS approximately 13dB better than in Mode B (see 4.2.2, RFS parameter)
Mode B: High Linearity mode, IIP3 approximately 15dB higher than in Mode A (see 4.2.2, IIP3 parameter)

5.2.2 Interrupt signal mapping

In receiver mode, two lines are dedicated to interrupt information. The interrupt pins are IRQ_0 and IRQ_1.
IRQ_0 has 3 selectable sources. IRQ_1 has 2 selectable sources. The two following tables summarize the interrupt management.

IRQParam_RX_irq_0	MCParam_Buffered_mode	IRQ_0	IRQ_0 Interrupt source
00	0	Output	Pattern
01	0	Output	RSSI_irq
10	0	Output	Pattern
11	0	Output	Pattern
00	1	Output	No interrupt available
01	1	Output	Write_byte
10	1	Output	/fifoempty
11	1	Output	Pattern

Table 5: IRQ_0 interrupt sources in receive mode.

IRQParam_RX_irq_1	MCParam_Buffered_mode	IRQ_1	IRQ_1 Interrupt source
00	0	Output	DCLK
01	0	Output	DCLK
10	0	Output	DCLK
11	0	Output	DCLK
00	1	Output	No interrupt available
01	1	Output	Fifofull
10	1	Output	RSSI_irq
11	1	Output	RSSI_irq

Table 6: IRQ_1 interrupt sources in receive mode.

5.2.3 Receiver in continuous mode

In this mode, the receiver has two output signals indicating recovered clock DCLK and recovered NRZ bit DATA. DCLK is connected to output pin IRQ_1 and DATA is connected to pin DATA configured in output mode. The bit synchronizer controls the recovered clock signal, DCLK. If the bit synchronizer is enabled by setting the bit /RXParam_Disable_bitsync to “0” (default value), the clock recovered from the incoming data stream appears at DCLK.

The function of the bit synchronizer is to remove glitches from the data stream and to provide a synchronous clock at DCLK. The output DATA is valid at the rising edge of DCLK. The following diagram shows the receiver chain operating in this mode

If the bit synchronizer is disabled, the DCLK output is held low and the raw demodulator output appears at DATA.
.

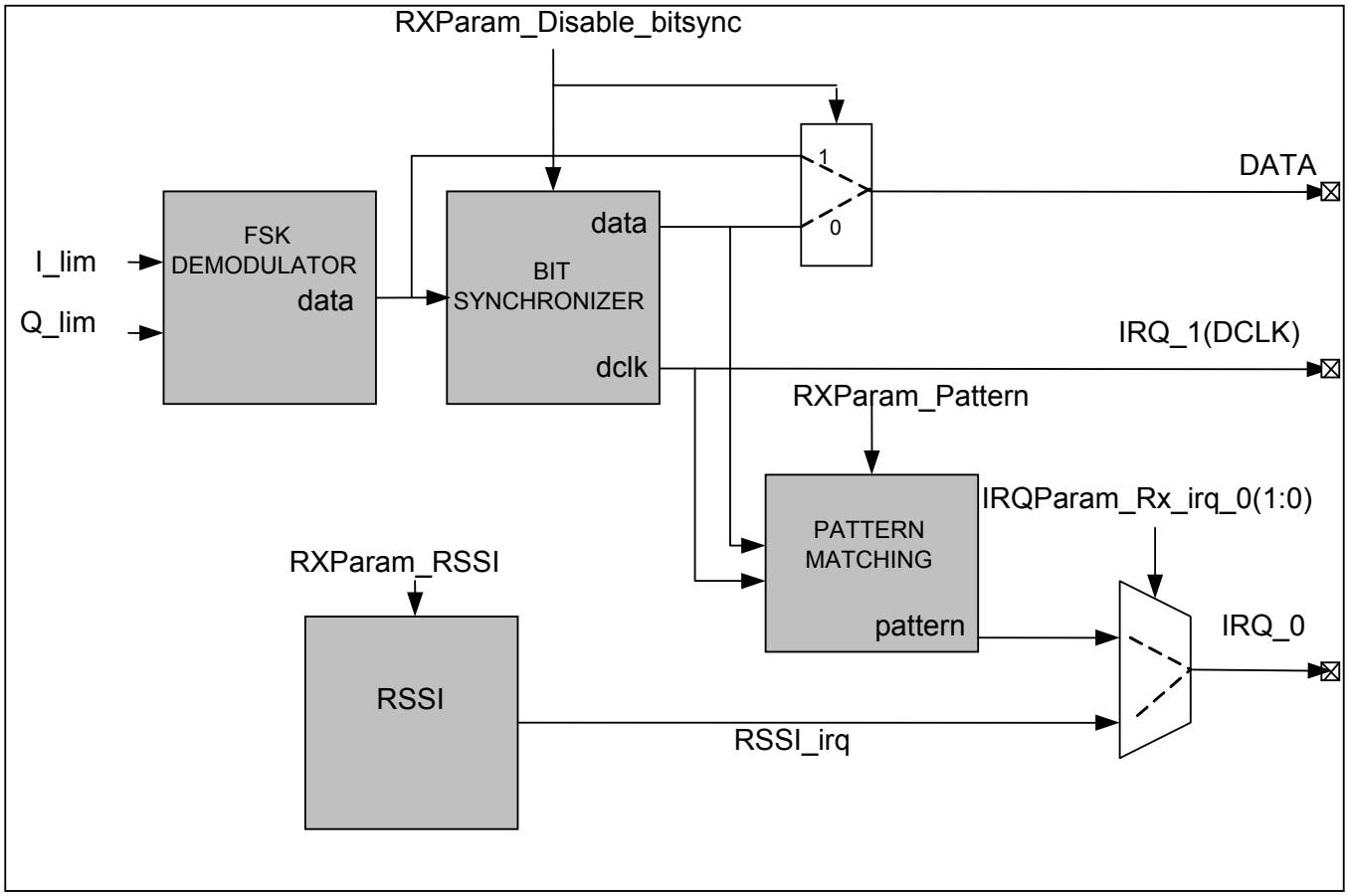

Figure 2: Receiver chain in continuous mode

5.2.3.1 Demodulator in continuous mode

The demodulator section comprises FSK demodulator, bit synchronizer, and Pattern Recognition blocks.

Data from the FSK baseband limited signals I_lim and Q_lim is first demodulated before passing to the bit synchronizer.

If the end-user application requires direct access to the output of the demodulator, then the RXParam_Disable_bitsync bit must be set high. In this case the demodulator output is directly connected to the DATA pin and the IRQ_1 pin (DCLK) is set to low.

For best operation of the demodulator it is recommended the modulation index β of the input signal meets the following condition:

$$\beta = \frac{2\Delta f}{BR} \geq 2$$

where Δf is the frequency deviation and BR the bit rate.

5.2.3.2 Bit synchronizer in continuous mode

The raw output signal from the demodulator may contain jitter and glitches. The bit synchronizer converts the data output of the demodulator into a glitch-free bit-stream DATA and generates a synchronized clock DCLK to be used for sampling the DATA output (see below). DCLK is available on pin IRQ_1 when the chip operates in continuous mode.

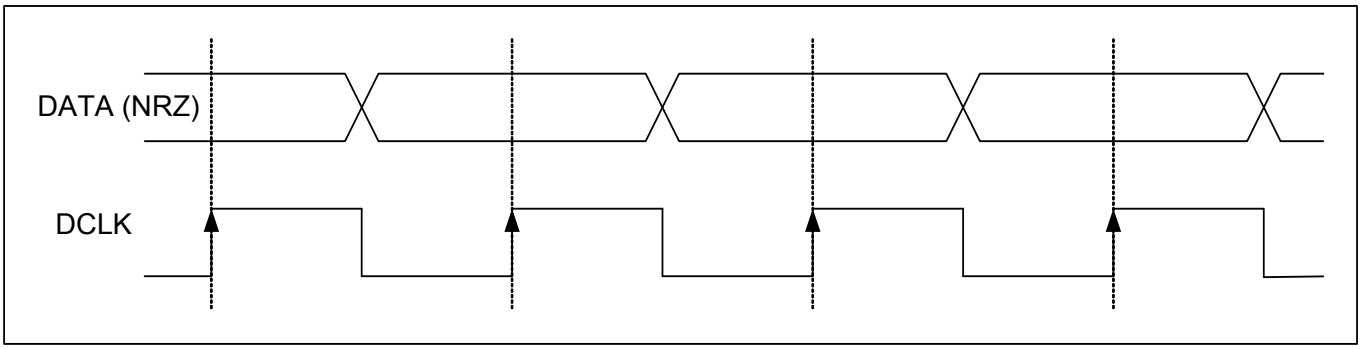

Figure 3: Bit synchronizer timing diagram

For proper operation, in addition to the requirement for the modulation index defined in Section 5.2.3.1, the Bit Synchronizer must first receive three bytes of alternating logic value preamble, i.e. “0101” sequences. After this startup phase, the rising edge of DCLK signal is centered on the demodulated bit. Subsequent data transitions will preserve this centering.

This has two implications:

- If the Bit Rates of Transmitter and Receiver are known to be the same, the XE1203F will be able to receive an infinite unbalanced sequence (all “0s” or all ”1s”) with no restriction.
- If there is a difference in Bit Rate between Tx and Rx, the amount of adjacent bits at the same level that the BitSync can withstand can be estimated as:

Number of bits = $0.5 \cdot \frac{BR}{\Delta BR}$

This implies approximately 6 consecutive unbalanced bytes when the Bit Rate precision is 1%, which is easily achievable (crystal tolerance is in the range of 50 to 100 ppm). It is recommended that the bit rate accuracy be better than ±5% (3% for Konnex mode operation).

The bit synchronizer is enabled by default. It is controlled by RXParam_Disable_bitsync. If the bit synchronizer is disabled the output of the demodulator is directed to DATA and the DCLK output (IRQ_1 Pin in continuous mode) is set to ‘0’.

The received bit rate is defined by the value of the MCParam_Br(6:0) configuration register, and is calculated as follows:

Bit rate = $\frac{152.34e3}{\text{int}(\text{Br}(6:0))+1}$ where int(x) is the integer value of the unsigned binary representation of x.

For the Konnex standard operation, the bit rate is fixed at 32.768 kbit/s. The bit synchronizer is automatically configured with the right bit rate value if the MCParam_Knx configuration bit is set high.

If needed, it is possible to select intermediate bit rates by changing the Over-Sampling Ratio (OSR) of the bit synchronizer, whose default value is 32. The latter can be superseded by setting high the register TParam_Chg_OSR. In this case, the bit rate becomes:

Bit rate = $\frac{152.34e3}{\text{int}(\text{Br}(6:0))+1} \cdot \frac{32}{\text{int}(OSR(7:0))+1}$,

where OSR(7:0) is the content of the register; TParam_OSR(7:0) as described in section 7.2.8.

For a correct operation of the bit synchronizer, the value of this register must be higher or equal to 15 and (int(OSR)+1) * Bit_rate should be inferior or equal to 4.87MHz.

5.2.3.3 Pattern recognition block in continuous mode

In receive mode this feature is activated by setting the RXParam_Pattern configuration register bit to high. The demodulated signal is compared with a pattern stored in the Reg_pattern(31:0) registers. The PATTERN signal (mapped to output pin IRQ_0) is driven by the output of this comparator and is synchronized by DCLK. It is set to high when a matching condition is detected, otherwise set to low. PATTERN output is updated at the rising edge of DCLK. The number of bits used for comparison is defined in the RXParam_Psize(1:0) register and the number of tolerated errors for the pattern recognition is defined in the RXParam_Ptol(1:0) register. Figure 4, illustrates the pattern matching process.

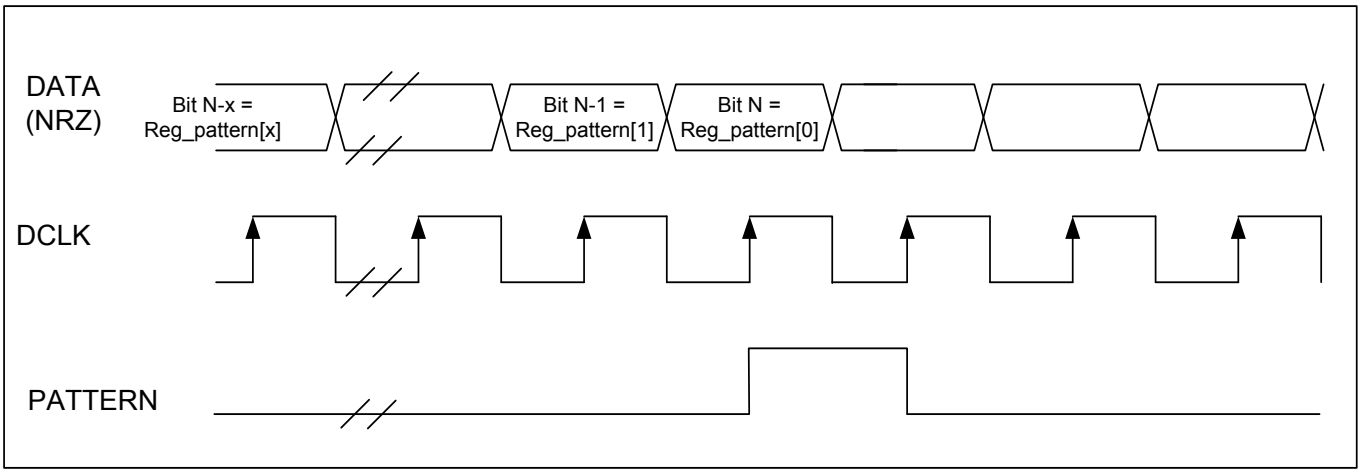

Figure 4: Pattern matching operation.

Note: The pattern recognizer is available only if the bit synchronizer is enabled.

5.2.3.4 RSSI in continuous mode

This function provides a Received Signal Strength Indication based on the signal level at the output of the base-band filter. To activate this function, the bit RXParam_RSSI must be set to "1". When activated, the 2-bit status information is stored in register RXParam_RSSI_OUT(1:0) and may be read through the serial control interface. The meaning of this status information is given in the table below, where V_{RFFIL} is the differential amplitude of the equivalent input RF signal when the receiver is operated in mode A. The thresholds VTHRi are at the output of the base-band filter divided by the gain between the input of the receiver and this output. When operated in mode B, equivalent VTHRi thresholds are shifted 15dBm higher.

RXPARAM_RSSI_out(1:0)	Description
0 0	$V_{RFFIL} \leq$ VTHR1
0 1	VTHR1 < $V_{RFFIL} \leq$ VTHR2
1 0	VTHR2 < $V_{RFFIL} \leq$ VTHR3
1 1	VTHR3 < V_{RFFIL}

Table 7: RSSI status description

The operating range of the RSSI measurement may be changed by programming the RXParam_RSSI_range bit; in this way two ranges with three VTHRi values may be selected. An additional way to increase RSSI operating range is to combine modes A and B thresholds. One could then cover input signals ranging from -110dBm (VTHR1, low range, mode A) up to -70dBm (VTHR3, high range, mode B)

The time diagram of an RSSI measurement is given in Figure 5. When the RSSI function has been activated the signal strength is periodically measured and the result is stored in RSSI_out_int; this result is transferred to the register RXParam_RSSI_out(1:0) each time this register is read via the SPI interface. TS_RSSI is the wake-up time required after the function has been activated to get a valid result and its value is given in section 4.2.2. TS_RSSIM is the period between two successive measurements and its value depends on the selected frequency deviation (100 μs for $\Delta f > 20$ kHz, 200 μs for 10 kHz < $\Delta f \leq 20$ kHz, 300 μs for 7 kHz < $\Delta f \leq 10$ kHz, 400 μs for 5 kHz < $\Delta f \leq 7$ kHz, and 500 μs $\Delta f \leq 5$ kHz).

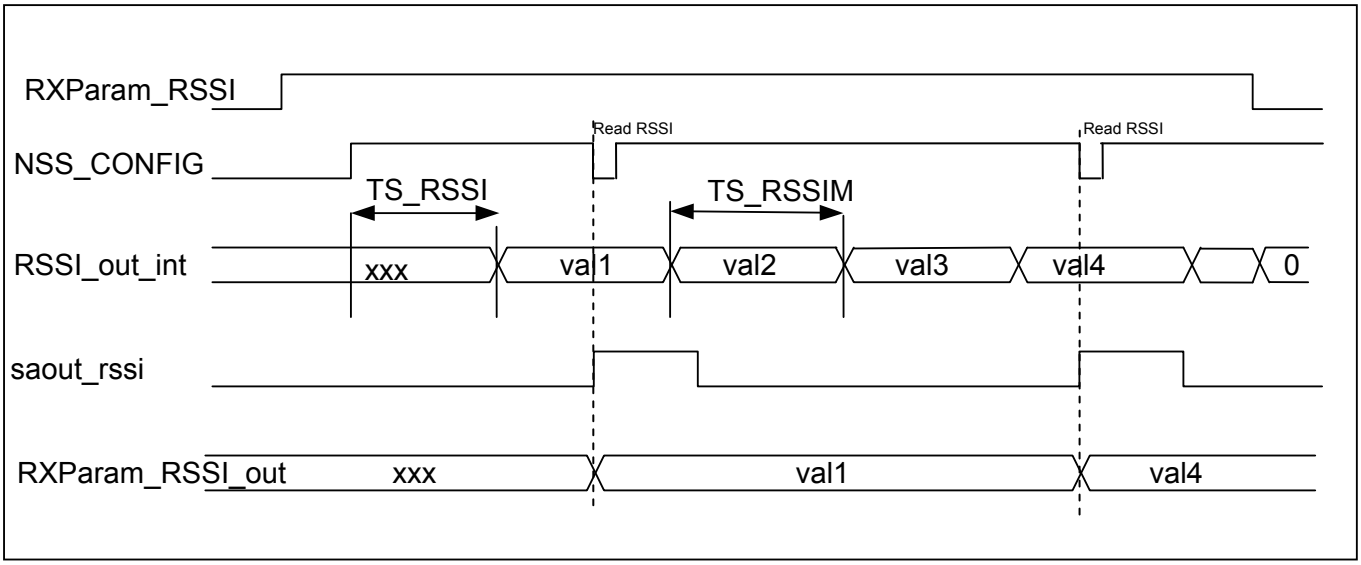

Figure 5: RSSI measurement timing diagram

Saout_rssi is internally generated during a read sequence of RXParam_RSSI_out register.

The RSSI block can also be used in interrupt mode by setting the bit IRQParam_RSSI_int to 1. When RSSI_out_int is equal or greater than a predefined value stored in IRQParam_RSSI_thr(1:0), the signal IRQParam_RSSI_signal_detect (can be read in the Configuration register) goes high and an interrupt signal RSSI_irq is generated. This interrupt signal can be used by a microcontroller if IRQParam_RX_irq_0 is set to "01" (see table 5).The interrupt is cleared by writing a 1 to the bit IRQParam_RSSI_signal_detect. If the bit IRQParam_RSSI_int remains high, the process starts again. The next figure shows the timing diagram of RSSI in interrupt mode.

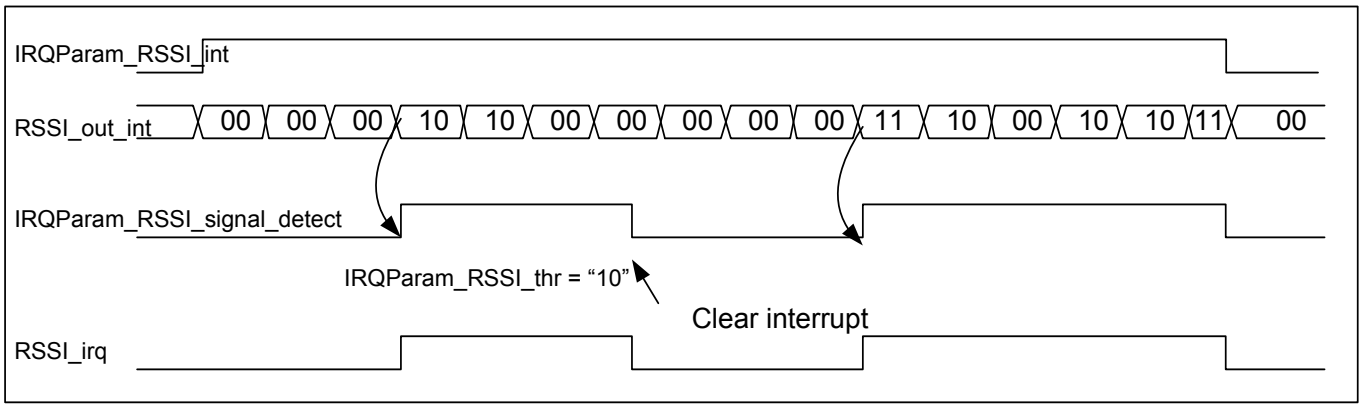

Figure 6: RSSI generating interrupt signal when detecting a threshold

5.2.3.5 Frequency Error Indicator in continuous mode – FEI

The block is switched ON by writing bit RXParam_FEI to '1'.This function provides information about the frequency error of the local oscillator compared with the input carrier frequency and can be used to implement an external AFC. The condition on the modulation index for proper behavior of the FEI function is:

$$\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$$

Where Δf is the frequency deviation and BR is the bit rate.

The time diagram of an FEI measurement is given in the next figure. When the FEI block has been woken up and is ready, and as long as the block is kept on, the frequency error is measured and the current result of the measurement is loaded in the register RXParam_FEI_out(15:0) each time registers 12 is read. TS_FEI is the time required for the first evaluation to be completed after the block has been started up and its value is given in section 4.2.2. Since the contents of the configuration register is validated at the rising edge of the enable signal NSS_CONFIG, the FEI block is actually started up at this time.

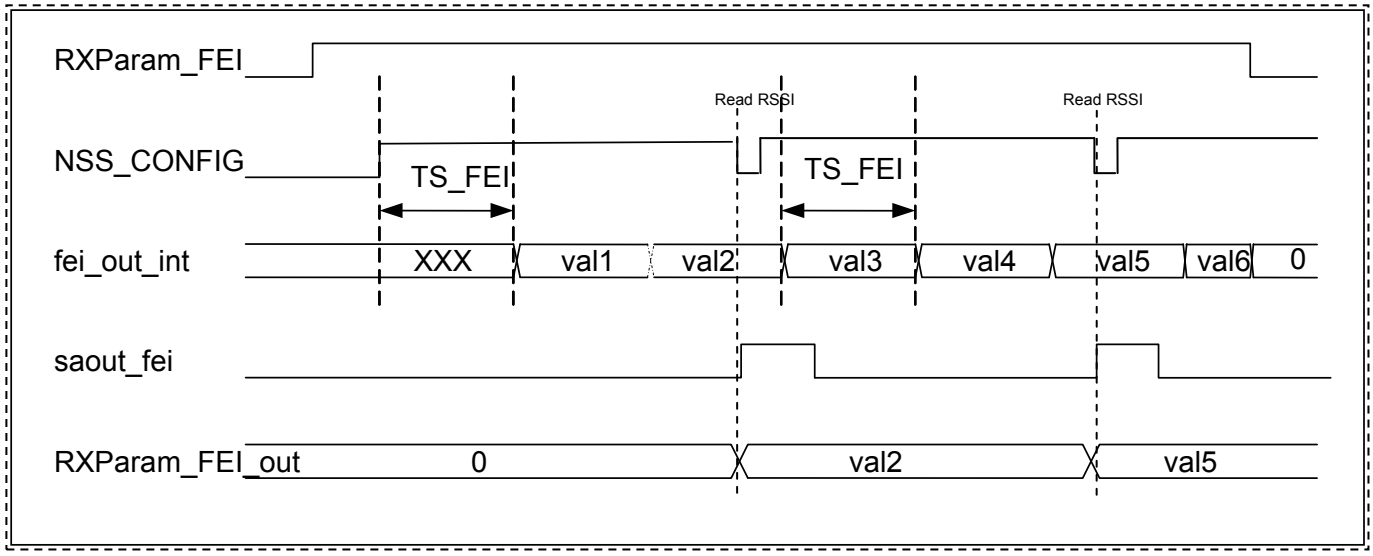

Figure 7: Timing diagram of an FEI measurement

To guarantee proper behavior of the FEI, the operation must be done when a preamble as defined in section 5.2.3.1 is received, and the sum of the frequency offset and the signal bandwidth (single sided) must be lower than the base band filter bandwidth (single sided). That is:

F_{offset} + SignalBW < FilterBW.

Where f_{offset} is the difference between the carrier frequency and the LO frequency, SignalBW is the signal bandwidth (single side) equal to the sum of the bit rate divided by 2 and the frequency deviation (BR/2 + DF), and FilterBW is the channel filter bandwidth defined by RXParam_BW(1:0) parameters.

The frequency error can be calculated by the following formula:

The frequency error = 500*int(FEI_out(15:0)) in Hz

Where int(x) is the integer value of the signed binary representation of x.

5.2.3.6 Frequency Error Correction

XE1205 offers two possibilities to correct the RF frequency error either by using FEI block with external microcontroller setting the corrected LO_Frequency or by using the internal Automatic Frequency error Cancellation (AFC).

When using FEI block, RXParam_FEI_out(15:0) can directly be subtracted to the register MCParam_Freq_lo(15:0) without further calculation by a microcontroller since the PLL step is 500 Hz i.e. RXParam_FEI_out (15:0) represents the number of step needed to compensate the frequency error .

Saout_fei is internally generated during a read sequence of register 12 in the same way as saout_rssi (refer to Figure 7).

To use AFC block, FEI block should be switched on by writing bit RXParam_FEI to '1' then AFC should be started by writing bit RX_Param:AFC_start to '1'. The LO_frequency error cancellation is effective providing bit RXParam_disable is written to '0' .Refer to previous chapter to guarantee proper behaviour of the FEI. RXParam_AFC_OK status register is automatically set to '0' when AFC is completed. RXParam_AFC_overflow will be automatically set to '1' in case the frequency error is too high to be automatically cancelled.

5.2.4 DATA pin in bidirectional or unidirectional mode (continuous mode only)

The DATA pin is bi-directional by default, and is used in both transmit and receive modes. In receive mode, DATA represents demodulated received data. In transmit mode baseband data is applied to this pin.

Some applications may require a separate input and output for transmitted and received data respectively. In this case the MCParam_Data_unidir configuration register bit must be set to '1'. The DATA pin is then set permanently to an output for received data, and NSS_DATA is used as the input.

5.2.5 Receiver in buffered mode

In this mode, the output of the bit synchronizer, i.e. the demodulated and resynchronized signal and the clock signal DCLK are not sent directly to the output pins DATA and IRQ_1 (DCLK). These signals are used to store the demodulated signal by packet of 8 bits in a 16 bytes FIFO. The following figure shows the receiver chain in this mode.

The FSK demodulator, bit synchronizer and pattern matching block work as described in section 5.2.2 but they are used with two additional blocks, FIFO and SPI.

When the chip is in receive mode and the MCParam_Buffered_mode bit is set to high then all the blocks described above are automatically enabled. In a normal communication frame the data stream comprises a 24 bit preamble, pattern (refer to section 5.2.3.3) and the data. Upon receipt of a recognized pattern, the receiver recognizes the start of a frame, strips off the preamble and pattern, then fills the FIFO with payload data to the microcontroller. This automated data recovery reduces the overhead for the host controller.

The IRQParam_Start_fill bit determines how the FIFO is filled:

If IRQParam_Start_fill is low, data only fills the FIFO subject to a correct pattern match. Data is shifted into the pattern recognition block which continuously compares the received data with the contents of the Reg_pattern(31:0) configuration register. If a match occurs a start sequence is detected, and the internal output of the pattern matching block is asserted for one bit length and the IRQParam_Start_detect bit is also asserted. This internal signal may be mapped to the IRQ_0 output using interrupt signal mapping (please refer to section 5.2.2). Once a pattern match has occurred, the pattern recognition block will remain inactive until IRQParam_Start_detect is re-asserted.

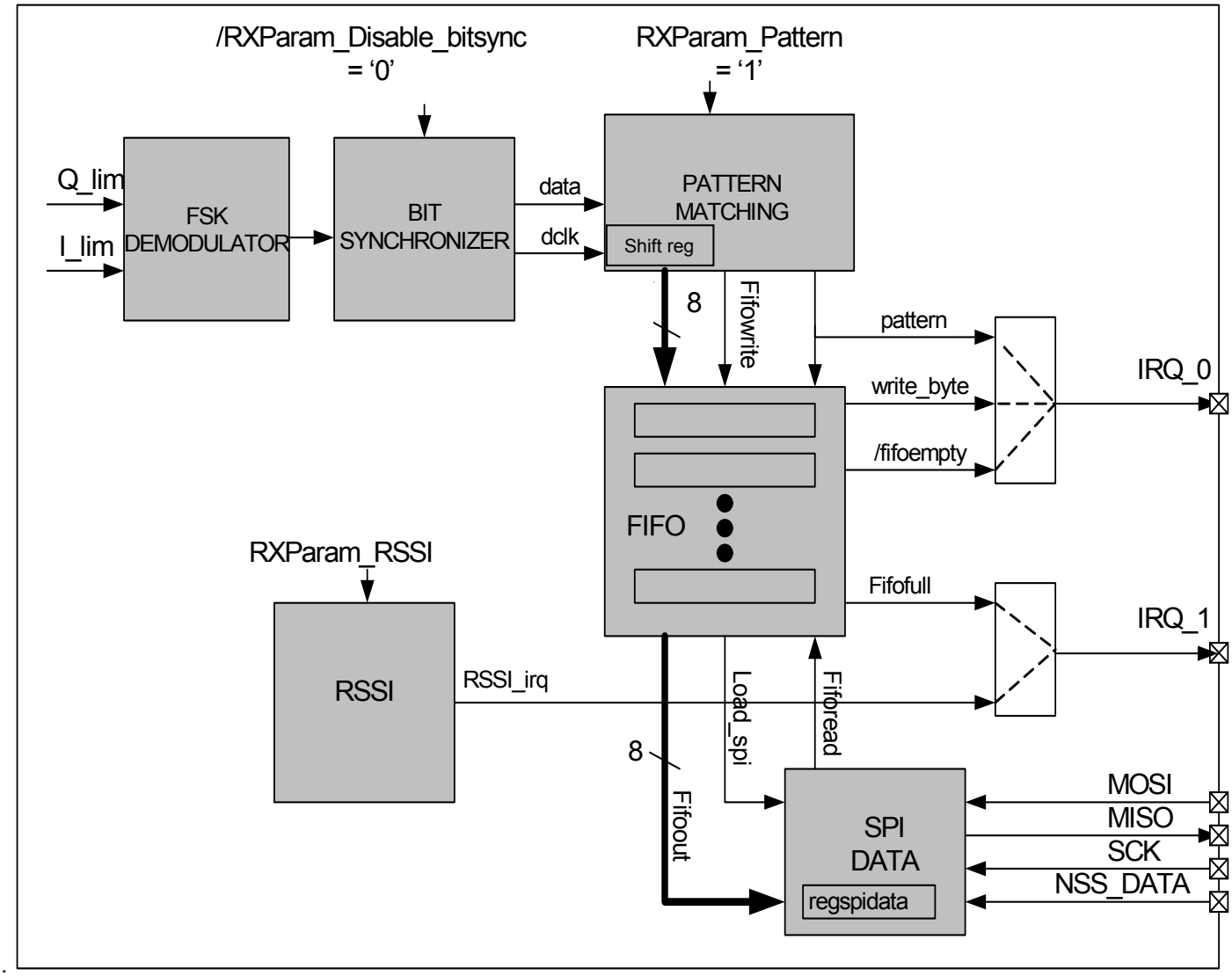

Figure 8: Receiver chain in buffered mode

If IRQParam_Start_fill is high, FIFO filling is initiated by asserting IRQParam_Start_detect.

Once sixteen bytes have been written to the FIFO the IRQParam_Fifofull signal is asserted. Data should then normally be read out. If no action is taken the FIFO will overflow and subsequent data will be lost. If this occurs the IRQParam_Fifooverrun bit is set. The IRQParam_Fifofull signal can be mapped to pin IRQ_1 as an interrupt for a microcontroller if IRQParam_RX_irq_1 is set to "01" (please refer to section 5.2.2).

To recover from an overflow situation a '1' must be written to IRQParam_Fifooverrun; this clears the contents of the FIFO, resets all FIFO status flags and re-initiates pattern matching (only when an overrun has occurred).

In order to clear the FIFO in reception, a "1" should be written in IRQParam_start_detect (bit 6 add 6).

Pattern matching can also be re-initiated during a FIFO filling sequence by writing a '1' to IRQParam_Start_detect.

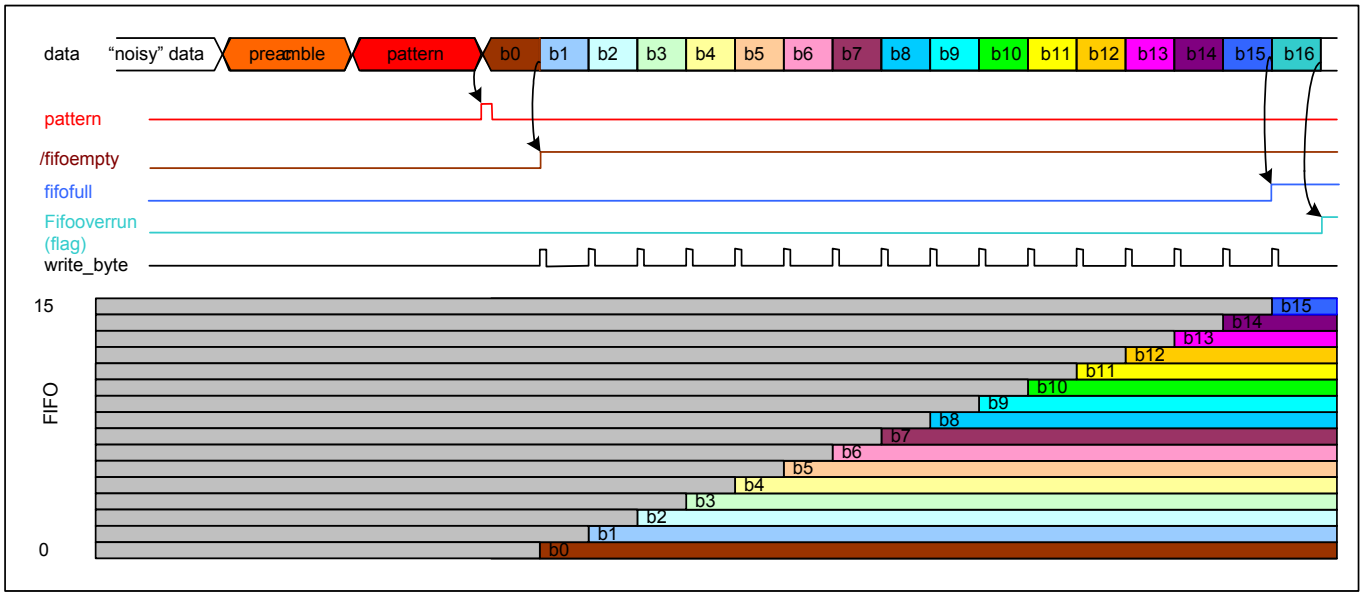

Figure 9: Start detection and FIFO filling

The FIFO filling process is shown in detail in Figure 9. As the first byte is written into the FIFO the signal /fifoempty goes high indicating that at least one byte is present. The microcontroller can then read the contents of the FIFO via the SPI interface. Once all data have been read from the FIFO then /fifoempty goes low. Once the last bit of the sixteenth byte has been written into the FIFO then the signal Fifofull is asserted; data should be read before the next byte is received.

This is illustrated in Figure 10.

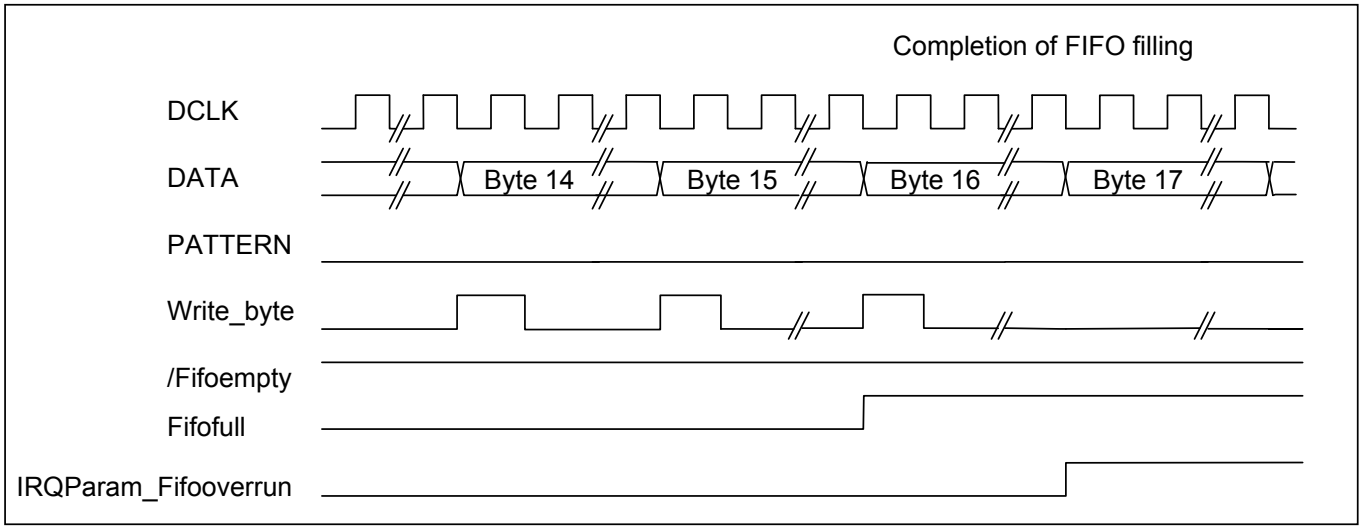

Figure 10: Completion of FIFO filling

The /fifoempty signal can be used as an interrupt signal for a microcontroller by mapping to pin IRQ_0 if IRQParam_RX_irq_0 is set to "10" (please refer to section 5.2.2). Alternatively, the WRITE_BYTE signal may also be used as an interrupt if IRQParam_RX_irq_0 is set to "01".

5.2.5.1 Demodulator in buffered mode

Demodulation in buffered mode occurs in the same way as in continuous mode (section 5.2.3.1). Received data is directly read from the FIFO and the DATA pin is not used.

5.2.5.2 Bit synchronizer in buffered mode

In buffered mode the bit synchronizer is automatically enabled (DCLK is not externally available).

5.2.5.3 Pattern recognition block in buffered mode

In buffered mode the pattern recognition block is automatically enabled. The PATTERN signal may be mapped to pin IRQ_0. Please refer to section 5.2.2 for further details.

5.2.5.4 RSSI in buffered mode

In buffered mode the Received Signal Strength Indication operates the same way as in continuous mode. In buffered mode, however, RSSI_irq may be mapped to IRQ_1 (please refer to section 5.2.2) instead of to IRQ_0 in continuous mode.

5.2.5.5 Frequency Error Indicator in buffered mode – FEI

In buffered mode the Frequency Error Indication operates the same way as in continuous mode. Please refer to section 5.2.3.5 for more details.

5.2.6 Additional narrowband filter bandwidths

The lowest bandwidth for the base-band filter which can be selected by changing only a 2-bit word in the configuration register is 10 kHz. However, as described in section 7.2.8, additional register settings allow this bandwidth to be further reduced. This option allows the user to improve the selectivity of the receiver for very narrow-band applications.

Activating this option is advised for bit rates and frequency deviations not higher than 4.8 kbit/s and 5 kHz and if the LO frequency of the receiver is well controlled, for instance by means of a very accurate crystal or the activation of an AFC.
The table below gives the sensitivity and the adjacent channel rejection for BR = 4.8 kbit/s and Δf = 5 kHz for different bandwidths.

Bandwidth SSB	TParam_Low _BW	TParam_Code_BW(8:0)	Sensitivity RFS (BER=0.1%)	Adjacent Channel Rejection ACR (25 kHz offset single tone)
10 kHz	0	X	-116 dBm	20 dBc
9 kHz	1	139	-116 dBm	25 dBc
8 kHz	1	160	-115.5 dBm	30 dBc
7 kHz	1	185	-115 dBm	35 dBc

Table 8: Performances of the receiver for very narrow bandwidths and 4.8 kbit/s

Table 9 below gives the sensitivity and the adjacent channel rejection for BR = 1.2 kbit/s and Δf = 2 kHz.

Bandwidth SSB	TParam_Low _BW	TParam_Code_BW(8:0)	Sensitivity RFS (BER=0.1%)	Adjacent Channel Rejection ACR (25 kHz offset single tone)
10 kHz	0	X	-117.5 dBm	18 dBc
9 kHz	1	139	-118 dBm	23 dBc
8 kHz	1	160	-119 dBm	28 dBc
7 kHz	1	185	-119.5 dBm	33 dBc

Table 9: Performances of the receiver for very narrow bandwidths and 1.2 kbit/s

It can be seen from table 9 that this option also allows the sensitivity to be improved for very low bit rates and frequency deviations.

5.3 TRANSMITTER SECTION

The XE1205 is set to transmit mode when MCParam_Select_mode is low by setting MCParam_Chip_mode(1:0) to “10”. If MCParam_Select_mode is high the XE1205 is set to transmit mode by setting pins SW(1:0) to “10”.

The data directly modulates the LO, or an (optional) pulse shaping filter can be used resulting in an adjacent channel power down to -37dBm at 25kHz for an output power up to 10dBm.

In continuous mode the transmitted data is sent directly to the frequency synthesizer.

In buffered mode the data is first written into the sixteen byte FIFO via the SPI interface; data from the FIFO is used to modulate the frequency synthesizer.

5.3.1 Output power

The output power of the power amplifier is programmable on four values with the register TXParam_Power (please refer to section 7.2.4 below), as shown in Table 10, where RFOP values are given in the Electrical Specifications section 4.2.2.

TXParam_POWER	Output power
0 0	RFOP1
0 1	RFOP2
1 0	RFOP3
1 1	RFOP4

Table 10: Output power settings

5.3.2 Transmitter in continuous mode

The transmitter works in continuous mode if the bit MCParam_Buffered_mode is low. The transmit data should be applied to pin DATA if register bit Data_unidir is low or pin NSS_DATA if register bit Data_unidir is high. Figure 11 shows the transmitter chain in continuous mode:

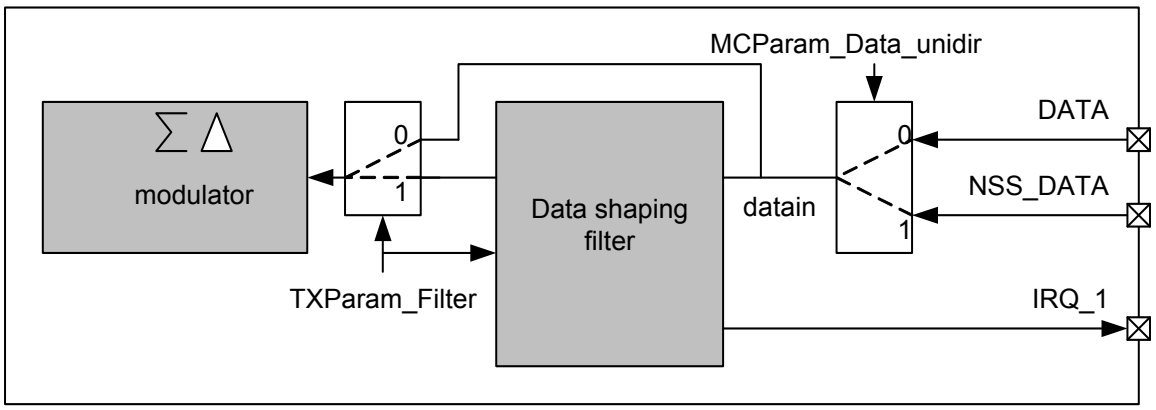

Figure 11: Transmitter data path in continuous mode

The pulse shaping function is enabled by setting TXParam_Filter to ‘1’. If the filtering option is selected, the DCLK signal is used as data clock in the transmission and this clock is generated at a frequency according to the selected bit rate. The DCLK signal is supplied to the microcontroller via the pin IRQ_1 which must update the data on the falling edge. The data is sampled at the rising edge of DCLK and filtered.

Figure 12 shows an example of filtered data for a bit rate of 4.8kbit/s and a frequency deviation of 5 kHz:

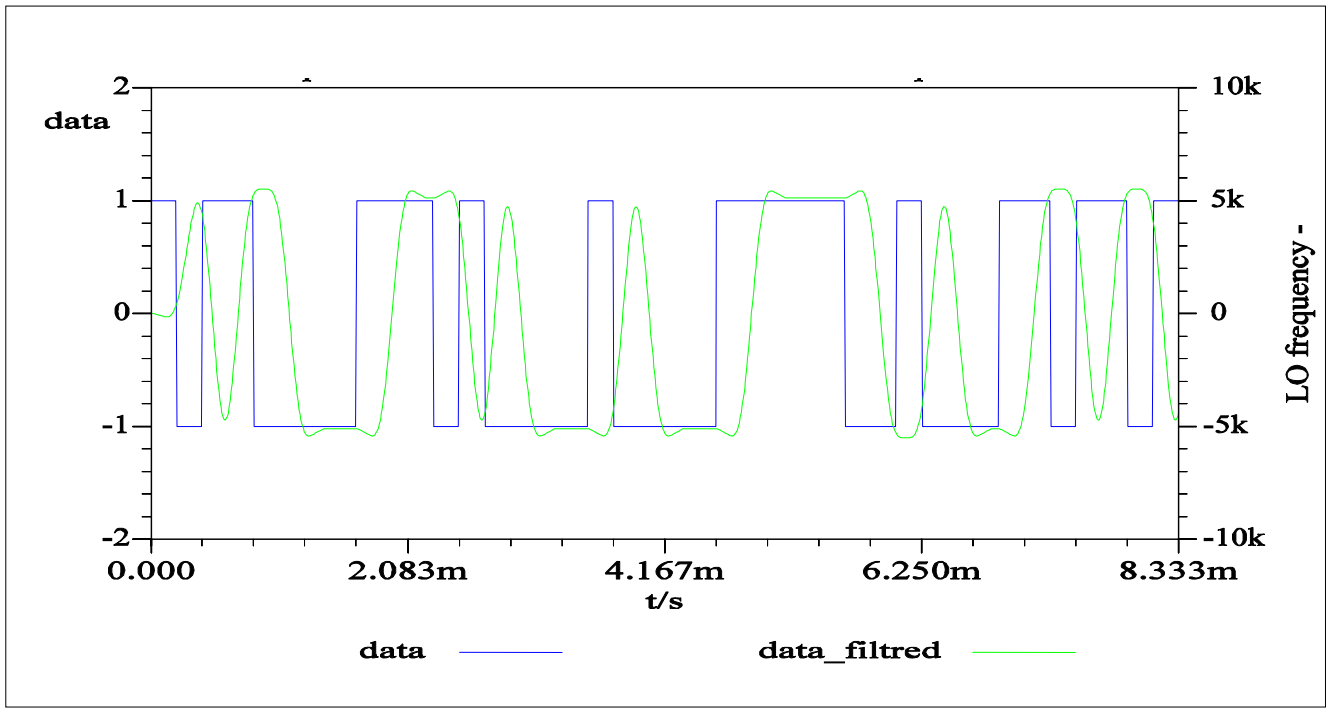

Figure 12: Pre-filtering of bit stream in transmit mode

The filtering option can be used for all bit rates specified in section 5.2.3.2 and for the following frequency deviations.

Freq_dev(8:0)	Frequency deviation (kHz)
000000101	2.5
000001010	5
000010100	10
000101000	20
001010000	40
010100000	80
101000000	160

Table 11: Available frequency deviations when using the filtering option

5.3.3 Transmitter in buffered mode.

The transmitter works in buffered mode if bit MCParam_Buffered_mode is high. Data to be transmitted is written to the 16-byte FIFO via the SPI interface. The data is loaded into a shift register which passes the data bit by bit to the data shaping filter or directly to the frequency synthesizer (as explained in the previous section). The transmitter chain is shown in Figure 13:

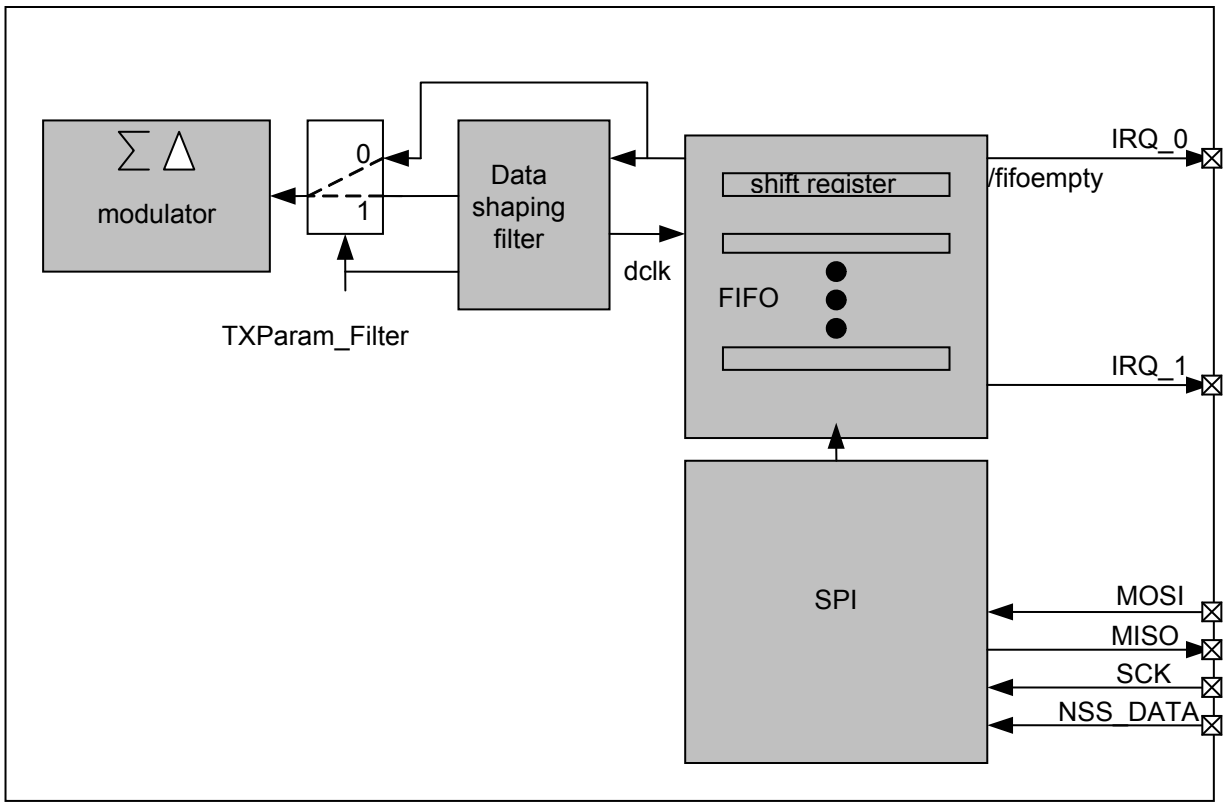

Figure 13: Transmit chain in buffered mode

FIFO operation in transmit mode is similar to receive mode; transmission either starts immediately after data is written into the FIFO or when the FIFO is full, determined by the IRQParam_Start_full bit setting.

If the transmit FIFO is full the interrupt signal fifofull is asserted on pin IRQ_1 (if configured accordingly). If data is written into the FIFO while it is full, the flag IRQParam_Fifooverrun will be set to '1' and the previous FIFO contents will be overwritten.

The IRQParam_Fifooverrun flag is cleared by writing a '1' to it. At the same time this clears the contents of the FIFO. Once the last data in the FIFO is loaded into the shift register, the flag /fifoempty is set to high on pin IRQ_0. If new data is not written in the FIFO and the last bit of the shift register has been transferred to the frequency synthesizer, the bit IRQParam_Tx_stopped goes high and the data seen by the frequency synthesizer is the last bit sent. If the transmitter is switched off (e.g. entry into another mode), the transmission will stop immediately even if there is still unsent data in the shift register.

In transmit mode the two interrupt signals are IRQ_0 and IRQ_1.

IRQ_1 is mapped to IRQParam_Fifofull signal indicating that the transmission FIFO is full when IRQParam_Tx_irq_1 is set to '0' and to TX_stopped when IRQParam_Tx_irq_1 is set to '1'.

IRQ_0 is mapped to the /fifoempty signal; this signal is used to indicate that the transmission FIFO is empty and must be refilled with data to continue data transmission.

5.4 FREQUENCY SYNTHESIZER

The Frequency Synthesizer generates the local oscillator (LO) signal for the receiver section as well as the continuous phase FSK (CPFSK) modulated signal for the transmitter section. The core of the synthesizer is implemented with a Sigma-Delta PLL architecture. The frequency is programmable with a step-size of 500 Hz in the 433, 868 and 915 MHz frequency bands. This block includes a crystal oscillator which provides the frequency reference for the PLL. This reference frequency can also be used as a reference clock for the external microcontroller on the CLKOUT pin.

5.4.1 Clock Output for an external processor

A reference clock can be generated for use by an external microcontroller. The OSCParam_Clkout configuration bit controls the CLKOUT pin. When set to high, CLKOUT is enabled, otherwise it is disabled. The output frequency at CLKOUT is defined by the value of the OSCParam_Clkout_freq(2:0) parameter. The output frequency at CLKOUT is the reference oscillator frequency divided by 2, 4, 8, 16 or 32. With a reference oscillator frequency of 39 MHz this provides a reference clock at 19.5 MHz, 9.75 MHz, 4.87 MHz, 2.44 MHz or 1.22 MHz, respectively.

This clock signal is disabled in Sleep Mode.

6 HIGHEST BIT RATES: EXAMPLE OF 304.7 KBIT/S OPERATION

XE1205 is able to sustain other bit rates between 152.34 kbit/s and 304.7 kbit/s using OSR_minus_1 register as described in section 5.2.3.2. It is recommended whenever possible to use a modulation index (β=2Δf/BR) ≥2 whenever possible. For the highest bit rates the receiver filter bandwidth will limit the maximal usuable β. Lower modulation indexes should be used then. In this chapter we provide the example of the highest bit rate.

In order to operate at 304.7 kbit/s the following settings should be used:

Please note that exact bitrate value is 304.6875 kbit/s.

6.1 REGISTERS SETTINGS

6.1.1 Bitrate (BR) and frequency deviation (fdev)

At 304.7 kbit/s, a modulation index close to 1 is compulsory because of the limited bandwidth of the Rx filter. Frequency deviation will be set to 160 kHz to also take benefit from the Tx filter available (Cf Table 11).
Consequently, following settings should be programmed:

Name	Address	Bits	Value (d)	Note
Freq_dev(8:0)	0	0	320	160.36 kHz
	1	7-0		
Br(6:0)	2	6-0	0	152.34 kbit/s…
Chg_OSR	27	4	1	
OSR (7:0)	28	7-0	15	…=>304.68 kbit/s

Table 12: common registers settings for 304.7 kbit/s

6.1.2 Rx filter

For a correct behavior we recommend to have an Rx filter bandwidth of minimum fdev + (BR/2).
Consequently, following settings should be programmed:

Name	Address	Bits	Value (d)	Note
BW(1:0)	8	6-5	3	200 kHz…
Max_BW	8	4	0	
TParam_Low_BW	19	2	1	
TParam_Code_BW(8:0)	21	6-0	87	…=>320 kHz
	22	7-6		

Table 13: Rx registers settings for 304.7 kbit/s

6.1.3 Tx filter

Tx filter is also available at 304.7 kbit/s operation and although not compulsory, its use is recommended to reduce spectrum bandwidth. Contrary to the other bitrates, an additional specific bit must be set.

Consequently, following settings should be programmed:

Name	Address	Bits	Value (d)	Note
Filter	7	4	1	
304 kbit/s_filter	18	3	1	

Table 14: Tx registers settings for 304.7 kbit/s

6.2 HARDWARE SETTINGS

When operating at 304.7 kbit/s, the loop filter must be modified. Typical recommended component values are provided below :

Name	434 MHz	869 MHz	915 MHz	Tolerance
CL1	3.3 nF	10 nF	10 nF	± 5%
CL2	220 pF	150 pF	150 pF	± 5%
RL1	1.5 kΩ	1.5 kΩ	1.5 kΩ	± 5%

Table 15: PLL Loop Filter Bill of Material for 304.7 kbit/s

6.3 OPERATION

Like for any other configuration, in order to avoid crystal misalignment issues and get the best performance it is recommended to perform an AFC with maximum Rx filter bandwidth before using the 304.7 kbit/s with the settings described above.

AFC operation may need to be performed at a lower datarate to cover worst case crystal, process and temperature variations.

Please note that all features including FIFO are available at bit rates up to 304.7 kbit/s.

6.4 TYPICAL PERFORMANCE

- Sensitivity@0.1%: -102 dBm in mode A and -90 dBm in mode B.
- ACR@1MHz offset, single tone: 25 dBc.

7 SERIAL INTERFACE DEFINITION AND PRINCIPLE OF OPERATION

7.1 SERIAL CONTROL INTERFACE

The XE1205 contains two SPI-compatible serial interfaces, one to send and read the chip configuration, the other to send and receive data in buffered mode. Both interfaces are configured in slave mode and share the same pins MISO (Master In Slave Out), MOSI (Master Out Slave In), SCK (Serial Clock). Two additional pins are required to select the SPI interface: NSS_CONFIG to change or read the transceiver configuration, and NSS_DATA to send or read data.

Figure 14 shows the connections between the transceiver and a microcontroller when buffered mode is used. IRQ_0 and IRQ_1 are not mentioned in the drawing but can be used.

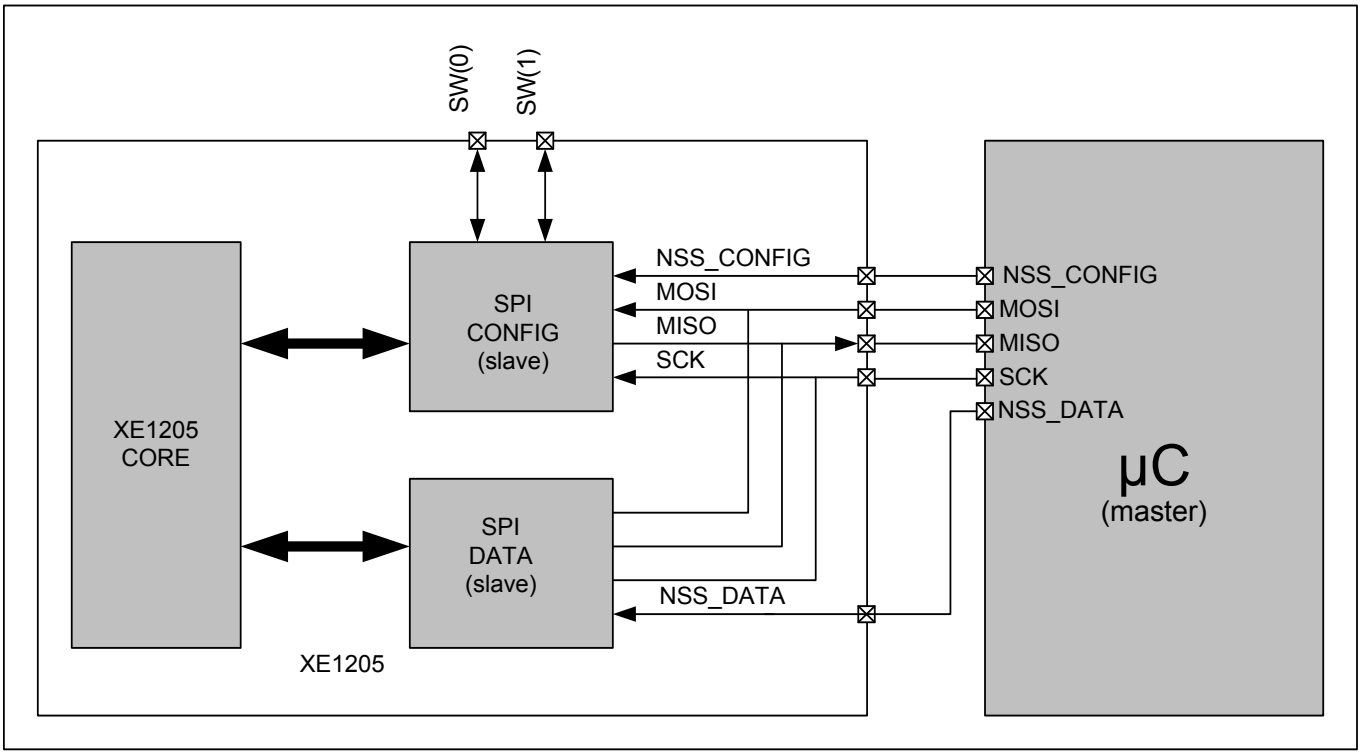

Figure 14: Connection between SPI DATA, SPI CONFIG and a micro-controller

It is possible to change between the four modes (sleep, stand-by, receive, transmit) by using the two-bit signal SW(1:0). This option is enabled by setting the bit MCParam_Select_mode to '1' in the configuration register.

A byte transmission can be seen as a rotate operation between the value stored in an 8 bit shift register of the master device (the microcontroller for instance) and the value stored in an 8 bit shift register of the selected slave device (the transceiver). The SCK line is used to synchronize both SPI interfaces. Data is transferred full-duplex from master to slave through the MOSI line and from slave to master through the MISO line. The most significant bit is always sent first. In both SPI interfaces the rising SCK edge is used to sample the received bit, and the falling SCK edge shifts the data inside the shift register. Max SCK frequency is 2MHz.

The NSS_CONFIG or NSS_DATA signal is controlled by the master device and should remain low during the byte transmission. It is not necessary to toggle the NSS_CONFIG signal back to high and back to low between each transmitted byte. However It is necessary to toggle the NSS_DATA signal back to high and back to low between each transmitted byte. The transmission is synchronized by the NSS_CONFIG or NSS_DATA signal. While the NSS_CONFIG or NSS_DATA is high, the counters controlling transmission are reset. Reception starts with the first clock cycle after the falling edge of NSS_CONFIG or NSS_DATA; if either signal goes high during a byte transmission the counters are reset and the byte has to be retransmitted.

7.1.1 Chip configuration via SPI_CONFIG interface

The SPI_CONFIG interface is selected if NSS_CONFIG is low even if the circuit is in buffered mode and NSS_DATA is low (SPI_CONFIG has priority). To configure the transceiver two bytes are required; the first byte contains a start bit (equal to 0), R/W information ('1' for a read operation or '0' for a write operation), 5 bits for the address of the register and finally a stop bit (equal to '1'). The second byte contains the data to be sent in write mode or the new address to read from in read mode. Figure 15 shows the timing diagram for a typical write sequence:

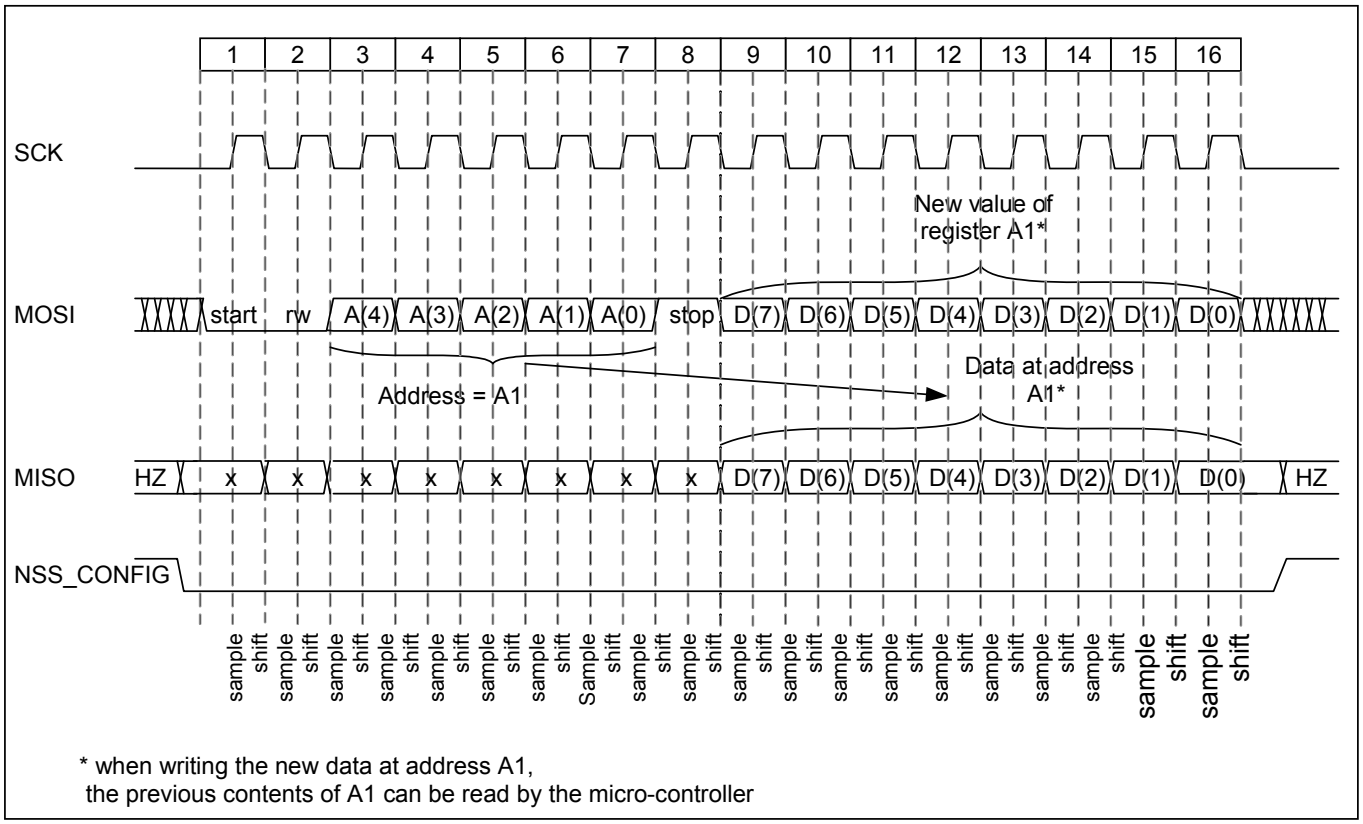

Figure 15: Write sequence when sending a new configuration to the XE1205 via the SPI _CONFIG

NSS_CONFIG must remain low during the transmission of the two bytes (address and data); if it goes high after the first byte, then the next byte will be considered as an address byte. When writing more than one register successively, NSS_CONFIG does not need to make a high to low transmission between two write sequences. The bytes are alternatively considered as an address byte followed by a data byte.

The read sequence via the SPI_CONFIG interface is similar to the write one except that the data byte contains all zeroes