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XE164

16-Bit Single-Chip
Real Time Signal Controller

16bit

Microcontrollers



Never stop thinking

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XE164

16-Bit Single-Chip

Real Time Signal Controller

Microcontrollers



Never stop thinking

XE164

Revision History: V2.1, 2008-08

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V2.0, 2008-03, Preliminary

V0.1, 2007-09, Preliminary

Page	Subjects (major changes since last revision)
several	Maximum frequency changed to 80 MHz
8	Specification of 6 ADC0 channels corrected
14f	Missing ADC0 channels added
28	Voltage domain for XTAL1/XTAL2 corrected to M
68	Coupling factors corrected
73, 75	Improved leakage parameters
74, 76	Pin leakage formula corrected
81	Improved ADC error values
94f	Improved definition of external clock parameters
107	JTAG clock speed corrected

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**16-Bit Single-Chip
Real Time Signal Controller
XE166 Family****1 Summary of Features**

For a quick overview and easy reference, the features of the XE164 are summarized here.

- High-performance CPU with five-stage pipeline
 - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
 - One-cycle 32-bit addition and subtraction with 40-bit result
 - One-cycle multiplication (16 × 16 bit)
 - Background division (32 / 16 bit) in 21 cycles
 - One-cycle multiply-and-accumulate (MAC) instructions
 - Enhanced Boolean bit manipulation facilities
 - Zero-cycle jump execution
 - Additional instructions to support HLL and operating systems
 - Register-based design with multiple variable register banks
 - Fast context switching support with two additional local register banks
 - 16 Mbytes total linear address space for code and data
 - 1024 Bytes on-chip special function register area (C166 Family compatible)
- Interrupt system with 16 priority levels for up to 83 sources
 - Selectable external inputs for interrupt generation and wake-up
 - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- On-chip memory modules
 - 1 Kbyte on-chip stand-by RAM (SBRAM)
 - 2 Kbytes on-chip dual-port RAM (DPRAM)
 - Up to 16 Kbytes on-chip data SRAM (DSRAM)
 - Up to 64 Kbytes on-chip program/data SRAM (PSRAM)
 - Up to 768 Kbytes on-chip program memory (Flash memory)
- On-Chip Peripheral Modules
 - Two Synchronizable A/D Converters with up to 16 channels, 10-bit resolution, conversion time below 1 μ s, optional data preprocessing (data reduction, range check)
 - 16-channel general purpose capture/compare unit (CAPCOM2)
 - Up to three capture/compare units for flexible PWM signal generation (CCU6x)
 - Multi-functional general purpose timer unit with 5 timers

Summary of Features

- Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
- On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 4 CAN nodes and gateway functionality
- On-chip real time clock
- Up to 12 Mbytes external address space for code and data
 - Programmable external bus characteristics for different address ranges
 - Multiplexed or demultiplexed external address/data buses
 - Selectable address bus width
 - 16-bit or 8-bit data bus width
 - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 75 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For ordering codes for the XE164 please contact your sales representative or local distributor.

This document describes several derivatives of the XE164 group. **Table 1** lists these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity the term **XE164** is used for all derivatives throughout this document.

Summary of Features

Table 1 XE164 Derivative Synopsis

Derivative¹⁾	Temp. Range	Program Memory²⁾	PSRAM³⁾	CCU6 Mod.	ADC⁴⁾ Chan.	Interfaces⁴⁾
SAF-XE164F-96FxxL	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164F-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1, 2	11 + 5	4 CAN Nodes, 6 Serial Chan.
SAF-XE164G-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164G-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1	6 + 5	2 CAN Nodes, 4 Serial Chan.
SAF-XE164H-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164H-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1, 2	11 + 5	No CAN Node, 6 Serial Chan.
SAF-XE164K-96F66L	-40 °C to 85 °C	768 Kbytes Flash	64 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-48F66L	-40 °C to 85 °C	384 Kbytes Flash	16 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.
SAF-XE164K-24F66L	-40 °C to 85 °C	192 Kbytes Flash	10 Kbytes	0, 1	6 + 5	No CAN Node, 4 Serial Chan.

1) This Data Sheet is valid for devices starting with and including design step AC.

Summary of Features

- 2) Specific information about the on-chip Flash memory in [Table 2](#).
- 3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM (12 Kbytes for devices with 192 Kbytes of Flash).
- 4) Specific information about the available channels in [Table 3](#).
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Summary of Features

The XE164 types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

Table 2 Flash Memory Allocation

Total Flash Size	Flash Area A¹⁾	Flash Area B	Flash Area C
768 Kbytes	C0'0000 _H ... C0'EFFF _H	C1'0000 _H ... CB'FFFF _H	n.a.
576 Kbytes	C0'0000 _H ... C0'EFFF _H	C1'0000 _H ... C8'FFFF _H	n.a.
384 Kbytes	C0'0000 _H ... C0'EFFF _H	C1'0000 _H ... C5'FFFF _H	n.a.
192 Kbytes	C0'0000 _H ... C0'EFFF _H	C1'0000 _H ... C1'FFFF _H	C4'0000 _H ... C4'FFFF _H

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XE164 types are offered with different interface options. **Table 3** lists the available channels for each option.

Table 3 Interface Channel Association

Total Number	Available Channels
11 ADC0 channels	CH0, CH2 ... CH5, CH8 ... CH11, CH13, CH15
6 ADC0 channels	CH0, CH2, CH3, CH4, CH5, CH8
5 ADC1 channels	CH0, CH2, CH4, CH5, CH6
4 CAN nodes	CAN0, CAN1, CAN2, CAN3
2 CAN nodes	CAN0, CAN1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1
4 serial channels	U0C0, U0C1, U1C0, U1C1

2 General Device Information

The XE164 series of real time signal controllers is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

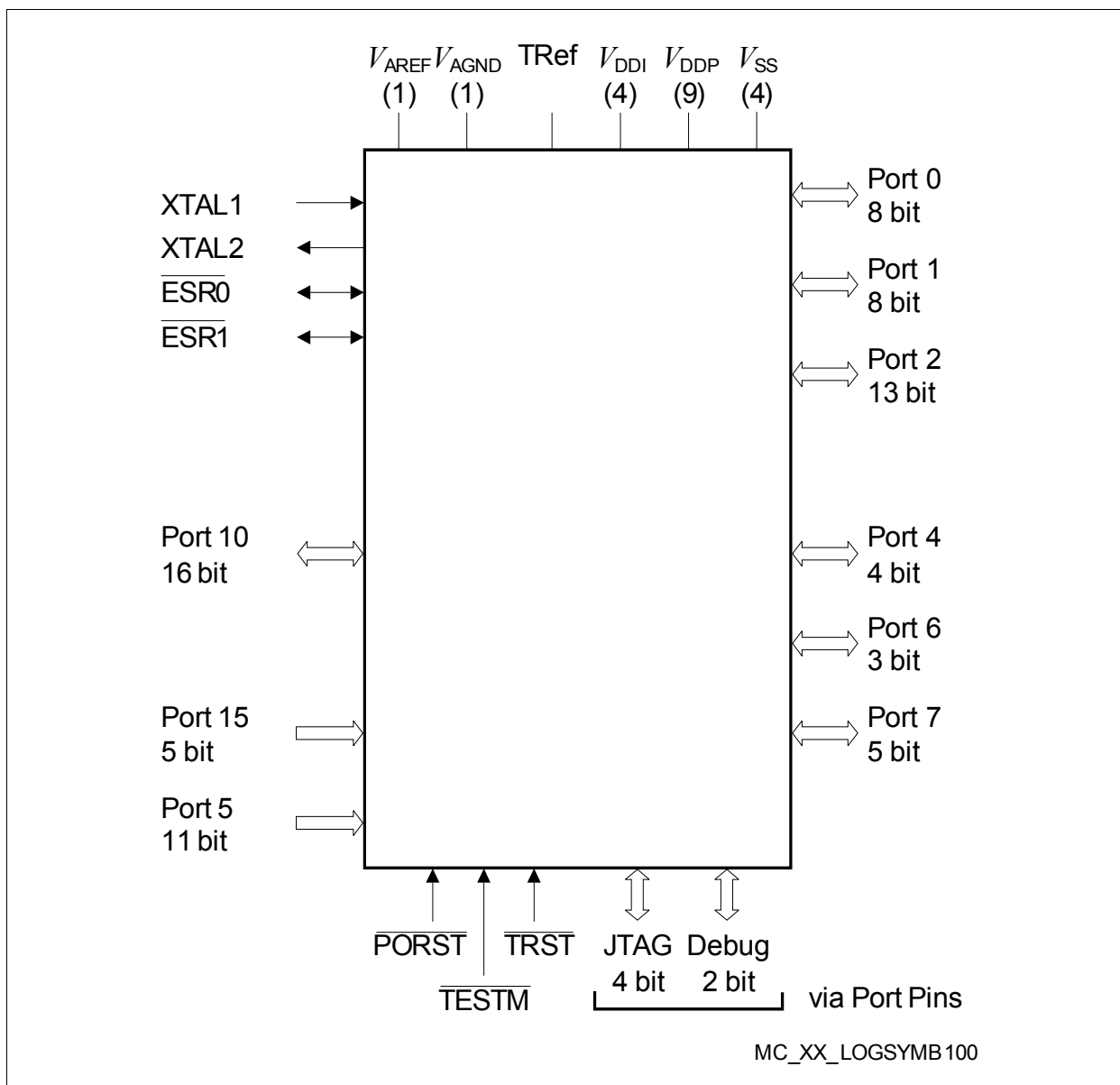


Figure 1 Logic Symbol

Notes to Pin Definitions

1. **Ctrl.:** The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bitfield PC to 1x00_B, output O1 is selected by 1x01_B, etc.
Output signal OH is controlled by hardware.
2. **Type:** Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	CCU62_ CCPOS0A	I	St/B	CCU62 Position Input 0
	TDI_C	I	St/B	JTAG Test Data Input
5	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE164's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT1 Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT2 Timer T6 Toggle Latch Output
	TDO_A	OH	St/B	JTAG Test Data Output
	ESR2_1	I	St/B	ESR2 Trigger Input 1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_ CCPOS1A	I	St/B	CCU62 Position Input 1
	TMS_C	I	St/B	JTAG Test Mode Selection Input
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	CCU62_ CTRAPA	I	St/B	CCU62 Emergency Trap Input
	$\overline{\text{BRKIN_C}}$	I	St/B	OCDS Break Signal Input
9	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_ SCLKOUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	CCU62_ CCPOS2A	I	St/B	CCU62 Position Input 2
	TCK_C	I	St/B	JTAG Clock Input
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input
11	P6.0	O0 / I	St/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	St/A	External Analog MUX Control Output 0 (ADC0)
	$\overline{\text{BRKOUT}}$	O3	St/A	OCDS Break Signal Output
	ADCx_ REQGTyC	I	St/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	St/A	USIC1 Channel 1 Shift Data Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
12	P6.1	O0 / I	St/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	St/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	St/A	GPT1 Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	St/A	USIC1 Channel 1 Shift Data Output
	ADCx_REQTRyC	I	St/A	External Request Trigger Input for ADC0/1
13	P6.2	O0 / I	St/A	Bit 2 of Port 6, General Purpose Input/Output
	EMUX2	O1	St/A	External Analog MUX Control Output 2 (ADC0)
	T6OUT	O2	St/A	GPT2 Timer T6 Toggle Latch Output
	U1C1_SCLKOUT	O3	St/A	USIC1 Channel 1 Shift Clock Output
	U1C1_DX1C	I	St/A	USIC1 Channel 1 Shift Clock Input
15	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
16	P15.2	I	In/A	Bit 2 of Port 15, General Purpose Input
	ADC1_CH2	I	In/A	Analog Input Channel 2 for ADC1
	T5IN	I	In/A	GPT2 Timer T5 Count/Gate Input
17	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6IN	I	In/A	GPT2 Timer T6 Count/Gate Input
18	P15.5	I	In/A	Bit 5 of Port 15, General Purpose Input
	ADC1_CH5	I	In/A	Analog Input Channel 5 for ADC1
	T6EUD	I	In/A	GPT2 Timer T6 External Up/Down Control Input
19	P15.6	I	In/A	Bit 6 of Port 15, General Purpose Input
	ADC1_CH6	I	In/A	Analog Input Channel 6 for ADC1
20	V_{AREF}	-	PS/A	Reference Voltage for A/D Converters ADC0/1
21	V_{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
22	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
23	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input
24	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3IN	I	In/A	GPT1 Timer T3 Count/Gate Input
28	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	T3EUD	I	In/A	GPT1 Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
29	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12HRB	I	In/A	External Run Control Input for T12 of CCU60
30	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	CCU6x_T12HRC	I	In/A	External Run Control Input for T12 of CCU6x
	CCU6x_T13HRC	I	In/A	External Run Control Input for T13 of CCU6x
31	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input
32	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	BRKIN_A	I	In/A	OCDS Break Signal Input
33	P5.11	I	In/A	Bit 11 of Port 5, General Purpose Input
	ADC0_CH11	I	In/A	Analog Input Channel 11 for ADC0
34	P5.13	I	In/A	Bit 13 of Port 5, General Purpose Input
	ADC0_CH13	I	In/A	Analog Input Channel 13 for ADC0
	EX0BINB	I	In/A	External Interrupt Trigger Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
35	P5.15	I	In/A	Bit 15 of Port 5, General Purpose Input
	ADC0_CH15	I	In/A	Analog Input Channel 15 for ADC0
36	P2.12	O0 / I	St/B	Bit 12 of Port 2, General Purpose Input/Output
	U0C0_SELO4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_SELO3	O2	St/B	USIC0 Channel 1 Select/Control 3 Output
	READY	I	St/B	External Bus Interface READY Input
37	P2.11	O0 / I	St/B	Bit 11 of Port 2, General Purpose Input/Output
	U0C0_SELO2	O1	St/B	USIC0 Channel 0 Select/Control 2 Output
	U0C1_SELO2	O2	St/B	USIC0 Channel 1 Select/Control 2 Output
	$\overline{\text{BHE}}/\overline{\text{WRH}}$	OH	St/B	External Bus Interf. High-Byte Control Output Can operate either as Byte High Enable (BHE) or as Write strobe for High Byte ($\overline{\text{WRH}}$).
39	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output
	AD13	OH / I	St/B	External Bus Interface Address/Data Line 13
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input
40	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output
	TxDC0	O1	St/B	CAN Node 0 Transmit Data Output
	AD14	OH / I	St/B	External Bus Interface Address/Data Line 14
	ESR1_5	I	St/B	ESR1 Trigger Input 5
	EX0AINA	I	St/B	External Interrupt Trigger Input
41	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output
	TxDC1	O1	St/B	CAN Node 1 Transmit Data Output
	AD15	OH / I	St/B	External Bus Interface Address/Data Line 15
	ESR2_5	I	St/B	ESR2 Trigger Input 5
	EX1AINA	I	St/B	External Interrupt Trigger Input
42	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output
	CC2_24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.
	$\overline{\text{CS0}}$	OH	St/B	External Bus Interface Chip Select 0 Output

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CC2_16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	A16	OH	St/B	External Bus Interface Address Line 16
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input
44	P4.1	O0 / I	St/B	Bit 1 of Port 4, General Purpose Input/Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_25	O3 / I	St/B	CAPCOM2 CC25IO Capture Inp./ Compare Out.
	$\overline{CS1}$	OH	St/B	External Bus Interface Chip Select 1 Output
45	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.
	A17	OH	St/B	External Bus Interface Address Line 17
	ESR1_0	I	St/B	ESR1 Trigger Input 0
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input
RxDC1A	I	St/B	CAN Node 1 Receive Data Input	
46	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output
	U0C0_SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.
	A18	OH	St/B	External Bus Interface Address Line 18
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.
	$\overline{CS2}$	OH	St/B	External Bus Interface Chip Select 2 Output
	T2IN	I	St/B	GPT1 Timer T2 Count/Gate Input
48	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
49	P4.3	O0 / I	St/B	Bit 3 of Port 4, General Purpose Input/Output
	CC2_27	O3 / I	St/B	CAPCOM2 CC27IO Capture Inp./ Compare Out.
	$\overline{CS3}$	OH	St/B	External Bus Interface Chip Select 3 Output
	RxDC2A	I	St/B	CAN Node 2 Receive Data Input
	T2EUD	I	St/B	GPT1 Timer T2 External Up/Down Control Input
53	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC60	O3 / I	St/B	CCU61 Channel 0 Input/Output
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
54	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
55	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC61	O3 / I	St/B	CCU61 Channel 1 Input/Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input
56	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output 1)
	CC2_21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input
57	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input
	TCK_A	I	St/B	JTAG Clock Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
58	P0.2	O0 / I	St/B	Bit 2 of Port 0, General Purpose Input/Output
	U1C0_SCLKOUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC62	O3 / I	St/B	CCU61 Channel 2 Input/Output
	A2	OH	St/B	External Bus Interface Address Line 2
	U1C0_DX1B	I	St/B	USIC1 Channel 0 Shift Clock Input
59	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_CC60	O2 / I	St/B	CCU60 Channel 0 Input/Output
	AD0	OH / I	St/B	External Bus Interface Address/Data Line 0
	ESR1_2	I	St/B	ESR1 Trigger Input 2
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input
60	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU60_CC61	O2 / I	St/B	CCU60 Channel 1 Input/Output
	AD1	OH / I	St/B	External Bus Interface Address/Data Line 1
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
61	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output
	U1C0_SELO0	O1	St/B	USIC1 Channel 0 Select/Control 0 Output
	U1C1_SELO1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output
	CCU61_COUT60	O3	St/B	CCU61 Channel 0 Output
	A3	OH	St/B	External Bus Interface Address Line 3
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input
62	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC62	O2 / I	St/B	CCU60 Channel 2 Input/Output
	AD2	OH / I	St/B	External Bus Interface Address/Data Line 2
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
63	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COUT61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input
65	TRef	IO	Sp/1	Control Pin for Core Voltage Generation 2)

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
66	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_SELO3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output
	CC2_23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.
	A23	OH	St/B	External Bus Interface Address Line 23
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input
	CAPIN	I	St/B	GPT2 Register CAPREL Capture Input
67	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output
	CCU60_COUT60	O2	St/B	CCU60 Channel 0 Output
	AD3	OH / I	St/B	External Bus Interface Address/Data Line 3
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input
68	P0.5	O0 / I	St/B	Bit 5 of Port 0, General Purpose Input/Output
	U1C1_SCLKOUT	O1	St/B	USIC1 Channel 1 Shift Clock Output
	U1C0_SELO2	O2	St/B	USIC1 Channel 0 Select/Control 2 Output
	CCU61_COUT62	O3	St/B	CCU61 Channel 2 Output
	A5	OH	St/B	External Bus Interface Address Line 5
	U1C1_DX1A	I	St/B	USIC1 Channel 1 Shift Clock Input
	U1C0_DX1C	I	St/B	USIC1 Channel 0 Shift Clock Input
69	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COUT61	O2	St/B	CCU60 Channel 1 Output
	AD4	OH / I	St/B	External Bus Interface Address/Data Line 4
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
70	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLKOUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COUT62	O2	St/B	CCU60 Channel 2 Output
	AD5	OH / I	St/B	External Bus Interface Address/Data Line 5
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
71	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CCU61_COUT63	O3	St/B	CCU61 Channel 3 Output
	A6	OH	St/B	External Bus Interface Address Line 6
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTRAPA	I	St/B	CCU61 Emergency Trap Input
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input
72	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	U1C0_SELO0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	AD6	OH / I	St/B	External Bus Interface Address/Data Line 6
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTRAPA	I	St/B	CCU60 Emergency Trap Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
73	P10.7	O0 / I	St/B	Bit 7 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	AD7	OH / I	St/B	External Bus Interface Address/Data Line 7
	U0C1_DX0B	I	St/B	USIC0 Channel 1 Shift Data Input
	CCU60_CCPOS0A	I	St/B	CCU60 Position Input 0
74	P0.7	O0 / I	St/B	Bit 7 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	U1C0_SELO3	O2	St/B	USIC1 Channel 0 Select/Control 3 Output
	A7	OH	St/B	External Bus Interface Address Line 7
	U1C1_DX0B	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTRAPB	I	St/B	CCU61 Emergency Trap Input
78	P1.0	O0 / I	St/B	Bit 0 of Port 1, General Purpose Input/Output
	U1C0_MCLKOUT	O1	St/B	USIC1 Channel 0 Master Clock Output
	U1C0_SELO4	O2	St/B	USIC1 Channel 0 Select/Control 4 Output
	A8	OH	St/B	External Bus Interface Address Line 8
	ESR1_3	I	St/B	ESR1 Trigger Input 3
	EX0BINA	I	St/B	External Interrupt Trigger Input
	CCU62_CTRAPB	I	St/B	CCU62 Emergency Trap Input