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XE216-512-FB236 Datasheet

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Table of Contents

1 xCORE Multicore Microcontrollers

The xCORE200 Series is a comprehensive range of 32-bit multicore microcontrollers that brings the low latency and timing determinism of the xCORE architecture to mainstream embedded applications. Unlike conventional microcontrollers, xCORE multicore microcontrollers execute multiple real-time tasks simultaneously and communicate between tasks using a high speed network. Because xCORE multicore microcontrollers are completely deterministic, you can write software to implement functions that traditionally require dedicated hardware.

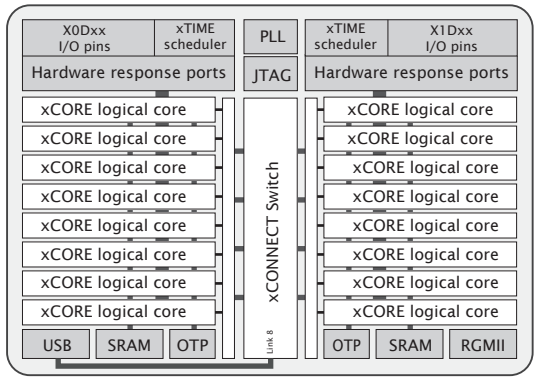

Figure 1: XE216-512-FB236 block diagram

Key features of the XE216-512-FB236 include:

- **Tiles**: Devices consist of one or more xCORE tiles. Each tile contains between five and eight 32-bit xCOREs with highly integrated I/O and on-chip memory.
- **Logical cores** Each logical core can execute tasks such as computational code, DSP code, control software (including logic decisions and executing a state machine) or software that handles I/O. Section 6.1
- **xTIME scheduler** The xTIME scheduler performs functions similar to an RTOS, in hardware. It services and synchronizes events in a core, so there is no requirement for interrupt handler routines. The xTIME scheduler triggers cores on events generated by hardware resources such as the I/O pins, communication channels and timers. Once triggered, a core runs independently and concurrently to other cores, until it pauses to wait for more events. Section 6.2
- **Channels and channel ends** Tasks running on logical cores communicate using channels formed between two channel ends. Data can be passed synchronously or asynchronously between the channel ends assigned to the communicating tasks. Section 6.5
- **xCONNECT Switch and Links** Between tiles, channel communications are implemented over a high performance network of xCONNECT Links and routed through a hardware xCONNECT Switch. Section 6.6

- **Ports** The I/O pins are connected to the processing cores by Hardware Response ports. The port logic can drive its pins high and low, or it can sample the value on its pins optionally waiting for a particular condition. Section 6.3
- **Clock blocks** xCORE devices include a set of programmable clock blocks that can be used to govern the rate at which ports execute. Section 6.4
- **Memory** Each xCORE Tile integrates a bank of SRAM for instructions and data, and a block of one-time programmable (OTP) memory that can be configured for system wide security features. Section 9
- **PLL** The PLL is used to create a high-speed processor clock given a low speed external oscillator. Section 7
- **USB** The USB PHY provides High-Speed and Full-Speed, device, host, and on-the-go functionality. Data is communicated through ports on the digital node. A library is provided to implement USB device functionality. Section 10
- **RGMII** The device has a set of pins that can be dedicated to communicate with an RGMII, including Gbit Ethernet PHYs, according to the RGMII v1.3 specification. Section 11
- **JTAG** The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory. Section 12

1.1 Software

Devices are programmed using C, C++ or xC (C with multicore extensions). XMOS provides tested and proven software libraries, which allow you to quickly add interface and processor functionality such as USB, Ethernet, PWM, graphics driver, and audio EQ to your applications.

1.2 xTIMEcomposer Studio

The xTIMEcomposer Studio development environment provides all the tools you need to write and debug your programs, profile your application, and write images into flash memory or OTP memory on the device. Because xCORE devices operate deterministically, they can be simulated like hardware within xTIMEcomposer: uniquely in the embedded world, xTIMEcomposer Studio therefore includes a static timing analyzer, cycle-accurate simulator, and high-speed in-circuit instrumentation.

xTIMEcomposer can be driven from either a graphical development environment, or the command line. The tools are supported on Windows, Linux and MacOS X and available at no cost from xmos.com/downloads. Information on using the tools is provided in the xTIMEcomposer User Guide, X3766.

2 XE216-512-FB236 Features

- **Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
  - 16 real-time logical cores on 2 xCORE tiles
  - Cores share up to 1000 MIPS
    - Up to 2000 MIPS in dual issue mode
  - Each logical core has:
    - Guaranteed throughput of between 1/5 and 1/8 of tile MIPS
    - 16x32bit dedicated registers
  - 167 high-density 16/32-bit instructions
    - All have single clock-cycle execution (except for divide)
    - 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions
- **USB PHY, fully compliant with USB 2.0 specification**
- **RGMII support, compliant with RGMII v1.3 specification**
- **Programmable I/O**
  - 128 general-purpose I/O pins, configurable as input or output
    - Up to 32 x 1bit port, 12 x 4bit port, 8 x 8bit port, 4 x 16bit port, 2 x 32bit port
    - 8 xCONNECT links
  - Port sampling rates of up to 60 MHz with respect to an external clock
  - 64 channel endss (32 per tile) for communication with other cores, on or off-chip
- **Memory**
  - 512KB internal single-cycle SRAM (max 256KB per tile) for code and data storage
  - 16KB internal OTP (max 8KB per tile) for application boot code
- **Hardware resources**
  - 12 clock blocks (6 per tile)
  - 20 timers (10 per tile)
  - 8 locks (4 per tile)
- **JTAG Module for On-Chip Debug**
- **Security Features**
  - Programming lock disables debug and prevents read-back of memory contents
  - AES bootloader ensures secrecy of IP held on external flash memory
- **Ambient Temperature Range**
  - Commercial qualification: 0°C to 70°C
  - Industrial qualification: -40°C to 85°C
- **Speed Grade**
  - 20: 1000 MIPS
- **Power Consumption**
  - 570 mA (typical)
- **236-pin FBGA package 0.5 mm pitch**

3 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	GND	VDDIOL	VDDIOL		TCK	CLK		4F X1D31 rx1	4F X1D29 rx_d0		8D X1D41 tx2	OTP_VCC		NC	MODE[0]		4F X0D29	VDDIOR	GND
B	1M X0D36	VDDIOL	VDDIOL	TDO	TMS	TRST_N	4E X1D33 rx3	4E X1D32 rx2	4F X1D28 rx_clk	4E X1D26 tx_clk	8D X1D42 tx1	OTP_VCC	NC	NC	MODE[1]	4E X0D33	4E X0D32	VDDIOR	VDDIOR
C	1N X0D37 $X_0L^4_3$	1O X0D38 $X_0L^5_3$	VDDIOL	TDI	DEBUG_N	RST_N	1C X1D10	1D X1D11	4F X1D30 rx0	4E X1D27 tx_d0	8D X1D43 tx0	8D X1D40 tx3	NC	NC	4F X0D31	4F X0D30	4F X0D28	4E X0D26 $X_0L^{10}_7$	4E X0D27 $X_0L^{11}_7$
D		1P X0D39 $X_0L^6_3$	8D X0D40 $X_0L^7_3$														1K X0D34 $X_0L^{12}_7$	1L X0D35 $X_0L^{13}_7$	
E	8D X0D43 $X_0L^{14}_7$	8D X0D42 $X_0L^{15}_7$	8D X0D41 $X_0L^{16}_7$														1J X0D25 $X_0L^{17}_7$	1I X0D24 $X_0L^{18}_7$	1G X1D01 $X_0L^{19}_7$
F	1K X1D34 $X_0L^{20}_7$	1L X1D35 $X_0L^{21}_7$	1M X1D36 $X_0L^{22}_7$				NC	VDD	VDD	VDDIOT	VDD	VDD	PLL_AVDD	PLL_AGND			4A X1D08 $X_0L^{23}_7$	4A X1D09 $X_0L^{24}_7$	1A X1D00 $X_0L^{25}_7$
G		32A X1D49 $X_0L^{26}_7$	32A X1D50 $X_0L^{27}_7$			VDD		GND		GND		GND		VDD			32A X0D69 $X_0L^{28}_7$	32A X0D70 $X_0L^{29}_7$	
H	32A X1D53 $X_0L^{30}_7$	32A X1D52 $X_0L^{31}_7$	32A X1D51 $X_0L^{32}_7$			VDD	GND	GND	GND	GND	GND	GND	GND	VDD			32A X0D68 $X_0L^{33}_7$	32A X0D67 $X_0L^{34}_7$	32A X0D66 $X_0L^{35}_7$
J	32A X1D54 $X_0L^{36}_7$	32A X1D55 $X_0L^{37}_7$	32A X1D56 $X_0L^{38}_7$			VDD		GND		GND		GND		VDD			32A X0D63 $X_0L^{39}_7$	32A X0D64 $X_0L^{40}_7$	32A X0D65 $X_0L^{41}_7$
K		32A X1D58 $X_0L^{42}_7$	32A X1D57 $X_0L^{43}_7$			VDD	GND	GND	GND	GND	GND	GND	GND	VDD			32A X0D62 $X_0L^{44}_7$	32A X0D61 $X_0L^{45}_7$	
L	32A X1D63 $X_0L^{46}_7$	32A X1D62 $X_0L^{47}_7$	32A X1D61 $X_0L^{48}_7$			VDD		GND		GND		GND		VDD			32A X0D58 $X_0L^{49}_7$	32A X0D57 $X_0L^{50}_7$	32A X0D56 $X_0L^{51}_7$
M	32A X1D64 $X_0L^{52}_7$	32A X1D65 $X_0L^{53}_7$	32A X1D66 $X_0L^{54}_7$			VDD	GND	GND	GND	GND	GND	GND	GND	VDD			32A X0D53 $X_0L^{55}_7$	32A X0D54 $X_0L^{56}_7$	32A X0D55 $X_0L^{57}_7$
N		32A X1D67 $X_0L^{58}_7$	32A X1D68 $X_0L^{59}_7$			VDD		GND		GND		GND		VDD			32A X0D51 $X_0L^{60}_7$	32A X0D52 $X_0L^{61}_7$	
P	32A X1D70 $X_0L^{62}_7$	32A X1D69 $X_0L^{63}_7$	1N X1D37 $X_1L^4_3$			VDD	VDD	VDD	USB_VDD	USB_VDD	VDD	VDD	VDD	NC			4B X1D07 $X_1L^{64}_7$	32A X0D50 $X_1L^{65}_7$	32A X0D49 $X_1L^{66}_7$
R	1O X1D38 $X_0L^5_3$	1P X1D39 $X_0L^6_3$	8D X1D17 $X_0L^7_3$														4A X1D03 $X_1L^{67}_7$	4B X1D05 $X_1L^{68}_7$	4B X1D06 $X_1L^{69}_7$
T		4D X1D16 $X_1L^3_3$	4D X1D18 $X_1L^2_3$														4A X1D02 $X_1L^{70}_7$	4B X1D04 $X_1L^{71}_7$	
U	1C X0D10 $X_1L^{73}_3$	1B X0D01 $X_1L^{72}_3$	4D X1D19 $X_1L^1_3$	1A X0D00	1D X0D11	4B X0D07	1E X1D12	USB_VDD33	USB_VBUS	USB_ID	USB_VSSAC	NC	1I X1D24	1G X0D22	1F X0D13	1H X0D23	4D X0D19 $X_1L^{74}_7$	4D X0D18 $X_1L^{75}_7$	4D X0D17 $X_1L^0_4$
V	1G X1D22 $X_1L^{94}_3$	VDDIOL	VDDIOL	4B X0D04	4B X0D06	4A X0D03	4A X0D08	4A X0D09	USB_DM	USB_DP	4C X1D21	4C X1D14	1J X1D25	4C X0D21	4C X0D14	1E X0D12	VDDIOR	VDDIOR	4D X0D16 $X_1L^4_4$
W	GND	VDDIOL	1H X1D23		4B X0D05	4A X0D02		1F X1D13	USB_RTUNE		4C X1D20	4C X1D15		4C X0D20	4C X0D15		VDDIOR	VDDIOR	GND

4 Signal Description

This section lists the signals and I/O pins available on the XE216-512-FB236. The device provides a combination of 1bit, 4bit, 8bit and 16bit ports, as well as wider ports that are fully or partially (gray) bonded out. All pins of a port provide either output or input, but signals in different directions cannot be mapped onto the same port.

Pins may have one or more of the following properties:

- PD/PU: The IO pin has a weak pull-down or pull-up resistor. The resistor is enabled during and after reset. Enabling a link or port that uses the pin disables the resistor. Thereafter, the resistor can be enabled or disabled under software control. The resistor is designed to ensure defined logic input state for unconnected pins. It should not be used to pull external circuitry. Note that the resistors are highly non-linear and only a maximum pull current is specified in Section 14.2.
- ST: The IO pin has a Schmitt Trigger on its input.
- IOL/IOT/IOR: The IO pin is powered from VDDIOL, VDDIOT, and VDDIOR respectively

Power pins (11)			
Signal	**Function**	**Type**	**Properties**
GND	Digital ground	GND	
OTP_VCC	OTP power supply	PWR	
PLL_AGND	Analog ground for PLL	PWR	
PLL_AVDD	Analog PLL power	PWR	
USB_VDD	Digital tile power	PWR	
USB_VDD33	USB Analog power	PWR	
USB_VSSAC	USB analog ground	GND	
VDD	Digital tile power	PWR	
VDDIOL	Digital I/O power (left)	PWR	
VDDIOR	Digital I/O power (right)	PWR	
VDDIOT	Digital I/O power (top)	PWR	

JTAG pins (6)			
Signal	**Function**	**Type**	**Properties**
RST_N	Global reset input	Input	IOL, PU, ST
TCK	Test clock	Input	IOL, PD, ST
TDI	Test data input	Input	IOL, PU
TDO	Test data output	Output	IOL, PD
TMS	Test mode select	Input	IOL, PU
TRST_N	Test reset input	Input	IOL, PU, ST

I/O pins (128)								
Signal	**Function**						**Type**	**Properties**
X0D00		$1A^0$					I/O	IOL, PD
X0D01	$X_0L3^2_{out}$	$1B^0$					I/O	IOL, PD
X0D02			$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	I/O	IOL, PD
X0D03			$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	I/O	IOL, PD
X0D04			$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	I/O	IOL, PD
X0D05			$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	I/O	IOL, PD
X0D06			$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	I/O	IOL, PD
X0D07			$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	I/O	IOL, PD
X0D08			$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	I/O	IOL, PD
X0D09			$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	I/O	IOL, PD
X0D10	$X_0L3^3_{out}$	$1C^0$					I/O	IOL, PD
X0D11		$1D^0$					I/O	IOL, PD
X0D12		$1E^0$					I/O	IOR, PD
X0D13		$1F^0$					I/O	IOR, PD
X0D14			$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	I/O	IOR, PD
X0D15			$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	I/O	IOR, PD
X0D16	$X_0L4^4_{in}$		$4D^0$	$8B^2$	$16A^{10}$		I/O	IOR, PD
X0D17	$X_0L4^3_{in}$		$4D^1$	$8B^3$	$16A^{11}$		I/O	IOR, PD
X0D18	$X_0L4^2_{in}$		$4D^2$	$8B^4$	$16A^{12}$		I/O	IOR, PD
X0D19	$X_0L4^1_{in}$		$4D^3$	$8B^5$	$16A^{13}$		I/O	IOR, PD
X0D20			$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	I/O	IOR, PD
X0D21			$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	I/O	IOR, PD
X0D22		$1G^0$					I/O	IOR, PD
X0D23		$1H^0$					I/O	IOR, PD
X0D24	$X_0L7^0_{in}$	$1I^0$					I/O	IOR, PD
X0D25	$X_0L7^0_{out}$	$1J^0$					I/O	IOR, PD
X0D26	$X_0L7^3_{out}$		$4E^0$	$8C^0$	$16B^0$		I/O	IOR, PD
X0D27	$X_0L7^4_{out}$		$4E^1$	$8C^1$	$16B^1$		I/O	IOR, PD
X0D28			$4F^0$	$8C^2$	$16B^2$		I/O	IOR, PD
X0D29			$4F^1$	$8C^3$	$16B^3$		I/O	IOR, PD
X0D30			$4F^2$	$8C^4$	$16B^4$		I/O	IOR, PD
X0D31			$4F^3$	$8C^5$	$16B^5$		I/O	IOR, PD
X0D32			$4E^2$	$8C^6$	$16B^6$		I/O	IOR, PD
X0D33			$4E^3$	$8C^7$	$16B^7$		I/O	IOR, PD
X0D34	$X_0L7^1_{out}$	$1K^0$					I/O	IOR, PD
X0D35	$X_0L7^2_{out}$	$1L^0$					I/O	IOR, PD
X0D36		$1M^0$		$8D^0$	$16B^8$		I/O	IOL, PD
X0D37	$X_0L0^4_{in}$	$1N^0$		$8D^1$	$16B^9$		I/O	IOL, PD
X0D38	$X_0L0^3_{in}$	$1O^0$		$8D^2$	$16B^{10}$		I/O	IOL, PD
X0D39	$X_0L0^2_{in}$	$1P^0$		$8D^3$	$16B^{11}$		I/O	IOL, PD
X0D40	$X_0L0^1_{in}$			$8D^4$	$16B^{12}$		I/O	IOL, PD

(continued)

Signal	Function					Type	Properties
X0D41	$X_0L0^0_{in}$		8D[5]	16B[13]		I/O	IOL, PD
X0D42	$X_0L0^0_{out}$		8D[6]	16B[14]		I/O	IOL, PD
X0D43	$X_0L0^1_{out}$		8D[7]	16B[15]		I/O	IOL, PD
X0D49	$X_0L5^4_{in}$				32A[0]	I/O	IOR, PD
X0D50	$X_0L5^3_{in}$				32A[1]	I/O	IOR, PD
X0D51	$X_0L5^2_{in}$				32A[2]	I/O	IOR, PD
X0D52	$X_0L5^1_{in}$				32A[3]	I/O	IOR, PD
X0D53	$X_0L5^0_{in}$				32A[4]	I/O	IOR, PD
X0D54	$X_0L5^0_{out}$				32A[5]	I/O	IOR, PD
X0D55	$X_0L5^1_{out}$				32A[6]	I/O	IOR, PD
X0D56	$X_0L5^2_{out}$				32A[7]	I/O	IOR, PD
X0D57	$X_0L5^3_{out}$				32A[8]	I/O	IOR, PD
X0D58	$X_0L5^4_{out}$				32A[9]	I/O	IOR, PD
X0D61	$X_0L6^4_{in}$				32A[10]	I/O	IOR, PD
X0D62	$X_0L6^3_{in}$				32A[11]	I/O	IOR, PD
X0D63	$X_0L6^2_{in}$				32A[12]	I/O	IOR, PD
X0D64	$X_0L6^1_{in}$				32A[13]	I/O	IOR, PD
X0D65	$X_0L6^0_{in}$				32A[14]	I/O	IOR, PD
X0D66	$X_0L6^0_{out}$				32A[15]	I/O	IOR, PD
X0D67	$X_0L6^1_{out}$				32A[16]	I/O	IOR, PD
X0D68	$X_0L6^2_{out}$				32A[17]	I/O	IOR, PD
X0D69	$X_0L6^3_{out}$				32A[18]	I/O	IOR, PD
X0D70	$X_0L6^4_{out}$				32A[19]	I/O	IOR, PD
X1D00	$X_0L7^2_{in}$	1A[0]				I/O	IOR, PD
X1D01	$X_0L7^1_{in}$	1B[0]				I/O	IOR, PD
X1D02	$X_0L4^0_{in}$		4A[0]	8A[0]	16A[0]	32A[20]	I/O	IOR, PD
X1D03	$X_0L4^0_{out}$		4A[1]	8A[1]	16A[1]	32A[21]	I/O	IOR, PD
X1D04	$X_0L4^1_{out}$		4B[0]	8A[2]	16A[2]	32A[22]	I/O	IOR, PD
X1D05	$X_0L4^2_{out}$		4B[1]	8A[3]	16A[3]	32A[23]	I/O	IOR, PD
X1D06	$X_0L4^3_{out}$		4B[2]	8A[4]	16A[4]	32A[24]	I/O	IOR, PD
X1D07	$X_0L4^4_{out}$		4B[3]	8A[5]	16A[5]	32A[25]	I/O	IOR, PD
X1D08	$X_0L7^4_{in}$		4A[2]	8A[6]	16A[6]	32A[26]	I/O	IOR, PD
X1D09	$X_0L7^3_{in}$		4A[3]	8A[7]	16A[7]	32A[27]	I/O	IOR, PD
X1D10		1C[0]					I/O	IOT, PD
X1D11		1D[0]					I/O	IOT, PD
X1D12		1E[0]					I/O	IOL, PD
X1D13		1F[0]					I/O	IOL, PD
X1D14			4C[0]	8B[0]	16A[8]	32A[28]	I/O	IOR, PD
X1D15			4C[1]	8B[1]	16A[9]	32A[29]	I/O	IOR, PD
X1D16	$X_0L3^1_{in}$		4D[0]	8B[2]	16A[10]		I/O	IOL, PD
X1D17	$X_0L3^0_{in}$		4D[1]	8B[3]	16A[11]		I/O	IOL, PD
X1D18	$X_0L3^0_{out}$		4D[2]	8B[4]	16A[12]		I/O	IOL, PD
X1D19	$X_0L3^1_{out}$		4D[3]	8B[5]	16A[13]		I/O	IOL, PD

(continued)

Signal	Function						Type	Properties
X1D20			4C[2]	8B[6]	16A[14]	32A[30]	I/O	IOR, PD
X1D21			4C[3]	8B[7]	16A[15]	32A[31]	I/O	IOR, PD
X1D22	$X_0L3^4_{out}$	1G[0]					I/O	IOL, PD
X1D23		1H[0]					I/O	IOL, PD
X1D24		1I[0]					I/O	IOR, PD
X1D25		1J[0]					I/O	IOR, PD
X1D26	tx_clk (rgmii)		4E[0]	8C[0]	16B[0]		I/O	IOT, PD
X1D27	tx_ctl (rgmii)		4E[1]	8C[1]	16B[1]		I/O	IOT, PD
X1D28	rx_clk (rgmii)		4F[0]	8C[2]	16B[2]		I/O	IOT, PD
X1D29	rx_ctl (rgmii)		4F[1]	8C[3]	16B[3]		I/O	IOT, PD
X1D30	rx0 (rgmii)		4F[2]	8C[4]	16B[4]		I/O	IOT, PD
X1D31	rx1 (rgmii)		4F[3]	8C[5]	16B[5]		I/O	IOT, PD
X1D32	rx2 (rgmii)		4E[2]	8C[6]	16B[6]		I/O	IOT, PD
X1D33	rx3 (rgmii)		4E[3]	8C[7]	16B[7]		I/O	IOT, PD
X1D34	$X_0L0^2_{out}$	1K[0]					I/O	IOL, PD
X1D35	$X_0L0^3_{out}$	1L[0]					I/O	IOL, PD
X1D36	$X_0L0^4_{out}$	1M[0]		8D[0]	16B[8]		I/O	IOL, PD
X1D37	$X_0L3^4_{in}$	1N[0]		8D[1]	16B[9]		I/O	IOL, PD
X1D38	$X_0L3^3_{in}$	1O[0]		8D[2]	16B[10]		I/O	IOL, PD
X1D39	$X_0L3^2_{in}$	1P[0]		8D[3]	16B[11]		I/O	IOL, PD
X1D40	tx3 (rgmii)			8D[4]	16B[12]		I/O	IOT, PD
X1D41	tx2 (rgmii)			8D[5]	16B[13]		I/O	IOT, PD
X1D42	tx1 (rgmii)			8D[6]	16B[14]		I/O	IOT, PD
X1D43	tx0 (rgmii)			8D[7]	16B[15]		I/O	IOT, PD
X1D49	$X_0L1^4_{in}$					32A[0]	I/O	IOL, PD
X1D50	$X_0L1^3_{in}$					32A[1]	I/O	IOL, PD
X1D51	$X_0L1^2_{in}$					32A[2]	I/O	IOL, PD
X1D52	$X_0L1^1_{in}$					32A[3]	I/O	IOL, PD
X1D53	$X_0L1^0_{in}$					32A[4]	I/O	IOL, PD
X1D54	$X_0L1^0_{out}$					32A[5]	I/O	IOL, PD
X1D55	$X_0L1^1_{out}$					32A[6]	I/O	IOL, PD
X1D56	$X_0L1^2_{out}$					32A[7]	I/O	IOL, PD
X1D57	$X_0L1^3_{out}$					32A[8]	I/O	IOL, PD
X1D58	$X_0L1^4_{out}$					32A[9]	I/O	IOL, PD
X1D61	$X_0L2^4_{in}$					32A[10]	I/O	IOL, PD
X1D62	$X_0L2^3_{in}$					32A[11]	I/O	IOL, PD
X1D63	$X_0L2^2_{in}$					32A[12]	I/O	IOL, PD
X1D64	$X_0L2^1_{in}$					32A[13]	I/O	IOL, PD
X1D65	$X_0L2^0_{in}$					32A[14]	I/O	IOL, PD
X1D66	$X_0L2^0_{out}$					32A[15]	I/O	IOL, PD
X1D67	$X_0L2^1_{out}$					32A[16]	I/O	IOL, PD
X1D68	$X_0L2^2_{out}$					32A[17]	I/O	IOL, PD
X1D69	$X_0L2^3_{out}$					32A[18]	I/O	IOL, PD

(continued)

Signal	Function	Type	Properties
X1D70	$X_0L2^4_{out}$ $32A^{19}$	I/O	IOL, PD

System pins (3)			
Signal	**Function**	**Type**	**Properties**
CLK	PLL reference clock	Input	IOL, PD, ST
DEBUG_N	Multi-chip debug	I/O	IOL, PU
MODE[1:0]	Boot mode select	Input	PU

usb pins (5)			
Signal	**Function**	**Type**	**Properties**
USB_DM	USB Serial Data Inverted	I/O	
USB_DP	USB Serial Data	I/O	
USB_ID	USB Device ID (OTG) - Reserved	I/O	
USB_RTUNE	USB resistor	I/O	
USB_VBUS	USB Power Detect Pin	I/O	

5 Example Application Diagram

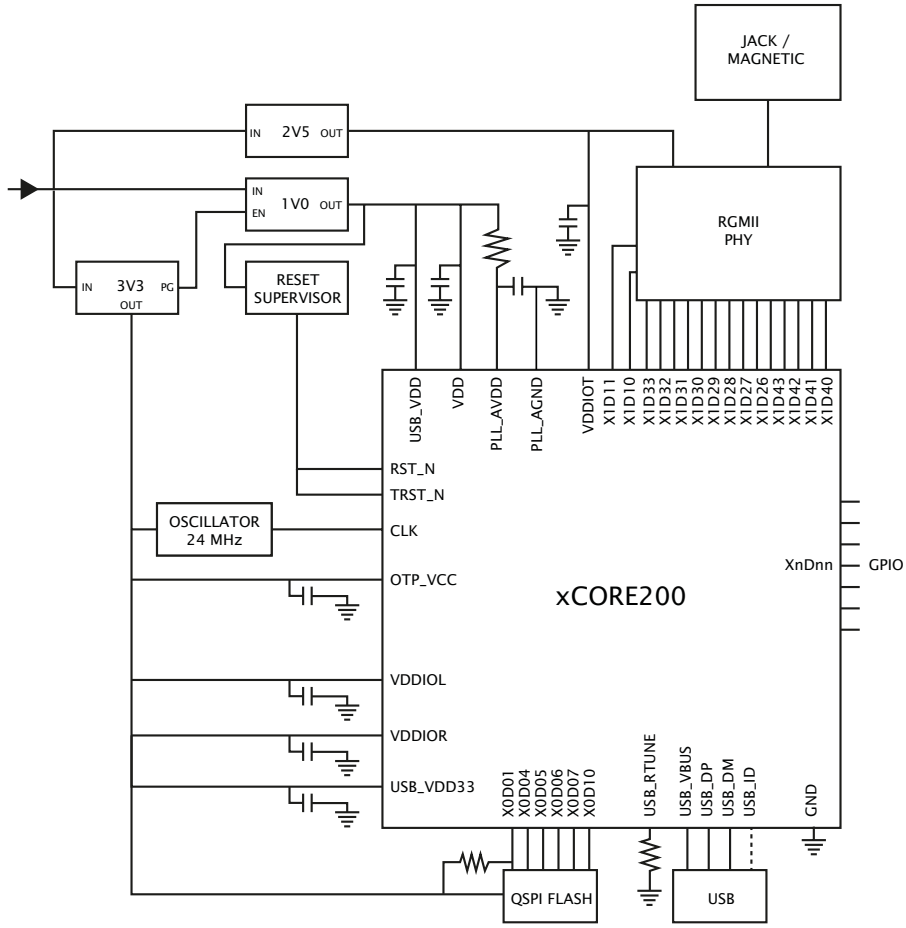

Figure 2: Simplified Reference Schematic

- see Section 10 for details on the USB PHY
- see Section 11 for details on RGMII integration
- see Section 13 for details on the power supplies and PCB design

6 Product Overview

The XE216-512-FB236 is a powerful device that consists of two xCORE Tiles, each comprising a flexible logical processing cores with tightly integrated I/O and on-chip memory.

6.1 Logical cores

Each tile has 8 active logical cores, which issue instructions down a shared five-stage pipeline. Instructions from the active cores are issued round-robin. If up to five logical cores are active, each core is allocated a fifth of the processing cycles. If more than five logical cores are active, each core is allocated at least $1/n$ cycles (for n cores). Figure 3 shows the guaranteed core performance depending on the number of cores used.

Figure 3: Logical core performance

Speed grade	MIPS	Frequency	Minimum MIPS per core (for *n* cores)							
			1	2	3	4	5	6	7	8
10	1000 MIPS	500 MHz	100	100	100	100	100	83	71	63

There is no way that the performance of a logical core can be reduced below these predicted levels (unless *priority threads* are used: in this case the guaranteed minimum performance is computed based on the number of priority threads as defined in the architecture manual). Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than five logical cores, the performance of each core is often higher than the predicted minimum but cannot be guaranteed.

The logical cores are triggered by events instead of interrupts and run to completion. A logical core can be paused to wait for an event.

6.2 xTIME scheduler

The xTIME scheduler handles the events generated by xCORE Tile resources, such as channel ends, timers and I/O pins. It ensures that all events are serviced and synchronized, without the need for an RTOS. Events that occur at the I/O pins are handled by the Hardware-Response ports and fed directly to the appropriate xCORE Tile. An xCORE Tile can also choose to wait for a specified time to elapse, or for data to become available on a channel.

Tasks do not need to be prioritised as each of them runs on their own logical xCORE. It is possible to share a set of low priority tasks on a single core using cooperative multitasking.

6.3 Hardware Response Ports

Hardware Response ports connect an xCORE tile to one or more physical pins and as such define the interface between hardware attached to the XE216-512-FB236, and the software running on it. A combination of 1bit, 4bit, 8bit, 16bit and 32bit

ports are available. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

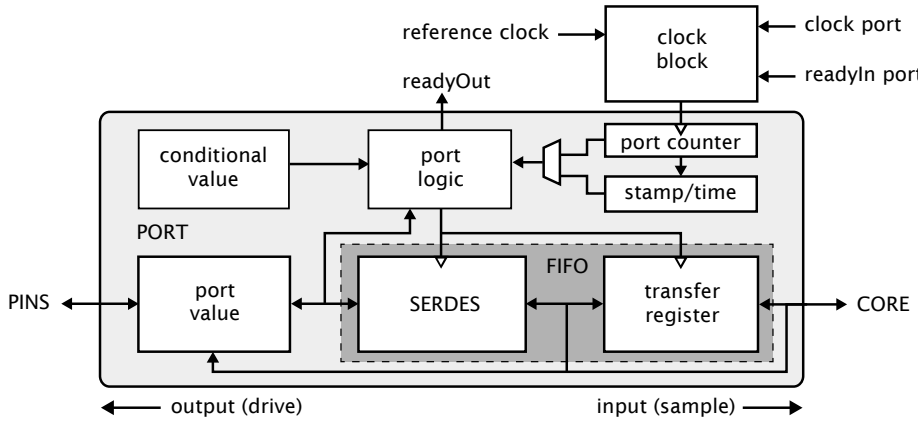

Figure 4: Port block diagram

The port logic can drive its pins high or low, or it can sample the value on its pins, optionally waiting for a particular condition. Ports are accessed using dedicated instructions that are executed in a single processor cycle. xCORE-200 IO pins can be used as *open collector* outputs, where signals are driven low if a zero is output, but left high impedance if a one is output. This option is set on a per-port basis.

Data is transferred between the pins and core using a FIFO that comprises a SERDES and transfer register, providing options for serialization and buffered data.

Each port has a 16-bit counter that can be used to control the time at which data is transferred between the port value and transfer register. The counter values can be obtained at any time to find out when data was obtained, or used to delay I/O until some time in the future. The port counter value is automatically saved as a timestamp, that can be used to provide precise control of response times.

The ports and xCONNECT links are multiplexed onto the physical pins. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

6.4 Clock blocks

xCORE devices include a set of programmable clocks called clock blocks that can be used to govern the rate at which ports execute. Each xCORE tile has six clock blocks: the first clock block provides the tile reference clock and runs at a default frequency of 100MHz; the remaining clock blocks can be set to run at different frequencies.

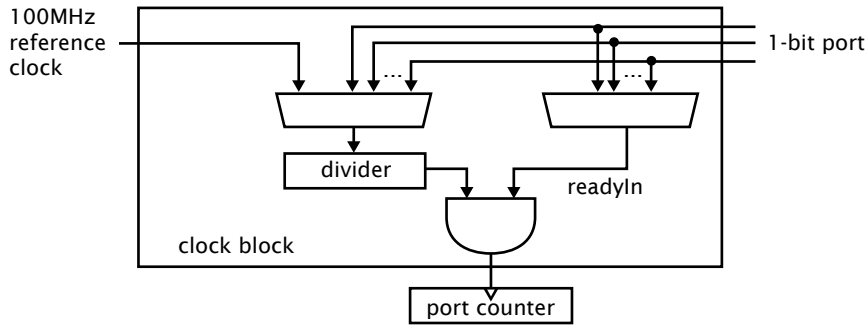

Figure 5: Clock block diagram

A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces. xCORE-200 clock blocks optionally divide the clock input from a 1-bit port.

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

6.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

6.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming

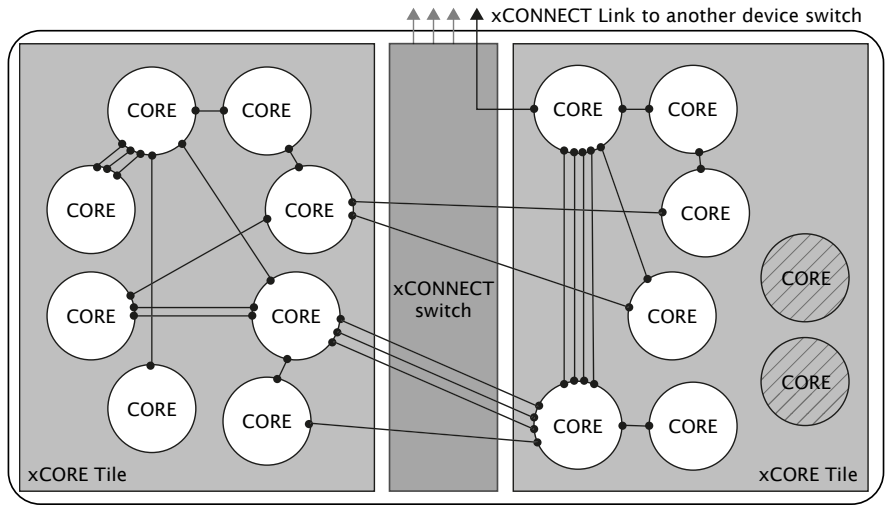

Figure 6: Switch, links and channel ends

and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-UE Link Performance and Design Guide, X2999.

7 PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock. The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 7:

Figure 7: PLL multiplier values and MODE pins

Oscillator Frequency	MODE 1	MODE 0	Tile Boot Frequency	PLL Ratio	PLL settings OD	F	R
3.25-10 MHz	0	0	130-400 MHz	40	1	159	0
9-25 MHz	1	1	144-400 MHz	16	1	63	0
25-50 MHz	1	0	167-400 MHz	8	1	31	0
50-100 MHz	0	1	196-400 MHz	4	1	15	0

Figure 7 also lists the values of OD, F and R, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

OD, F and R must be chosen so that $0 \leq R \leq 63$, $0 \leq F \leq 4095$, $0 \leq OD \leq 7$, and $260MHz \leq F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \leq 1.3GHz$. The OD, F, and R values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value during and after deassertion of the system reset. If the USB PHY is used, then either a 24 MHz or 12 MHz oscillator must be used.

If a different tile frequency is required (eg, 500 MHz), then the PLL must be reprogrammed after boot to provide the required tile frequency. The XMOS tools perform this operation by default. Further details on configuring the clock can be found in the xCORE-200 Clock Frequency Control document.

8 Boot Procedure

The device is kept in reset by driving RST_N low. When in reset, all GPIO pins have a pull-down enabled. When the device is taken out of reset by releasing RST_N the processor starts its internal reset process. After 15-150 μs (depending on the input clock) the processor boots.

The xCORE Tile boot procedure is illustrated in Figure 8. If bit 5 of the security register (*see* §9.1) is set, the device boots from OTP. To get a high value, a 3K3 pull-up resistor should be strapped onto the pin. To assure a low value, a pull-down resistor is required if other external devices are connected to this port.

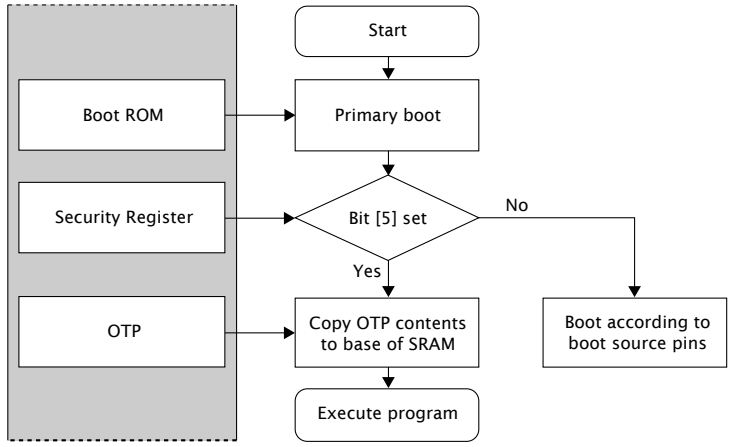

Figure 8: Boot procedure

The boot image has the following format:

- A 32-bit program size s in words.

X0D06	X0D05	X0D04	Tile 0 boot	Tile 1 boot	Enabled links
0	0	0	QSPI master	Channel end 0	None
0	0	1	SPI master	Channel end 0	None
0	1	0	SPI slave	Channel end 0	None
0	1	1	SPI slave	SPI slave	None
1	0	0	Channel end 0	Channel end 0	XL0 (2w)
1	0	1	Channel end 0	Channel end 0	XL4-XL7 (5w)
1	1	0	Channel end 0	Channel end 0	XL1, XL2, XL5, and XL6 (5w)
1	1	1	Channel end 0	Channel end 0	XL0-XL3 (5w)

Figure 9: Boot source pins

- Program consisting of $s \times 4$ bytes.
- A 32-bit CRC, or the value 0x0D15AB1E to indicate that no CRC check should be performed.

The program size and CRC are stored least significant byte first. The program is loaded into the lowest memory address of RAM, and the program is started from that address. The CRC is calculated over the byte stream represented by the program size and the program itself. The polynomial used is 0xEDB88320 (IEEE 802.3); the CRC register is initialized with 0xFFFFFFFF and the residue is inverted to produce the CRC.

8.1 Boot from QSPI master

If set to boot from QSPI master, the processor enables the six pins specified in Figure 10, and drives the SPI clock at 50 MHz (assuming a 400 MHz core clock). A READ command is issued with a 24-bit address 0x000000. The clock polarity and phase are 0 / 0.

Pin	Signal	Description
X0D01	SS	Slave Select
X0D04..X0D07	SPIO	Data
X0D10	SCLK	Clock

Figure 10: QSPI pins

The xCORE Tile expects each byte to be transferred with the *least-significant nibble first*. Programmers who write bytes into an QSPI interface using the most significant nibble first may have to reverse the nibbles in each byte of the image stored in the QSPI device.

The pins used for QSPI boot are hardcoded in the boot ROM and cannot be changed. If required, an QSPI boot program can be burned into OTP that uses different pins.

8.2 Boot from SPI master

If set to boot from SPI master, the processor enables the four pins specified in Figure 11, and drives the SPI clock at 2.5 MHz (assuming a 400 MHz core clock). A READ command is issued with a 24-bit address 0x000000. The clock polarity and phase are 0 / 0.

Figure 11: SPI master pins

Pin	Signal	Description
X0D00	MISO	Master In Slave Out (Data)
X0D01	SS	Slave Select
X0D10	SCLK	Clock
X0D11	MOSI	Master Out Slave In (Data)

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. Programmers who write bytes into an SPI interface using the most significant bit first may have to reverse the bits in each byte of the image stored in the SPI device.

If a large boot image is to be read in, it is faster to first load a small boot-loader that reads the large image using a faster SPI clock, for example 50 MHz or as fast as the flash device supports.

The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

8.3 Boot from SPI slave

If set to boot from SPI slave, the processor enables the three pins specified in Figure 12 and expects a boot image to be clocked in. The supported clock polarity and phase are 0/0 and 1/1.

Figure 12: SPI slave pins

Pin	Signal	Description
X0D00	SS	Slave Select
X0D10	SCLK	Clock
X0D11	MOSI	Master Out Slave In (Data)

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

8.4 Boot from xConnect Link

If set to boot from an xConnect Link, the processor enables its link(s) around 2 us after the boot process starts. Enabling the Link switches off the pull-down resistors on the link, drives all the TX wires low (the initial state for the Link), and monitors the RX pins for boot-traffic; they must be low at this stage. If the internal pull-down is too weak to drain any residual charge, external pull-downs of 10K may be required on those pins.

The boot-rom on the core will then:

1. Allocate channel-end 0.
2. Input a word on channel-end 0. It will use this word as a channel to acknowledge the boot. Provide the null-channel-end 0x0000FF02 if no acknowledgment is required.
3. Input the boot image specified above, including the CRC.
4. Input an END control token.
5. Output an END control token to the channel-end received in step 2.
6. Free channel-end 0.
7. Jump to the loaded code.

8.5 Boot from OTP

If an xCORE tile is set to use secure boot (see Figure 8), the boot image is read from address 0 of the OTP memory in the tile's security module.

This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.

Each tile has its own individual OTP memory, and hence some tiles can be booted from OTP while others are booted from SPI or the channel interface. This enables systems to be partially programmed, dedicating one or more tiles to perform a particular function, leaving the other tiles user-programmable.

8.6 Security register

The security register enables security features on the xCORE tile. The features shown in Figure 13 provide a strong level of protection and are sufficient for providing strong IP security.

9 Memory

9.1 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in four sectors each containing 512 rows of 32 bits which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

Feature	Bit	Description
Disable JTAG	0	The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
Disable Link access	1	Other tiles are forbidden access to the processor state via the system switch. Disabling both JTAG and Link access transforms an xCORE Tile into a "secure island" with other tiles free for non-secure user application code.
Secure Boot	5	The xCORE Tile is forced to boot from address 0 of the OTP, allowing the xCORE Tile boot ROM to be bypassed (*see* §8).
Redundant rows	7	Enables redundant rows in OTP.
Sector Lock 0	8	Disable programming of OTP sector 0.
Sector Lock 1	9	Disable programming of OTP sector 1.
Sector Lock 2	10	Disable programming of OTP sector 2.
Sector Lock 3	11	Disable programming of OTP sector 3.
OTP Master Lock	12	Disable OTP programming completely: disables updates to all sectors and security register.
Disable JTAG-OTP	13	Disable all (read & write) access from the JTAG interface to this OTP.
Disable Global Debug	14	Disables access to the DEBUG_N pin.
	21..15	General purpose software accessable security register available to end-users.
	31..22	General purpose user programmable JTAG UserID code extension.

Figure 13: Security register features

The OTP memory is programmed using three special I/O ports: the OTP address port is a 16-bit port with resource ID 0x100200, the OTP data is written via a 32-bit port with resource ID 0x200100, and the OTP control is on a 16-bit port with ID 0x100300. Programming is performed through `libotp` and `xburn`.

9.2 SRAM

Each xCORE Tile integrates a single 256KB SRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or 32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

10 USB PHY

The USB PHY provides High-Speed and Full-Speed, device, host, and on-the-go functionality. The PHY is configured through a set of peripheral registers (Appendix F),

and data is communicated through ports on the digital node. A library, XUD, is provided to implement *USB-device* functionality.

The USB PHY is connected to the ports on Tile 0 and Tile 1 as shown in Figure 14. When the USB PHY is enabled on Tile 0, the ports shown can on Tile 0 only be used with the USB PHY. When the USB PHY is enabled on Tile 1, then the ports shown can on Tile 1 only be used with the USB PHY. All other IO pins and ports are unaffected. The USB PHY should not be enabled on both tiles. Two clock blocks can be used to clock the USB ports. One clock block for the TXDATA path, and one clock block for the RXDATA path. Details on how to connect those ports are documented in an application note on USB for xCORE-200.

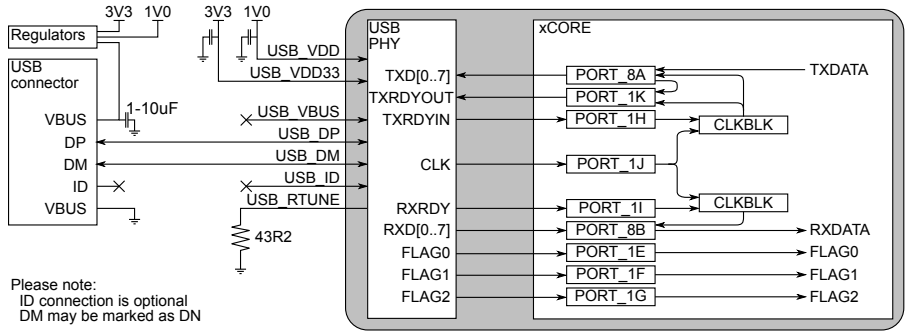

Figure 14: Bus powered *USB-device*

An external resistor of 43.2 ohm (1% tolerance) should connect USB_RTUNE to ground, as close as possible to the device.

10.1 USB VBUS

USB_VBUS need not be connected if the device is wholly powered by USB, and the device is used to implement a *USB-device*.

If you use the USB PHY to design a self-powered *USB-device*, then the device must be able detect the presence of VBus on the USB connector (so the device can disconnect its pull-up resistors from D+/D- to ensure the device does not have any voltage on the D+/D- pins when VBus is not present, “USB Back Voltage Test”). This requires USB_VBUS to be connected to the VBUS pin of the USB connector as is shown in Figure 15.

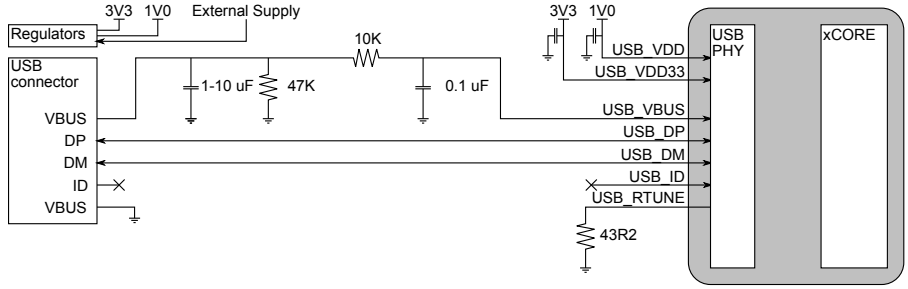

Figure 15: Self powered *USB-device*

When connecting a USB cable to the device it is possible an overvoltage transient will be present on VBus due to the inductance of the USB cable combined with the required input capacitor on VBus. The circuit in Figure 15 ensures that the transient does not damage the device. The 10k series resistor and 0.1uF capacitor ensure than any input transient is filtered and does not reach the device. The 47k resistor to ground is a bleeder resistor to discharge the input capacitor when VBus is not present. The 1-10uF input capacitor is required as part of the USB specification. A typical value would be 2.2uF to ensure the 1uF minimum requirement is met even under voltage bias conditions.

In any case, extra components (such as a ferrite bead and diodes) may be required for EMC compliance and ESD protection. Different wiring is required for USB-host and USB-OTG.

10.2 Logical Core Requirements

The XMOS XUD software component runs in a single logical core with endpoint and application cores communicating with it via a combination of channel communication and shared memory variables.

Each IN (host requests data from device) or OUT (data transferred from host to device) endpoint requires one logical core.

11 RGMII

The device has a series of pins that are dedicated to communicate with an RGMII PHY, as per the RGMII v1.3 spec. This can be used to communicate with GBit Ethernet PHYs. The pins and functions are listed in Figure 16. When RGMII mode is enabled (using processor status register 2) these pins can no longer be used as GPIO pins, and will instead be driven directly from an RGMII block that provides DDR to SDR conversion, which in turn is interfaced to a set of ports on Tile 1.

Figure 16: RGMII block pin functions

Pin	RGMII Function	
X1D40	TX3	Transmit bit 3
X1D41	TX2	Transmit bit 2
X1D42	TX1	Transmit bit 1
X1D43	TX0	Transmit bit 0
X1D26	TX_CLK	Receive clock (125 MHz)
X1D27	TX_CTL	Transmit data valid/error
X1D28	RX_CLK	Receive clock (125 MHz)
X1D29	RX_CTL	Receive data valid/error
X1D30	RX0	Receive bit 0
X1D31	RX1	Receive bit 1
X1D32	RX2	Receive bit 2
X1D33	RX3	Receive bit 3

The RGMII block is connected to the ports on Tile 1 as shown in Figure 17. When the RGMII block is enabled, the ports shown can only be used with the RGMII block, and IO pins X1D26..X1D33/X1D40..X1D43 can only be used with the RGMII block. Ports and pins not used in Figure 17 can be used as normal.

The RGMII block generates a clock (configured using processor status register 2), and has the facility to delay the outgoing clock edge, putting it out of phase with the data. The RGMII block translates the double data-rate 4-wire data signals and 1-wire control signal into single-data rate 8-wire TX and DX signals and two control signals. Figure 17 shows how four clock blocks can be used to clock the RGMII ports. One clock block for the TXDATA path, one clock block for the RXDATA path, one clock block to delay the TX_CLK, and one clock block clocked on a negative valid signal to enable mode switching between 10/100/1000 speeds. Details on how to connect those ports are documented in an application note on RGMII for xCORE200. The XMOS RGMII software component runs a MAC layer on Tile 1.

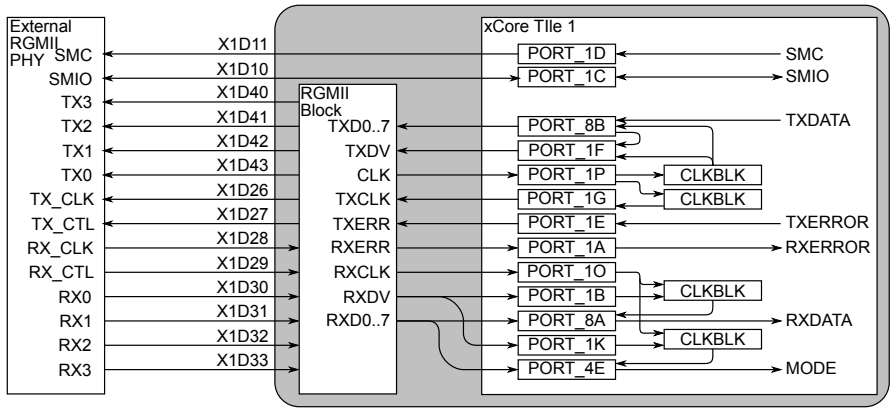

Figure 17: RGMII port functions on Tile 1

The SMI interface should be connected to two one-bit ports that are configured as open-drain IOs, using external pull-ups to 2.5V. Ports 1C and 1D are notionally allocated for this, but any GPIO can be used for this purpose.

The bundles of RX and TX pins should be wired using matched trace-lengths over an uninterrupted ground-plane. The RGMII pins are supplied through the VDDIOT supply pins, which should be provided with 2.5V. Decouplers should be placed with a short path to VDDIOT and ground. If the PHY supports a 3.3V IO voltage, then a 3.3V supply can be used for VDDIOT.

The RGMII PHY should be configured so that RX_CLK is low during reset of the xCORE. This may be achieved by putting a pull-down resistor on the reset of the PHY, keeping the PHY in reset until the RGMII layer on the xCORE takes the PHY out of reset.

12 JTAG

The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory.

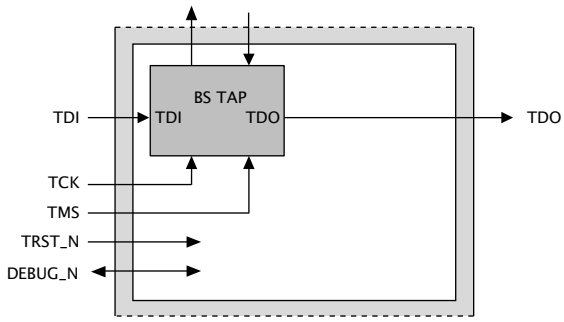

Figure 18: JTAG chain structure

The JTAG chain structure is illustrated in Figure 18. It comprises a single 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. It has a 4-bit IR and 32-bit DR. It also provides access to a chip TAP that in turn can access the xCORE Tile for loading code and debugging.

The TRST_N pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the TRST_N pin can be tied to ground to hold the JTAG module in reset.

The DEBUG_N pin is used to synchronize the debugging of multiple xCORE Tiles. This pin can operate in both output and input mode. In output mode and when configured to do so, DEBUG_N is driven low by the device when the processor hits a debug break point. Prior to this point the pin will be tri-stated. In input mode and when configured to do so, driving this pin low will put the xCORE Tile into debug mode. Software can set the behavior of the xCORE Tile based on this pin. This pin should have an external pull up of 4K7-47KΩ or left not connected in single core applications.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 19.

Figure 19: IDCODE return value

Bit31				Device Identification Register																										Bit0
Version				Part Number																Manufacturer Identity										1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1
0				0				0				0				6				6				3				3			