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XMC4700 / XMC4800

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM[®] Cortex[®]-M4
32-bit processor core

Data Sheet

V1.0 2016-01

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Microcontroller Series
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XMC4[78]00 Data Sheet

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Page	Subjects
8	Corrected EtherCAT features to 8 Fieldbus Memory Management Units (FMMU) and 8 Sync Manager.
46	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
53	Added HIBIO characteristics.
58	Corrected DAC INL and gain error.
70	Changed frequency dependency of the current consumption.
73	Added peripheral idle current overview.
127ff	Updated package parameters and drawings.
132	Higher HBM and CDM ESD limits.

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc4000> to get access to the latest versions of those documents.

1 Summary of Features

The XMC4[78]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

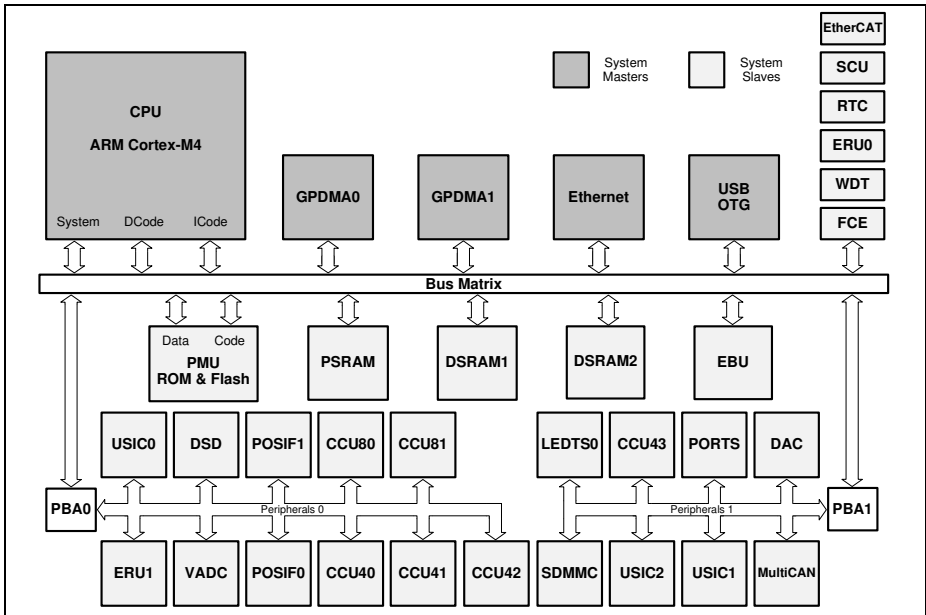


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High Performance 32-bit ARM Cortex-M4 CPU
 - 16-bit and 32-bit Thumb2 instruction set
 - DSP/MAC instructions
 - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 96 KB on-chip high-speed program memory
- 128 KB on-chip high speed data memory
- 128 KB on-chip high-speed communication memory
- 2,048 KB on-chip Flash Memory with 8 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- EtherCATSlave interface (ECAT) capable of 100 Mbit/s transfer rates with 2 MII ports, 8 Fieldbus Memory Management Units (FMMU), 8 Sync Manager, 64 bit distributed clocks
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 6 nodes, 256 message objects (MO), data rate up to 1 Mbaud
- Six Universal Serial Interface Channels (USIC), providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability

- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - E: LFBGA
 - F: LQFP
 - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4[78]00 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4[78]00 series, some descriptions may not apply to a specific product. Please see [Table 1](#).

For simplicity the term **XMC4[78]00** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4[78]00 Device Types

Derivative¹⁾	Package	Flash Kbytes	SRAM Kbytes
XMC4700-E196x2048	PG-LFBGA-196	2048	352
XMC4700-F144x2048	PG-LQFP-144	2048	352
XMC4700-F100x2048	PG-LQFP-100	2048	352
XMC4700-E196x1536	PG-LFBGA-196	1536	276

Summary of Features
Table 1 Synopsis of XMC4[78]00 Device Types (cont'd)

Derivative ¹⁾	Package	Flash Kbytes	SRAM Kbytes
XMC4700-F144x1536	PG-LQFP-144	1536	276
XMC4700-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x2048	PG-LFBGA-196	2048	352
XMC4800-F144x2048	PG-LQFP-144	2048	352
XMC4800-F100x2048	PG-LQFP-100	2048	352
XMC4800-E196x1536	PG-LFBGA-196	1536	276
XMC4800-F144x1536	PG-LQFP-144	1536	276
XMC4800-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x1024	PG-LFBGA-196	1024	200
XMC4800-F144x1024	PG-LQFP-144	1024	200
XMC4800-F100x1024	PG-LQFP-100	1024	200

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4[78]00 Device Types

Derivative ¹⁾	LED TS Intf.	SD MMC Intf.	EBU Intf. ²⁾	ETH Intf. ³⁾	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4700-E196x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x2048	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-E196x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x1536	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]

Summary of Features
Table 2 Features of XMC4[78]00 Device Types (cont'd)

Derivative ¹⁾	LED TS Intf.	SD MMC Intf.	EBU Intf. ²⁾	ETH Intf. ³⁾	ECAT Slave Intf.	USB Intf.	USIC Chan.	MulticAN Nodes, MO
XMC4800-E196x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x2048	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1536	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1024	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]

1) x is a placeholder for the supported temperature range.

2) Memory types supported S=SDRAM, D=DEMUX, M=MUX 16-bit and 32-bit, M16=MUX 16-bit

3) Supported interfaces, M=MII, R=RMII.

Table 3 Features of XMC4[78]00 Device Types

Derivative ¹⁾	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.
XMC4700-E196x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4700-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x2048	32	4	2	4 x 4	2 x 4	2

Summary of Features

Table 3 Features of XMC4[78]00 Device Types (cont'd)

Derivative ¹⁾	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.
XMC4800-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1024	24	4	2	4 x 4	2 x 4	2

1) x is a placeholder for the supported temperature range.

1.4 Definition of Feature Variants

The XMC4[78]00 types are offered with several memory sizes and number of available VADC channels. [Table 4](#) describes the location of the available Flash memory, [Table 5](#) describes the location of the available SRAMs, [Table 6](#) the available VADC channels.

Table 4 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
1,024 Kbytes	0800 0000 _H – 080F FFFF _H	0C00 0000 _H – 0C0F FFFF _H
1,536 Kbytes	0800 0000 _H – 0817 FFFF _H	0C00 0000 _H – 0C17 FFFF _H
2,048 Kbytes	0800 0000 _H – 081F FFFF _H	0C00 0000 _H – 0C1F FFFF _H

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
200 Kbytes	1FFE E000 _H – 1FFF FFFF _H	2000 0000 _H – 2001 FFFF _H	–
276 Kbytes	1FFE 8000 _H – 1FFF FFFF _H	2000 0000 _H – 2001 FFFF _H	2002 0000 _H – 2002 CFFF _H
352 Kbytes	1FFE 8000 _H – 1FFF FFFF _H	2000 0000 _H – 2001 FFFF _H	2002 0000 _H – 2003 FFFF _H

Table 6 ADC Channels¹⁾

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-144 PG-LFBGA-196	CH0..CH7	CH0..CH7	CH0..CH7	CH0..CH7
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4700 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 7001 _H	EES-AA, ES-AA, AA
JTAG IDCODE	101D F083 _H	EES-AA, ES-AA, AA

Table 8 XMC4800 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 8001 _H	EES-AA, ES-AA, AA
JTAG IDCODE	101D F083 _H	EES-AA, ES-AA, AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

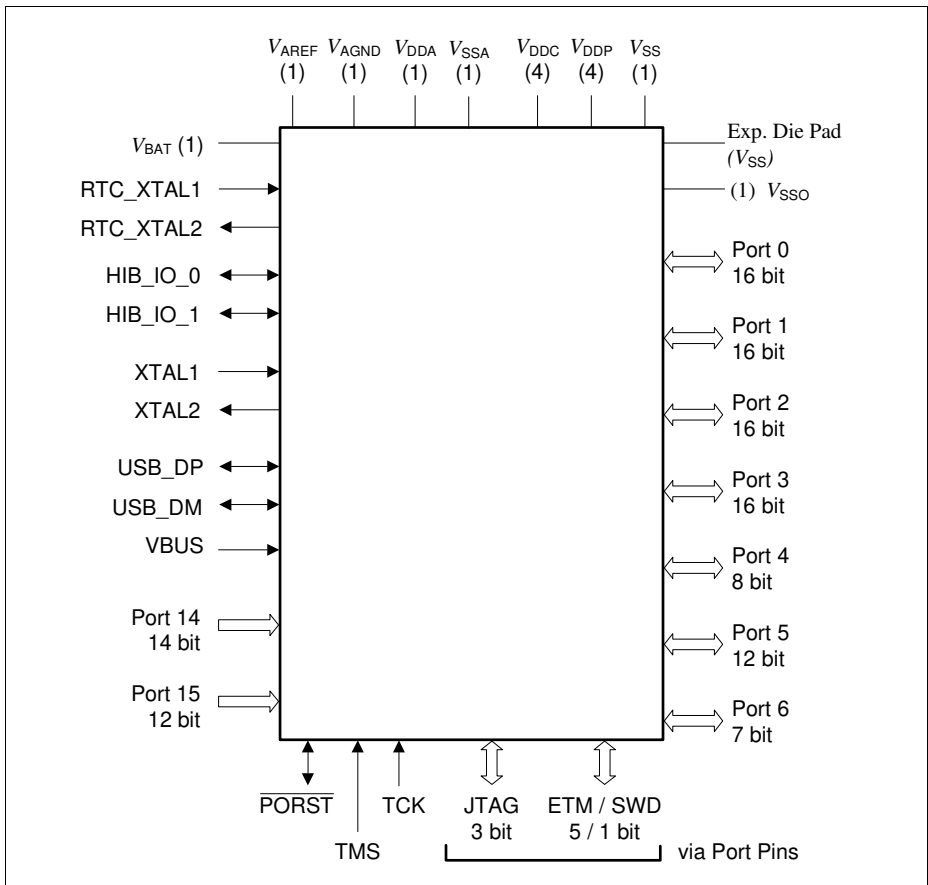


Figure 2 XMC4[78]00 Logic Symbol PG-LQFP-144

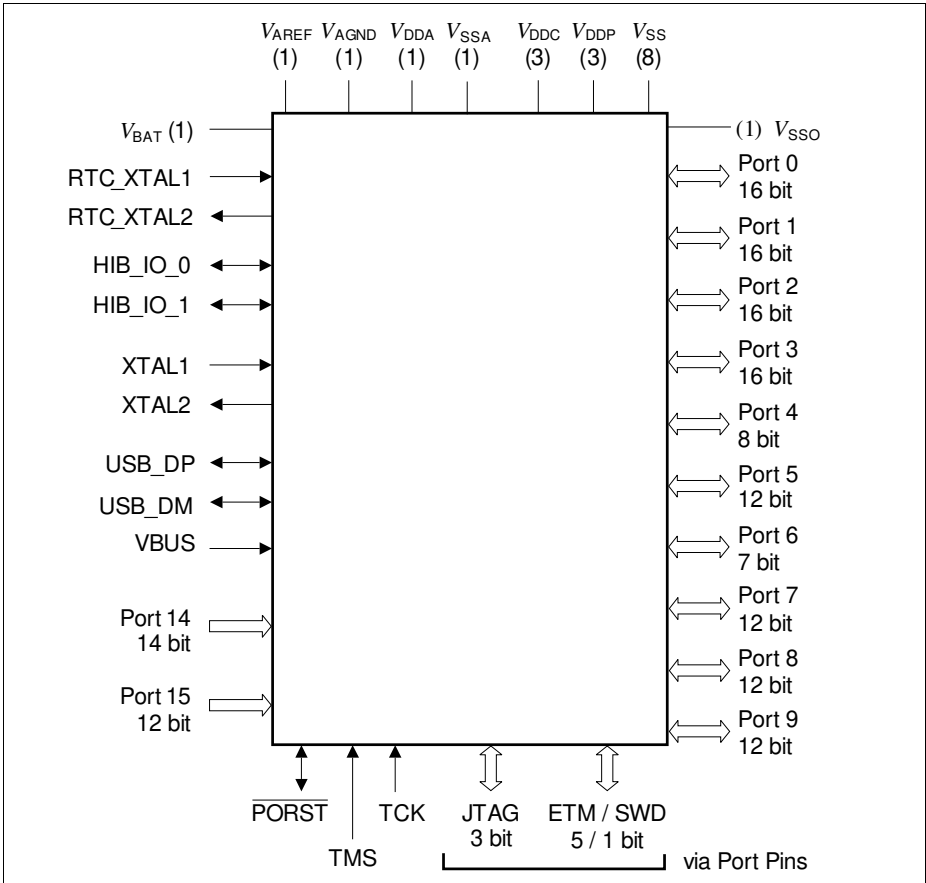


Figure 3 XMC4[78]00 Logic Symbol PG-LFBGA-196

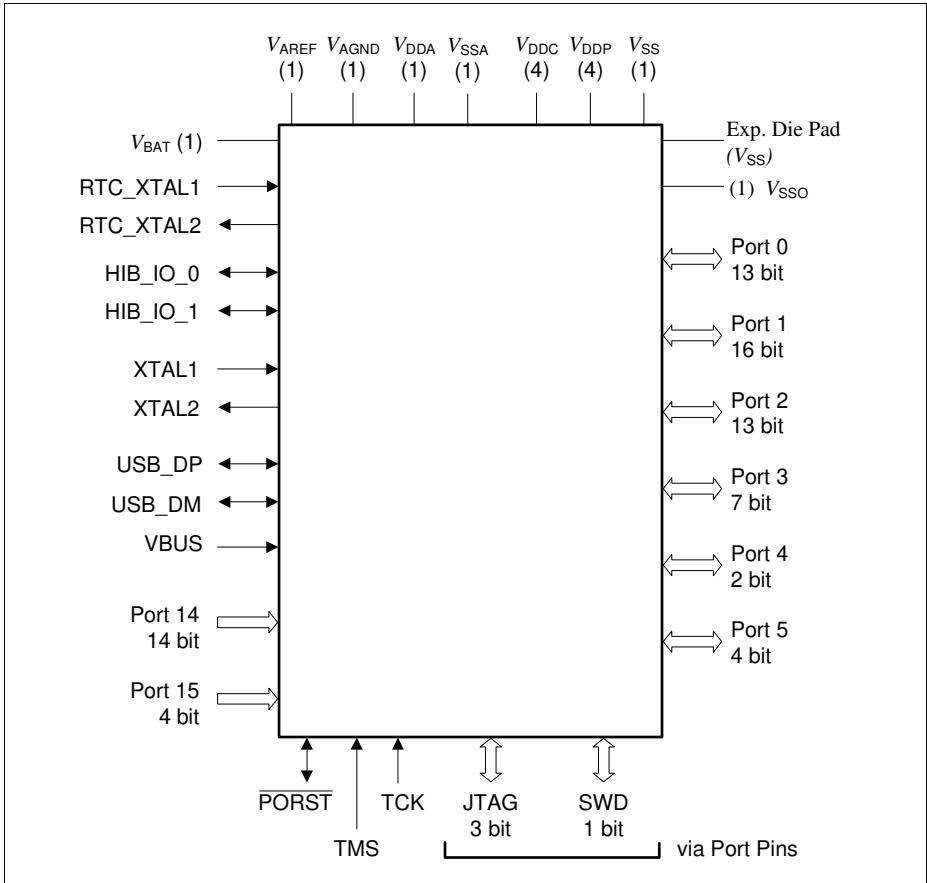


Figure 4 XMC4[78]00 Logic Symbol PG-LQFP-100

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

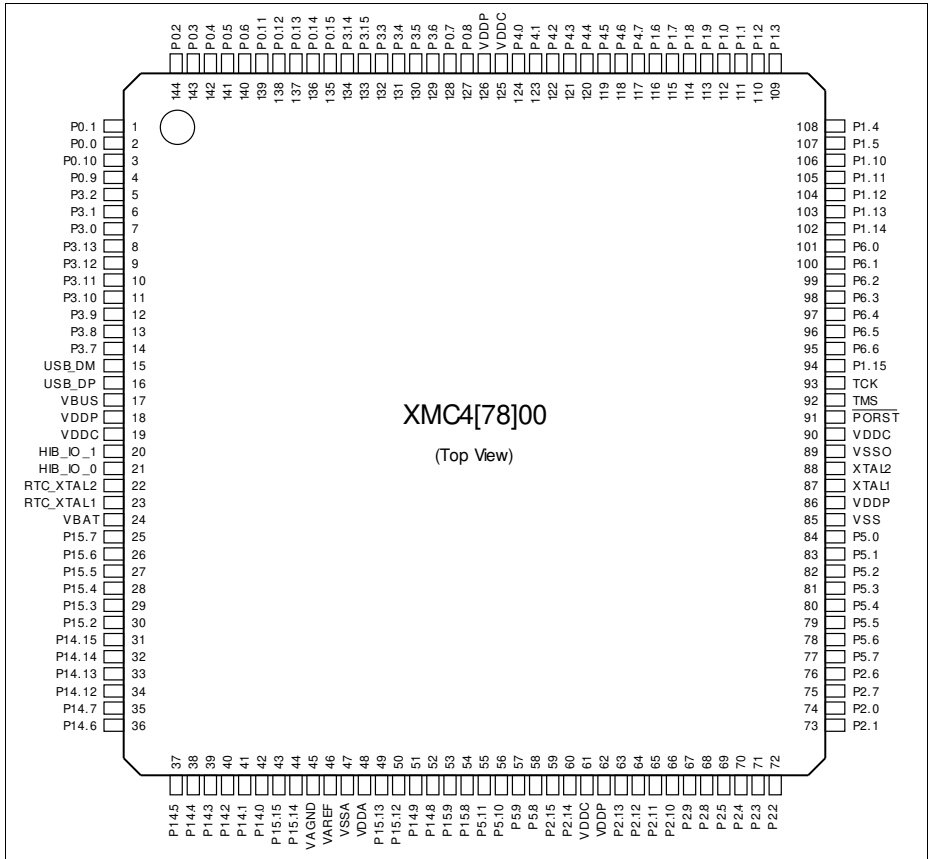


Figure 5 XMC4[78]00 PG-LQFP-144 Pin Configuration (top view)

General Device Information

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	P8.6	P8.8	P8.10	P8.9	P8.11	P8.1	P9.8	P9.7	P9.9	P9.5	P9.4	n.c.	VSS	A
B	n.c.	P8.3	P8.2	P8.7	P8.5	P8.4	P8.0	P9.10	P9.11	n.c.	P9.6	n.c.	VSS	n.c.	B
C	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	n.c.	n.c.	C
D	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	P9.3	P9.2	D
E	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	n.c.	P9.1	E
F	USB_D M	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	P9.0	P7.11	F
G	USB_D P	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	P7.9	P7.10	G
H	RTC_X TAL1	RTC_X TAL2	HIB_I O_1	HIB_I O_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	n.c.	P7.8	H
J	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	$\overline{\text{PORST}}$	P1.15	n.c.	P7.7	J
K	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	n.c.	P7.6	K
L	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	P7.0	P7.5	L
M	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	P7.1	P7.3	M
N	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	P7.2	P7.4	N
P	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	n.c.	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

XMC4[78]00 - (top view)

Figure 6 XMC4[78]00 PG-LFBGA-196 Pin Configuration (top view)

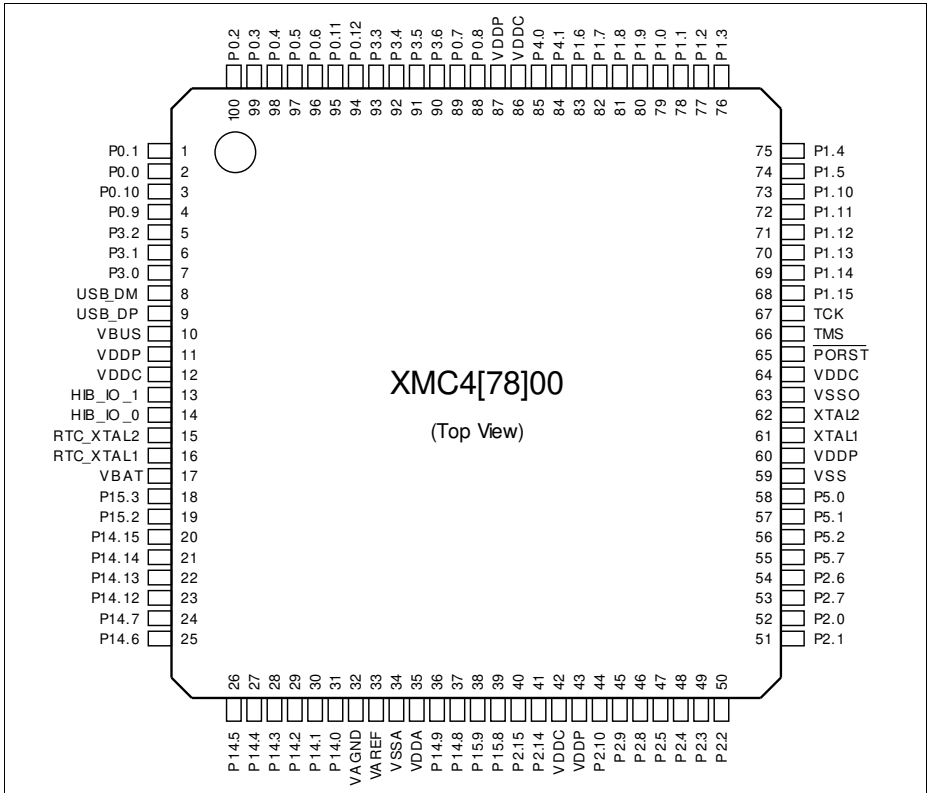


Figure 7 XMC4[78]00 PG-LQFP-100 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 9 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 10 Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.0	E4	2	2	A1+	
P0.1	E3	1	1	A1+	
P0.2	C3	144	100	A2	
P0.3	C4	143	99	A2	
P0.4	D5	142	98	A2	
P0.5	C5	141	97	A2	
P0.6	C6	140	96	A2	
P0.7	D7	128	89	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	C8	127	88	A2	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	F4	4	4	A2	
P0.10	D4	3	3	A1+	

General Device Information
Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.11	G5	139	95	A1+	
P0.12	F5	138	94	A1+	
P0.13	E5	137	-	A1+	
P0.14	G6	136	-	A1+	
P0.15	E6	135	-	A1+	
P1.0	F9	112	79	A1+	
P1.1	G9	111	78	A1+	
P1.2	E11	110	77	A2	
P1.3	E12	109	76	A2	
P1.4	E10	108	75	A1+	
P1.5	F10	107	74	A1+	
P1.6	D9	116	83	A2	
P1.7	D10	115	82	A2	
P1.8	C10	114	81	A2	
P1.9	D11	113	80	A2	
P1.10	F12	106	73	A1+	
P1.11	F11	105	72	A1+	
P1.12	G11	104	71	A2	
P1.13	G12	103	70	A2	
P1.14	G10	102	69	A2	
P1.15	J12	94	68	A2	
P2.0	L11	74	52	A2	
P2.1	M12	73	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	M11	72	50	A2	
P2.3	N11	71	49	A2	
P2.4	N10	70	48	A2	
P2.5	P10	69	47	A2	
P2.6	L9	76	54	A1+	
P2.7	M9	75	53	A1+	
P2.8	N9	68	46	A2	
P2.9	P9	67	45	A2	

General Device Information

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P2.10	N8	66	44	A2	
P2.11	P8	65	-	A2	
P2.12	N7	64	-	A2	
P2.13	P7	63	-	A2	
P2.14	M7	60	41	A2	
P2.15	L6	59	40	A2	
P3.0	E1	7	7	A2	
P3.1	D2	6	6	A2	
P3.2	D3	5	5	A2	
P3.3	H7	132	93	A1+	
P3.4	G7	131	92	A1+	
P3.5	D6	130	91	A2	
P3.6	C7	129	90	A2	
P3.7	G4	14	-	A1+	
P3.8	G3	13	-	A1+	
P3.9	H5	12	-	A1+	
P3.10	H6	11	-	A1+	
P3.11	F3	10	-	A1+	
P3.12	F2	9	-	A2	
P3.13	E2	8	-	A2	
P3.14	F6	134	-	A1+	
P3.15	F7	133	-	A1+	
P4.0	D8	124	85	A2	
P4.1	C9	123	84	A2	
P4.2	G8	122	-	A1+	
P4.3	H8	121	-	A1+	
P4.4	E7	120	-	A1+	
P4.5	F8	119	-	A1+	
P4.6	E8	118	-	A1+	
P4.7	E9	117	-	A1+	
P5.0	K9	84	58	A1+	
P5.1	K8	83	57	A1+	
P5.2	K7	82	56	A1+	

General Device Information

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P5.3	L10	81	-	A2	
P5.4	M10	80	-	A2	
P5.5	L8	79	-	A2	
P5.6	M8	78	-	A2	
P5.7	L7	77	55	A1+	
P5.8	K6	58	-	A2	
P5.9	M6	57	-	A2	
P5.10	K5	56	-	A1+	
P5.11	L5	55	-	A1+	
P6.0	J10	101	-	A2	
P6.1	H9	100	-	A2	
P6.2	K10	99	-	A2	
P6.3	J9	98	-	A1+	
P6.4	H10	97	-	A2	
P6.5	H11	96	-	A2	
P6.6	H12	95	-	A2	
P7.0	L13	-	-	A2	
P7.1	M13	-	-	A2	
P7.2	N13	-	-	A2	
P7.3	M14	-	-	A2	
P7.4	N14	-	-	A1+	
P7.5	L14	-	-	A1+	
P7.6	K14	-	-	A1+	
P7.7	J14	-	-	A1+	
P7.8	H14	-	-	A2	
P7.9	G13	-	-	A1+	
P7.10	G14	-	-	A1+	
P7.11	F14	-	-	A1+	
P8.0	B7	-	-	A2	
P8.1	A7	-	-	A2	
P8.2	B3	-	-	A2	
P8.3	B2	-	-	A2	
P8.4	B6	-	-	A1+	

General Device Information

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P8.5	B5	-	-	A1+	
P8.6	A2	-	-	A1+	
P8.7	B4	-	-	A1+	
P8.8	A3	-	-	A2	
P8.9	A5	-	-	A1+	
P8.10	A4	-	-	A1+	
P8.11	A6	-	-	A1+	
P9.0	F13	-	-	A2	
P9.1	E14	-	-	A2	
P9.2	D14	-	-	A1+	
P9.3	D13	-	-	A2	
P9.4	A12	-	-	A1+	
P9.5	A11	-	-	A1+	
P9.6	B11	-	-	A1+	
P9.7	A9	-	-	A1+	
P9.8	A8	-	-	A1+	
P9.9	A10	-	-	A1+	
P9.10	B8	-	-	A1+	
P9.11	B9	-	-	A1+	
P14.0	N3	42	31	AN/DIG_IN	
P14.1	N2	41	30	AN/DIG_IN	
P14.2	M3	40	29	AN/DIG_IN	
P14.3	L4	39	28	AN/DIG_IN	
P14.4	M1	38	27	AN/DIG_IN	
P14.5	M2	37	26	AN/DIG_IN	
P14.6	L3	36	25	AN/DIG_IN	
P14.7	L2	35	24	AN/DIG_IN	
P14.8	P5	52	37	AN/DAC/DI G_IN	
P14.9	N5	51	36	AN/DAC/DI G_IN	
P14.12	L1	34	23	AN/DIG_IN	
P14.13	K4	33	22	AN/DIG_IN	