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## Features

- 21 dB Small Signal Gain
- 25 dBm P1dB Compression Point
- 38 dBm Output IP3 Linearity
- 17 dB Gain Control with Bias Adjust
- Lead-Free 3 mm 16-lead QFN Package
- 100% RF Testing
- RoHS\* Compliant and 260°C Reflow Compatible

## Description

The XP1042-QT is a packaged driver amplifier that operates over the 12 - 16 GHz frequency band. The device provides 21 dB gain and 38 dBm Output Third Order Intercept Point (OIP3) across the band and is offered in an industry standard, fully molded 3 mm QFN package. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part.

The device is manufactured in 0.5  $\mu\text{m}$  GaAs pHEMT device technology with BCB wafer coating to enhance ruggedness and repeatability of performance.

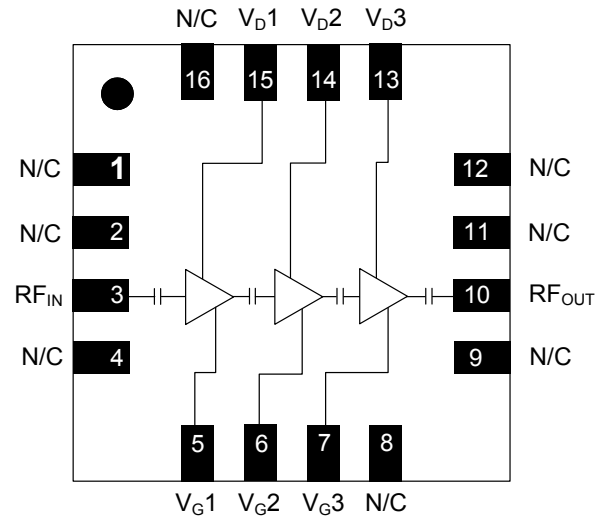
The XP1042-QT is specifically designed for Point to Point radio applications and is well suited for other telecom applications such as SATCOM and VSAT.

## Ordering Information<sup>1</sup>

Part Number	Package
XP1042-QT-0G00	bulk quantity
XP1042-QT-0G0T	tape and reel
XP1042-QT-EV1	evaluation module

1. Reference Application Note M513 for reel size information.

## Functional Schematic



## Pin Configuration

Pin No.	Function	Pin No.	Function
1-2	Not Connected	10	RF Output
3	RF Input	11-12	Not Connected
4	Not Connected	13	Drain 3 Bias
5	Gate 1 Bias	14	Drain 2 Bias
6	Gate 2 Bias	15	Drain 1 Bias
7	Gate 3 Bias	16	Not Connected
8-9	Not Connected	17 <sup>2</sup>	Paddle

2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

\* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

**Electrical Specifications: Freq = 12 - 16 GHz, T<sub>A</sub> = +25°C**

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB	19	21	-
Input Return Loss (S11)	dB	-	12	-
Output Return Loss (S22)	dB	-	10	-
Reverse Isolation (S12)	dB	-	50	-
NF at Max Gain	dB	-	6	8
P1dB	dB	-	25	-
OIP3 at Pout = 8 dBm per Tone	dBm	36	38	-
Drain Bias Voltage (Vd1,2,3)	VDC	-	5	-
Gate Bias Voltage (Vg1,2,3)	VDC	-2	-1	-
Supply Current (Id1)	mA	-	75	125
Supply Current (Id2)	mA	-	75	125
Supply Current (Id3)	mA	-	150	250

**Absolute Maximum Ratings<sup>3,4</sup>**

Parameter	Absolute Max.
Supply Voltage (Vd1,2,3)	+8.0 V
Supply Current (Id1,2,3)	550 mA
Gate Bias Voltage (Vg1,2,3)	-2.4 V
Max Power Dissipation (Pdiss)	2.8 W
RF Input Power	15 dBm
Operating Temperature (Ta)	-55°C to +85°C
Storage Temperature (Tstg)	-65°C to +165°C
Channel Temperature (Tch) <sup>5</sup>	150°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- Operating at nominal conditions with T<sub>J</sub> ≤ +150°C will ensure MTTF > 1 x 10<sup>6</sup> hours.

**Handling Procedures**

Please observe the following precautions to avoid damage:

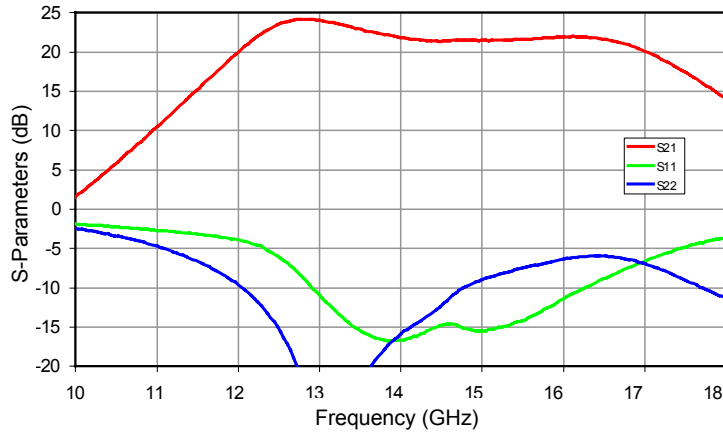
**Static Sensitivity**

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A devices.

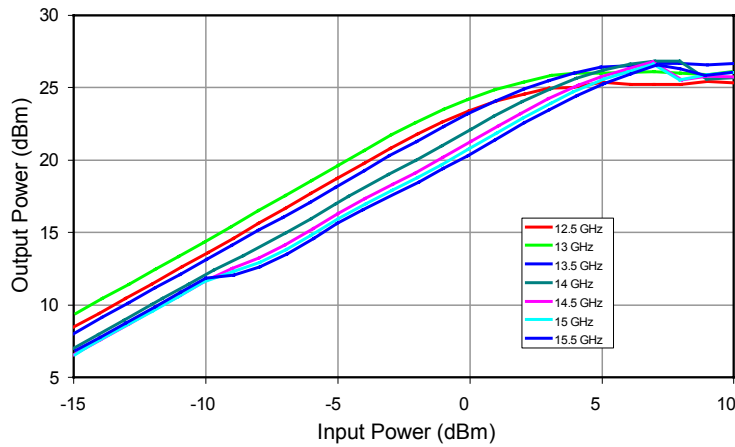


**Typical Performance Curves:  $V_D = 5\text{ V}$ ,  $I_{D1} = 125\text{ mA}$ ,  $I_{D2} = 125\text{ mA}$ ,  $I_{D3} = 250\text{ mA}$**

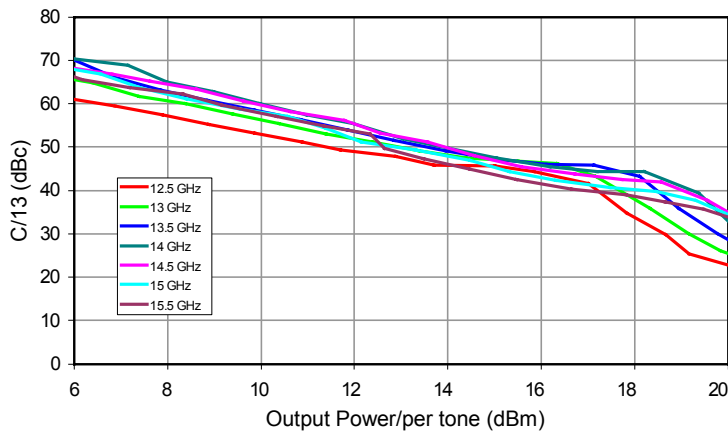
**S-Parameters vs. Frequency**



**Output Power vs. Input Power**



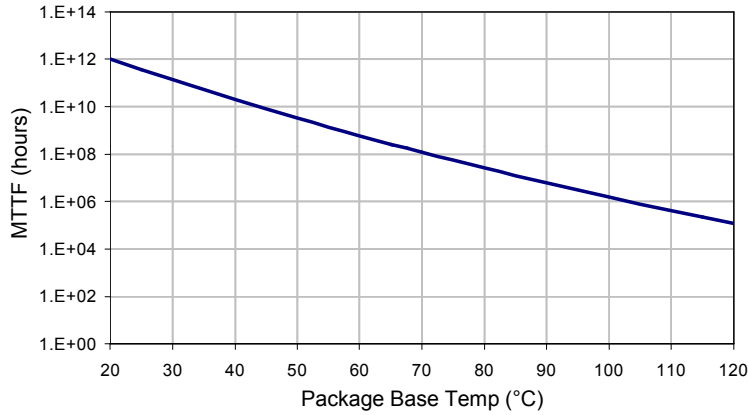
**C/13 vs. Output Power, 100 MHz per tone**



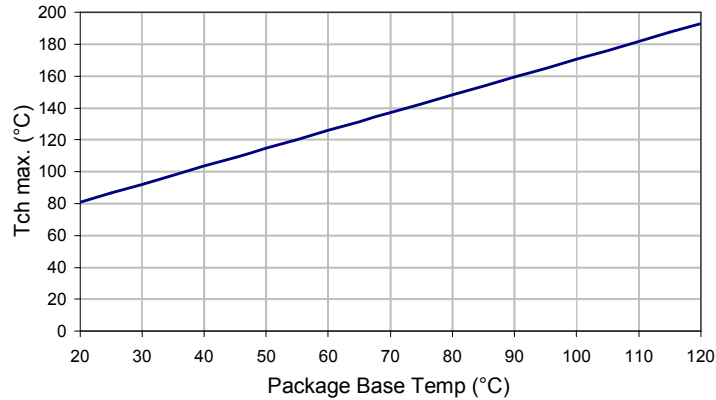
## MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.

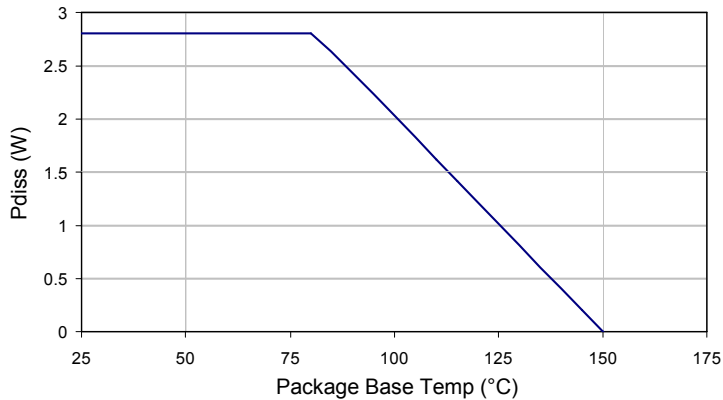
**MTTF Hours vs. Package Base Temperature**  
 $V_{D1,2,3} = 5\text{ V}$ ,  $I_{D1} = 125\text{ mA}$ ,  $I_{D2} = 125\text{ mA}$ ,  $I_{D3} = 250\text{ mA}$



**Tch (max.) vs. Package Base Temperature**  
 $V_{D1,2,3} = 5\text{ V}$ ,  $I_{D1} = 125\text{ mA}$ ,  $I_{D2} = 125\text{ mA}$ ,  $I_{D3} = 250\text{ mA}$



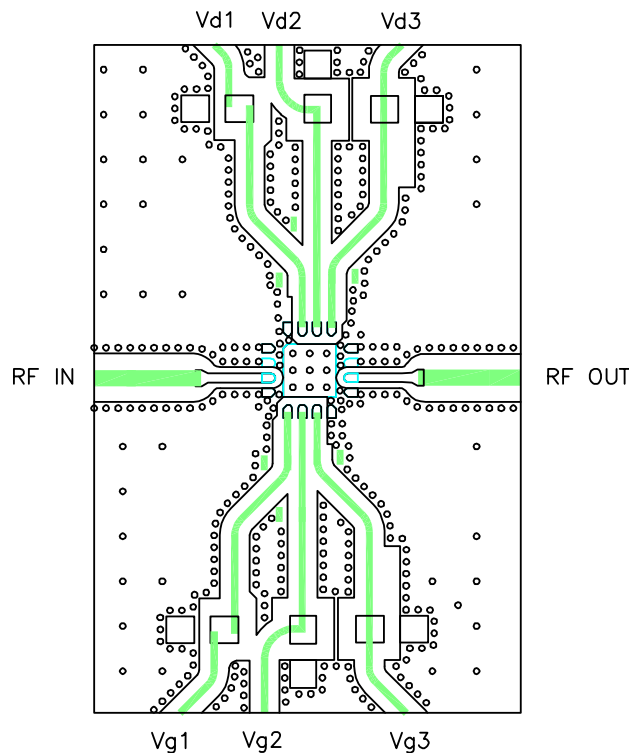
**Operating Power De-rating Curve (continuous)**  
 $V_{D1,2,3} = 5\text{ V}$ ,  $I_{D1} = 125\text{ mA}$ ,  $I_{D2} = 125\text{ mA}$ ,  $I_{D3} = 250\text{ mA}$



**App Note [1] Biasing** - As shown in the Pin Designations table, the device is operated by biasing VD1,2,3 at 5 V with 125, 125, 250 mA respectively. It is recommended to use active bias to keep the currents constant in order to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is  $-1$  V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

**App Note [2] Board Layout** - As shown in the board layout, it is recommended to provide 100 pF decoupling caps as close to the bias pins as possible, with additional 10  $\mu$ F decoupling caps.

## Recommended Layout

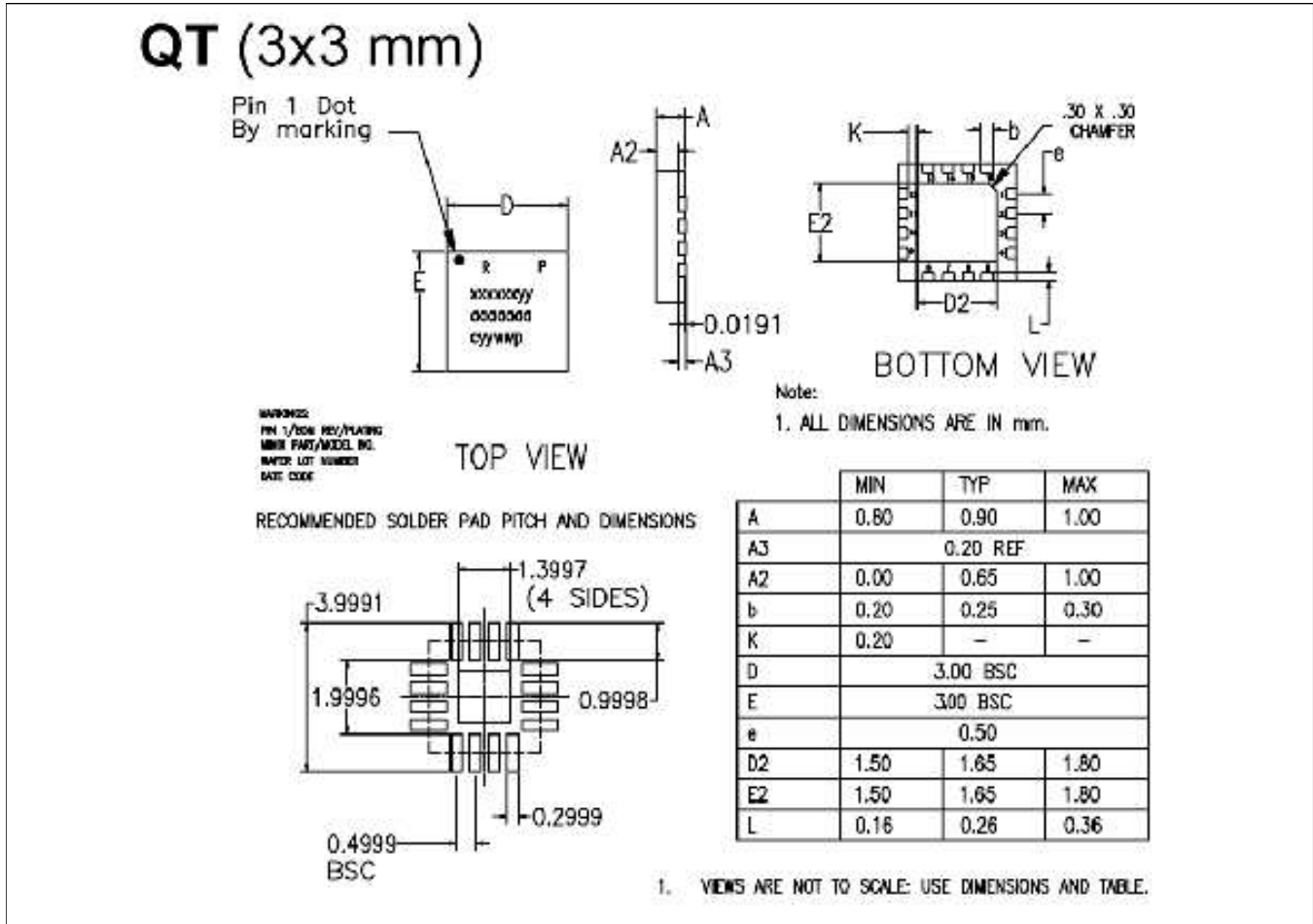


Recommended Caps:

(6x) 100pF, 0402

(6x) 10nF, 0805

Lead-Free 3 mm 16-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.  
Meets JEDEC moisture sensitivity level 3 requirements.  
Plating is 100% matte tin over copper.

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