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GENERAL DESCRIPTION

The XR16C850[1] (850) is a Universal Asynchronous Receiver and Transmitter (UART). This device supports Intel and PC mode data bus interface and is software compatible to industry standard 16C450, 16C550, ST16C580 and ST16C650A UARTs.

The 850 has 128 bytes of TX and RX FIFOs and is capable of operating up to a serial data rate of 2 Mbps. The internal registers include the 16C550 register set plus Exar's enhanced registers for additional features to support today's highly demanding data communication needs. The enhanced features include automatic hardware and software flow control, selectable TX and RX trigger levels, and wireless infrared (IrDA) encoder/decoder.

The XR16C850 is available in the 44 pin PLCC and 48 pin TQFP packages. They both provide the standard Intel Bus mode and PC ISA bus (PC) mode. The Intel Bus mode is compatible with the ST16C450 and ST16C550 while the PC mode allows connection to the PC ISA bus.

NOTE: *1 Covered by U.S. patent #5,649,122 and #5,949,787.*

FEATURES

Added feature in devices with top mark date code of "F2 YYWW" and newer:

- 5 volt tolerant inputs
- 0 ns address hold time (T_{AH})

- 2.97 to 5.5 volt operation
- Pin to pin compatible to ST16C550, ST16C580, ST16C650A and TL16C750
- 128-byte Transmit and Receive FIFOs
- Transmit/Receive FIFO Counters
- Programmable TX/RX FIFO Trigger Levels
- Automatic Hardware/Software Flow Control
- Auto RS-485 half duplex direction support
- Programmable Xon/Xoff characters
- Infrared (IrDA) TX and RX Encoder/Decoder
- Sleep Mode (100 uA stand-by)

APPLICATIONS

- Battery Operated Electronics
- Internet Appliances
- Handheld Terminal
- Personal Digital Assistants
- Cellular Phones DataPort
- Wireless Infrared Data Communications Systems

FIGURE 1. BLOCK DIAGRAM

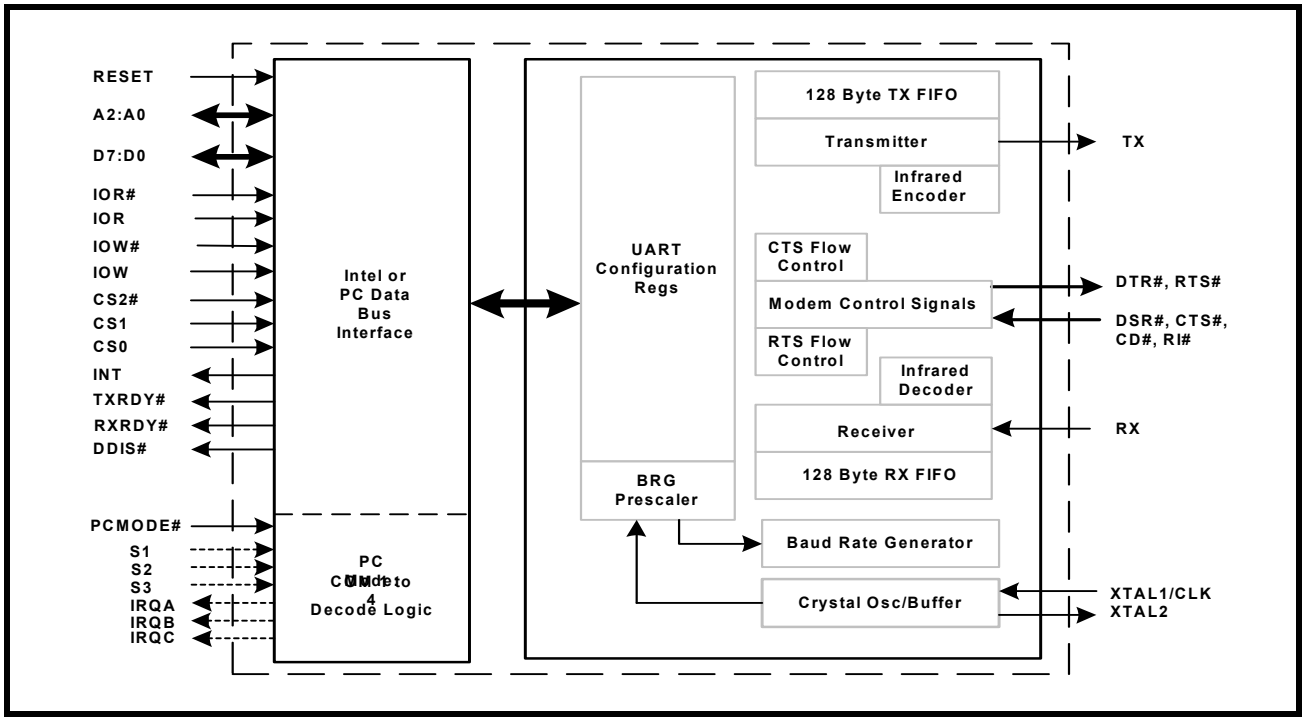
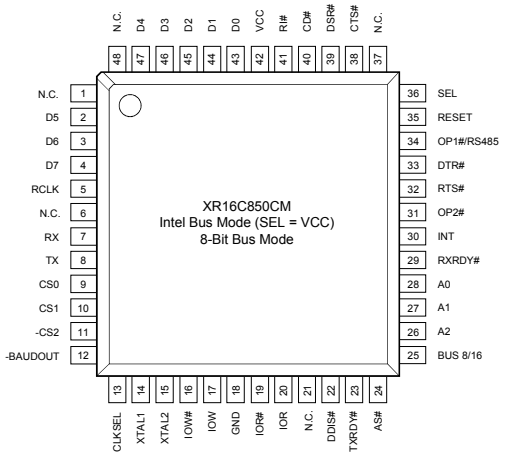
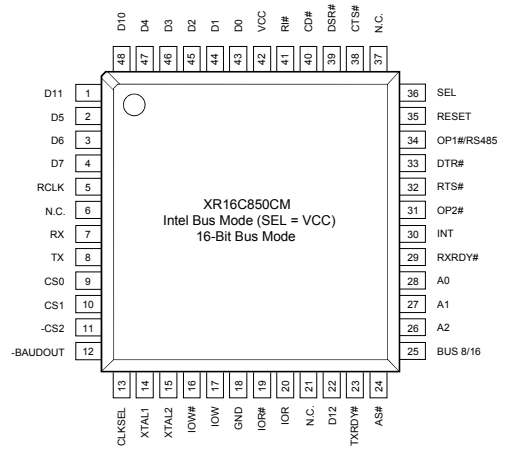
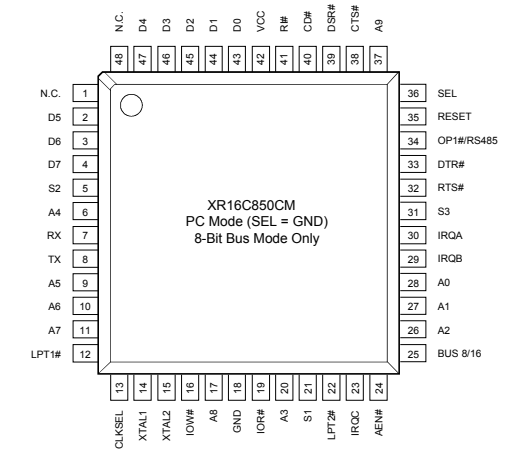


FIGURE 2. PINOUTS IN INTEL BUS MODE AND PC MODE, TQFP AND PLCC PACKAGES

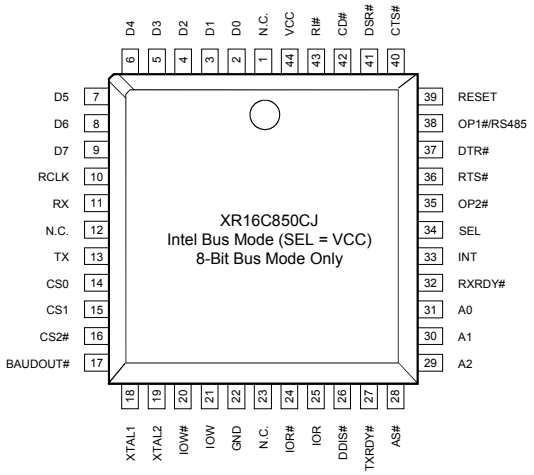
48-TQFP PACKAGE

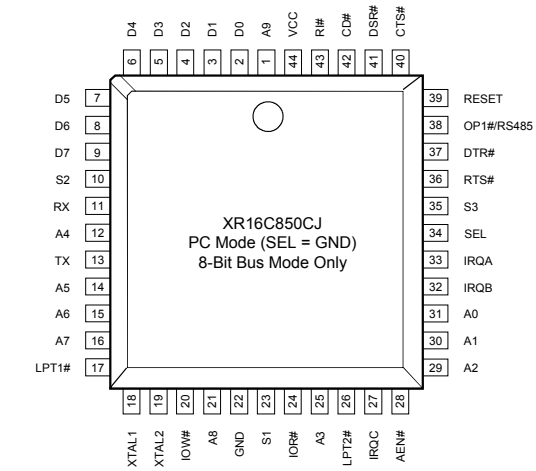






44-PLCC PACKAGE





ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16C850CJ	44-Lead PLCC	0°C to +70°C	Active
XR16C850CM	48-Lead TQFP	0°C to +70°C	Active
XR16C850IJ	44-Lead PLCC	-40°C to +85°C	Active
XR16C850IM	48-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

NOTE: Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
INTEL BUS MODE INTERFACE. THE SEL PIN IS CONNECTED TO VCC.				
A2 A1 A0	29 30 31	26 27 28	I	Address data lines [2:0]. A2:A0 selects internal UART's configuration registers.
D0 D1 D2 D3 D4 D5 D6 D7	2 3 4 5 6 7 8 9	43 44 45 46 47 2 3 4	I/O	Data bus lines [7:0] (bidirectional).
IOR#	24	19	I	Input/Output Read (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], places it on the data bus to allow the host processor to read it on the leading edge. Either an active IOR# or IOR is required to transfer data from 850 to CPU during a read operation. If not used, connect this pin to VCC. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
IOR	25	20	I	Input/Output Read (active high). Same as IOR# but active high. Either an active IOR# or IOR is required to transfer data from 850 to CPU during a read operation. If not used, connect this pin to GND. During PC Mode, this pin becomes A3. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
IOW#	20	16	I	Input/Output Write (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0]. Either an active IOW# or IOW is required to transfer data from 850 to the Intel type CPU during a write operation. If not used, connect this pin to VCC. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
IOW	21	17	I	Input/Output Write (active high). The rising edge instigates the internal write cycle and the falling edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0]. Either an active IOW# or IOW is required to transfer data from 850 to the Intel type CPU during a write operation. During PC Mode, this pin becomes A8. If not used, connect this pin to GND. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
CS0	14	9	I	Chip Select 0 input (active high). This input selects the XR16C850 device. If CS1 or CS2# is used as the chip select then this pin must be connected to VCC. During PC Mode, this pin becomes A5. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
CS1	15	10	I	Chip Select 1 input (active high). This input selects the XR16C850 device. If CS0 or CS2# is used as the chip select then this pin must be connected to VCC. During PC Mode, this pin becomes A6. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
CS2#	16	11	I	Chip Select 2 input (active low). This input selects the XR16C850 device. If CS0 or CS1 is used as the chip select then this pin must be connected to GND. During PC Mode, this pin becomes A7. Caution: **SEE"FACTORY TEST MODE" ON PAGE 7.**
INT	33	30	O	Interrupt Output. This output becomes active whenever the transmitter, receiver, line and/or modem status register has an active condition and is enabled by IER. See interrupt section for more details. During PC mode, this pin becomes IRQA.
RXRDY#	32	29	O	Receive Ready (active low). A logic 0 indicates receive data ready status, i.e. the RHR is full or the FIFO has one or more RX characters available for unloading. For details, see **Table 2**. During PC Mode, this pin becomes IRQB.
TXRDY#	27	23	O	Transmit Ready (active low). Buffer ready status is indicated by a logic 0, i.e. at least one location is empty and available in the FIFO or THR. For details, see **Table 2**. During PC Mode, this pin becomes IRQC.
AS#	28	24	I	Address Strobe input (active low). In the Intel bus mode, the leading-edge transition of AS# latches the chip selects (CS0, CS1, CS2#) and the address lines A0, A1 and A2. This input is used when the address lines are not stable for the duration of a read or write operation. In devices with top mark date code of "F2 YYWW" and newer, the address bus is latched even if this input is not used. These devices feature a '0 ns' address hold time. See "AC Electrical Characteristics" . If not required, this input can be permanently tied to GND. During PC Mode, this pin becomes AEN#.
D10 D11 D12	- - -	48 1 22	O	High order data bus. When BUS8/16 is selected as 16 bit data bus mode (BUS8/16 is grounded), RX data errors (break, parity, framing) can be read via these pins. D10 = Parity, D11 = Framing, and D12 = Break. When BUS8/16 is selected as 8 bit data bus mode (BUS8/16 is at VCC), D10 and D11 are inactive and D12 becomes DDIS#. During PC Mode, D10 and D11 are inactive and D12 becomes LPT2#.
BUS8/16	-	25	I	8 or 16 Bit Bus select. For normal 8 bit operation, this pin should be connected to VCC or left open. To select 16 bit bus mode, this pin should be connected to GND. When 16 bit bus mode is enabled, DDIS# becomes D12. 16 bit bus mode is not available for PC Mode. Only RX data error will be provided during this operation. This pin has an internal pull-up resistor.
CLKSEL	-	13	I	Clock Select. The div-by-1 or div-by-4 pre-scaleable clock is selected by this pin. The div-by-1 clock is selected when CLKSEL is connected to VCC or the div-by-4 is selected when CLKSEL is connected to GND. MCR bit-7 can override the state of this pin following reset or initialization (see MCR bit-7). This pin is not available on 40 and 44 pin packages which provide MCR bit-7 selection only. This pin has an internal pull-up resistor.
RCLK	10	5	I	This input is used as external 16X clock input to the receiver section. If not used, connect the -BAUDOUT pin to this input externally. During PC Mode, this pin becomes S2.

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
BAUD-OUT#	17	12	O	Baud Rate Generator Output (active low). This pin provides the 16X clock of the selected data rate from the baud rate generator. The RCLK pin must be connected externally to BAUDOUT# when the receiver is operating at the same data rate. When the PC mode is selected, the baud rate generator clock output is internally connected to the RCLK input. This pin then functions as the printer port decode logic output (LPT1#), see Table 3.
DDIS#	26	22	O	Drive Disable Output. This pin goes to a logic 0 whenever the host CPU is reading data from the 850. It can control the direction of a data bus transceiver between the CPU and 850 or other logic functions. If 16 bit bus mode is selected, this pin becomes D12. During PC Mode, this pin becomes LPT2#.
OP2#	35	31	O	Output Port 2. General purpose output. During PC Mode, this pin becomes S3.
PC MODE INTERFACE SIGNALS. CONNECT SEL PIN TO GND TO SELECT PC MODE.				
A3	25	20	I	Address-3 Select Bit. This pin is used as the 4th address line to decode the COM1-4 and LPT ports. See Table 1 for details. During Intel Bus Mode, this pin becomes IOR.
A4	12	6	I	Address-4 Select Bit. This pin is used as the 5th address line to decode the COM1-4 and LPT ports. This pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40-Pin PDIP package which operates in the Intel Bus Mode Only. See Table 1 for details. During Intel Bus Mode, this pin is inactive.
A5 A6 A7 A8	14 15 16 21	9 10 11 17	I	Address-5 thru Address-8 Select Bit. These pins are used as the 6th thru 9th address lines to decode the COM1-4 and LPT ports. See Table 1 for details. During Intel Bus Mode, A5 becomes CS0, A6 becomes CS1, A7 becomes CS2#, and A8 becomes IOW.
A9	1	37	I	Address-9 Select Bit. This pin is used as the 10th address line to decode the COM1-4 and LPT ports. This pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40-Pin PDIP package which operates in the Intel Bus Mode Only. See Table 1 for details. During Intel Bus Mode, this pin is inactive.
AEN#	28	24	I	Address Enable input (active low). When AEN# transitions to logic 0, it decodes and validates COM 1-4 ports address per S1, S2 and S3 inputs. During Intel Bus Mode, this pin becomes AS#.
S1 S2 S3	23 10 35	21 5 31	I	Select 1 to 3. These are the standard PC COM 1-4 ports and IRQ selection inputs. See Table 1 and Table 3 for details. The S1 pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40 pin PDIP packages which operates in the Intel Bus Mode Only. During Intel Bus Mode, S1 is inactive, S2 becomes RCLK, and S3 becomes OP2#.
IRQA IRQB IRQC	33 32 27	30 29 23	O	Interrupt Request A, B and C Outputs (active high, three-state). These are the interrupt outputs associated with COM 1-4 to be connected to the host data bus. See interrupt section for details. The Interrupt Requests A, B or C functions as IRQx to the PC bus. IRQx is enabled by setting MCR bit-3 to logic 1 and the desired interrupt(s) in the interrupt enable register (IER). During Intel Bus Mode, IRQA becomes INT, IRQB becomes RXRDY#, and IRQC becomes TXRDY#.
LPT1#	17	12	O	Line Printer Port-1 Decode Logic Output (active low). This pin functions as the PC standard LPT-1 printer port address decode logic output, see Table 1. The baud rate generator clock output, BAUDOUT#, is internally connected to the RCLK input in the PC mode. During Intel Bus Mode, LPT1# becomes BAUDOUT#.

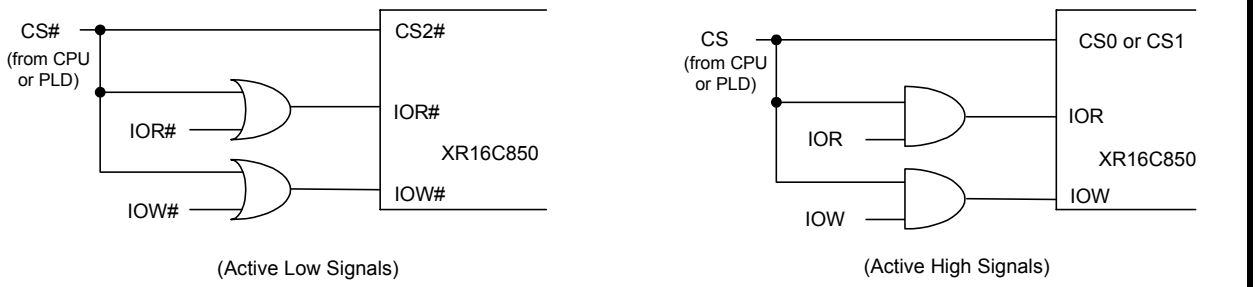
NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
LPT2#	26	22	O	Line Printer Port-2 Decode Logic Output (active low) - This pin functions as the PC standard LPT-2 printer port address decode logic output, see **Table 1**. During Intel Bus Mode, LPT2# becomes DDIS#/D12.
MODEM OR SERIAL I/O INTERFACE				
TX	13	8	O	Transmit Data or wireless infrared transmit data. This output is active low in normal standard serial interface operation (RS-232, RS-422 or RS-485) and active high in the infrared mode. Infrared mode can be enabled by connecting pin ENIR to VCC or through software selection after power up.
RX	11	7	I	Receive Data or wireless infrared receive data. Normal received data input idles at logic 1 condition and logic 0 in the infrared mode. The wireless infrared pulses are applied to the decoder. This input must be connected to its idle logic state in either normal, logic 1, or infrared mode, logic 0, else the receiver may report “receive break” and/or “error” condition(s).
RTS#	36	32	O	Request to Send or general purpose output (active low). This port may be used for automatic hardware flow control, see EFR bit-6, MCR bit-1, FCTR bits 0-1 and IER bit-6. RTS# output must be asserted before auto RTS flow control can start. If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, leave it unconnected.
CTS#	40	38	I	Clear to Send or general purpose input (active low). If used for automatic hardware flow control, data transmission will be stopped when this pin is de-asserted and will resume when this pin is asserted again. See EFR bit-7, MCR bit-2 and IER bit-7. If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
DTR#	37	33	O	Data Terminal Ready or general purpose output (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, leave it unconnected.
DSR#	41	39	I	Data Set Ready input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
CD#	42	40	I	Carrier Detect input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
RI#	43	41	I	Ring Indicator input or general purpose input (active low). If this pin is not needed for modem communication, then it can be used as a general I/O. If it is not used, connect it to VCC.
ANCILLARY SIGNALS				
XTAL1	18	14	I	Crystal or external clock input. See **Figure 7** for typical oscillator connections. Caution: this input is not 5V tolerant.
XTAL2	19	15	O	Crystal or buffered clock output. See **Figure 7** for typical oscillator connections.
SEL	34	36	I	PC Mode Select (active low). When this input is at logic 0, it enables the on-board chip select decode function according to PC ISA bus COM[4:1] and IRQ[4,3] port definitions. See **Table 3** for details. This pin has an internal 100kΩ pull-up resistor. This pin is not available on the 40 pin PDIP packages which operate in the Intel Bus Mode only.

NAME	44-PIN PLCC	48-PIN TQFP	TYPE	DESCRIPTION
OP1#/ RS485	38	34	O	Output Port 1 (General purpose output) or RS-485 Direction Control Signal. RS-485 direction control can be selected when FCTR Bit-3 is set to “1”. During data transmit cycle, RS485 pin is low. An inverter is usually required before connecting to RS-485 Transceiver.
RESET	39	35	I	Reset Input (active high). When it is asserted, the UART configuration registers are reset to default values, see **Table 15**.
VCC	44	42	Pwr	Power supply input. All inputs are 5V tolerant except for XTAL1 for devices with top mark date code of "F2 YYWW" and newer. Devices with top mark date code of "EC YYWW" and older do not have 5V tolerant inputs.
GND	22	18	Pwr	Power supply common ground.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

Factory Test Mode

For devices with top mark date code of "EC YYWW" and older devices, please note that if IOR# (or IOR) and IOW# (or IOW) are both asserted simultaneously, the 850 will enter a Factory Test Mode. The most noticeable Factory Test Mode symptom is the continuous transmission of the same character on the TX pin. This usually happens during power-up or when another device in the design requires both signals to be asserted simultaneously (like an SDRAM). A solution to this would be to OR (AND if using active-high signals) the chip selects with the read and write signals to the XR16C850 as shown below:



For devices with top mark date code of "F2 YYWW" and higher devices, the solution for the Factory Test Mode given in the figure above has been incorporated into the UART. It will only enter Factory Test Mode when all three signals (chip select, read and write) are asserted simultaneously.

1.0 PRODUCT DESCRIPTION

The XR16C850 (850) provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The XR16C850 represents such an integration with greatly enhanced features. The 850 is fabricated using an advanced CMOS process.

Enhanced Features

The 850 is an upward solution that provides 128 bytes of transmit and receive FIFO memory, instead of 32 bytes provided in the 16C650A, 16 bytes in the 16C550, or none in the 16C450. The 850 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 850 by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 128 byte FIFO in the 850, the data buffer will not require unloading/loading for 12.2 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO trigger level interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 850 provides a RS-485 half-duplex direction control signal, pin OP1#/RS485 to select the external transceiver direction. It automatically changes the state of the output pin for receive state after the last stop-bit of the last character has been shifted out of the TX shift register. Afterward, upon loading a TX data byte, it changes state of the output pin back for transmit state. The RS-485 direction control pin is not activated after reset. To activate the direction control function, the user has to set EFR Bit-4, and FCTR Bit-3 to “1”. This pin (OP1#/RS485) is high for receive state, low for transmit state.

Data Bus Interface

Two data bus interfaces are available to the user. The PC mode allows direct interconnect to the PC ISA bus while the Intel Bus Mode operates similar to the standard CPU interface available on the 16C450/550/650A. When the PC mode is selected, the external logic circuitry required for PC COM port address decode and chip select is eliminated. These functions are provided internally in the 850.

Data Rate

The 850 is capable of operation up to 1.5 Mbps with a 24 MHz crystal or external clock input with a 16X sampling clock. However, it is possible to operate up to 2.25 Mbps with a 36 MHz external clock for devices with top mark date code of "F2 YYWW" and newer, and up to 2 Mbps with a 33 MHz external clock for devices with top mark date code of "EC YYWW" and older. With a crystal of 14.7456 MHz and through a software option, the user can select data rates up to 921.6 Kbps.

The rich feature set of the 850 is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. In addition, there is a PC Mode that has two additional three state interrupt lines and one selectable open source interrupt output. The open source interrupt scheme allows multiple interrupts to be combined in a “WIRE-OR” operation, thus reducing the number of interrupt lines in larger systems. Following a power on reset or an external reset, the 850 is software compatible with previous generation of UARTs, 16C450 and 16C550 and 16C650A.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Host Data Bus Interface

The host interface is 8 data bits wide with 3 address lines and control signals to execute bus read and write transactions. The 850 supports 2 types of host interfaces: Intel and PC mode. The Intel bus interface is selected by connecting SEL to logic 1. When the SEL pin is set to a logic 1, the 850 interface is the same as industry standard 16C550. The Intel bus interconnections are shown in **Figure 3**. The special PC mode is selected when SEL is connected to logic 0. The PC mode interconnections are shown in **Figure 4**.

FIGURE 3. XR16C850 INTEL BUS INTERCONNECTIONS

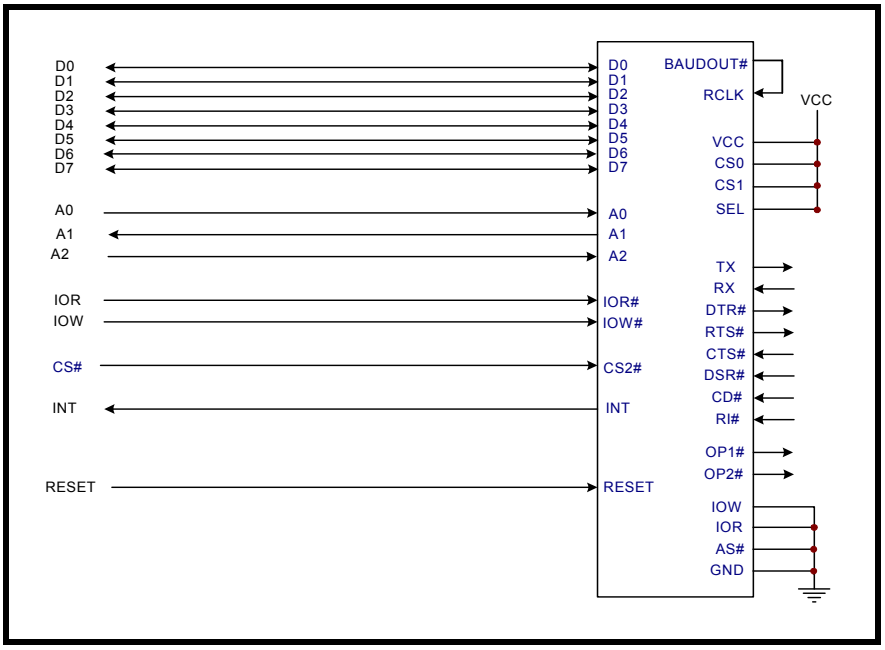
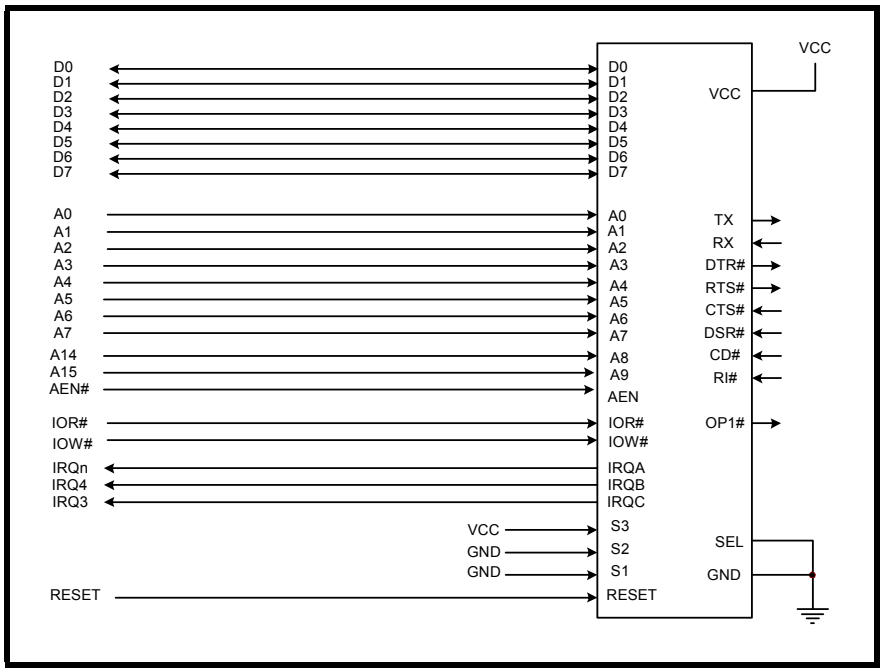


FIGURE 4. XR16C850 PC MODE INTERCONNECTIONS



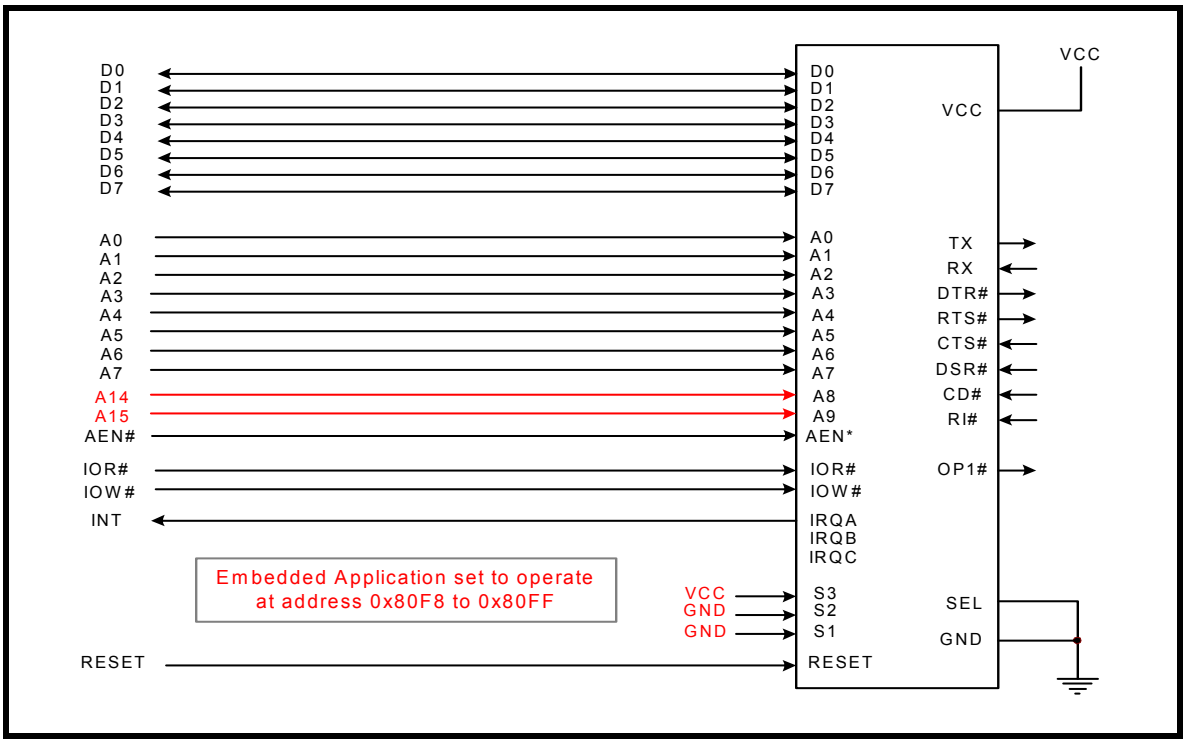
2.2 PC MODE

The PC mode interface includes an on-chip address decoder and interrupt selection function for the standard PC COM 1-4 ports addresses. The selection is made through three input signals: S1, S2 and S3. The selection summary is shown in **Table 1**. Although the on-chip address decoder was designed for PC applications ranging from 0x278 to 0x3FF, it can fit into an embedded applications by offsetting the address lines to the 850. An example is shown in **Figure 5** where the UART is operating from 0x80F8 to 0x80FF address space. Operating in the PC mode eliminates external address decode components.

TABLE 1: PC MODE INTERFACE ON-CHIP ADDRESS DECODER AND INTERRUPT SELECTION.

SEL# INPUT	S3, S2, S1 INPUTS	A3-A9 ADDRESS LINES TO ON-CHIP DECODER	COM/LPT PORT SELECTION	IRQ OUTPUT SELECTION
0	0 0 0	0x3F8 - 0x3FF	COM-1	IRQB (for PC's IRQ4)
0	0 0 1	0x2F8 - 0x2FF	COM-2	IRQC (for PC's IRQ3)
0	0 1 0	0x3E8 - 0x3EF	COM-3	IRQB (for PC's IRQ4)
0	0 0 0	0x3F8 - 0x3FF	COM-4	IRQB (for PC's IRQ4)
0	1 0 0	0x2F8 - 0x2FF	COM-1	IRQA (for PC's IRQn
0	1 0 1	0x3E8 - 0x3EF	COM-2	IRQA (for PC's IRQn)
0	1 1 0	0x2E8 - 0x2EF	COM-3	IRQA (for PC's IRQn)
0	1 1 1	0x3F8 - 0x3FF	COM-4	IRQA (for PC's IRQn)
0	X X X	0x278 - 0x27F	LPT-2	N/A
0	X X X	0x378 - 0x37F	LPT-1	N/A

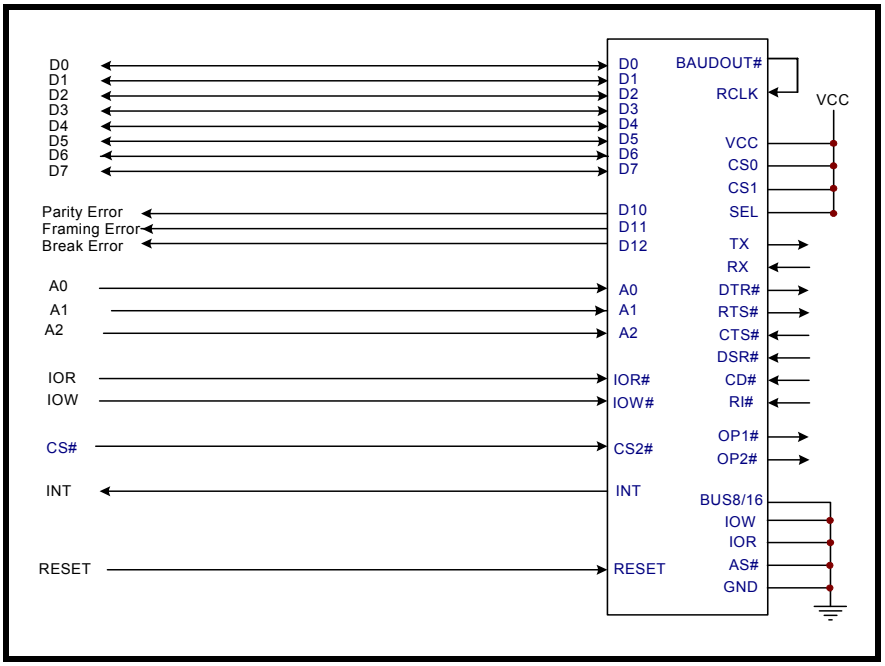
FIGURE 5. PC MODE INTERFACE IN AN EMBEDDED APPLICATION.



2.3 16-Bit Bus Interface

The 16-bit bus interface is only available on the 48 pin package. The 16-bit bus mode is enabled when the BUS8/16 pin is connected to GND. In this mode, the RX data errors can be read via the higher order data bus pins D10-D12. See Figure 6.

FIGURE 6. XR16C850 16-BIT BUS INTERFACE



2.4 5-Volt Tolerant Inputs

For devices that have top mark date code "F2 YYWW" and newer, the 850 can accept a voltage of up to 5.5V on any of its inputs (except XTAL1) when operating from 2.97V to 5.5V. XTAL1 is not 5 volt tolerant. Devices that have top mark date code "EC YYWW" and older do not have 5V tolerant inputs.

2.5 Device Reset

The RESET input resets the internal registers and the serial interface outputsto their default state (see Table 15). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.6 Device Identification and Revision

The XR16C850 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x10 for the XR16C850 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.7 Internal Registers

The 850 has a set of enhanced registers for controlling, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scractchpad register (SPR).

Beyond the general 16C550 features and capabilities, the 850 offers enhanced feature registers (EMSR, TRG, FC, FCTR, EFR, Xon/Xoff 1, Xon/Xoff 2) that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, automatic RS-485 half-duplex direction output enable/disable, FIFO trigger level control, and FIFO level counters. All the register functions are discussed in full detail later in **"Section 3.0, UART INTERNAL REGISTERS" on page 25**.

2.8 DMA Mode

The DMA Mode (a legacy term) in this document does not mean "Direct Memory Access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A/B and TXRDY# A/B output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 850 activates the interrupt output pin for each data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the 850 sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior.

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY# A/B	0 = 1 byte. 1 = no data.	0 = at least 1 byte in FIFO 1 = FIFO empty.	1 to 0 transition when FIFO reaches the trigger level, or timeout occurs. 0 to 1 transition when FIFO empties.
TXRDY# A/B	0 = THR empty. 1 = byte in THR.	0 = FIFO empty. 1 = at least 1 byte in FIFO.	0 = FIFO has at least 1 empty location. 1 = FIFO is full.

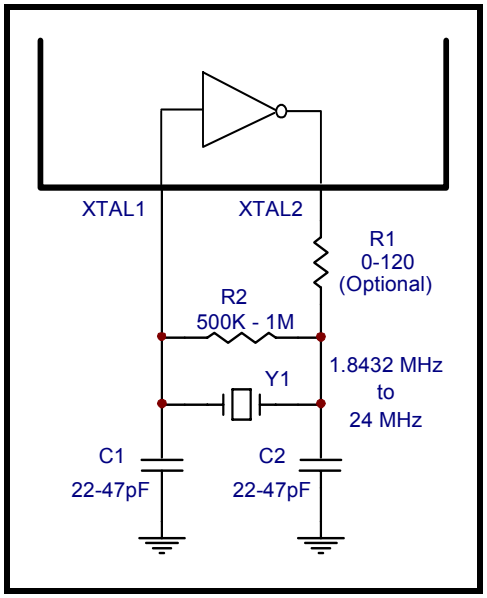
2.9 Interrupts

The output function of interrupt outputs change according to the operating bus type. During the Intel Bus Mode, the INT output will always be active high and MCR bit-3 will have no effect on the INT output pin. In the PC Mode, the IRQ outputs are in three-state mode unless MCR bit-3 and S3 are both a logic 1. **Table 3** summarizes its behavior in Intel and PC mode of operation.

TABLE 3: INTERRUPT OUTPUT FUNCTIONS

BUS MODE	MCR BIT-3	S3 (PC MODE ONLY)	INTERRUPT OUTPUT (INT OR IRQ)
Intel	X	X	Active High
PC	0	0	Three-State
	0	1	Three-State
	1	0	Three-State
	1	1	Active High

FIGURE 7. TYPICAL OSCILLATOR CONNECTIONS



2.10 Crystal Oscillator or External Clock

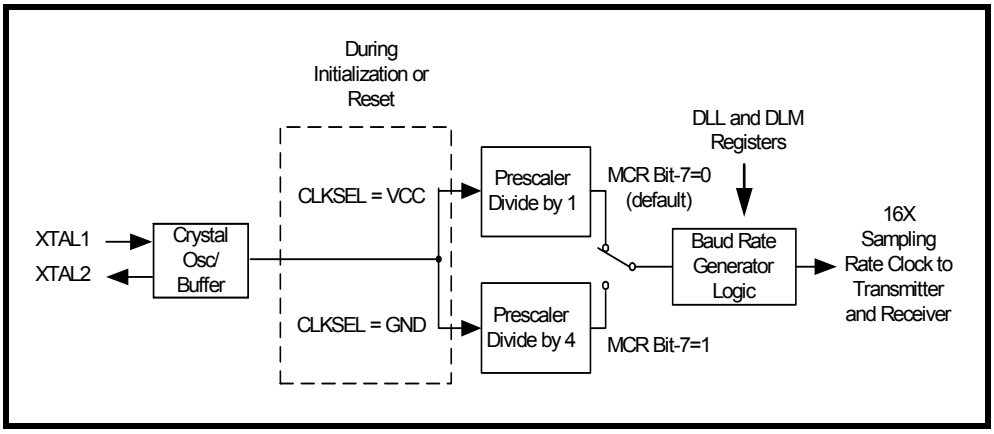
The 850 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see **"Section 2.11, Programmable Baud Rate Generator" on page 14**. To use the same clock for the receiver as used with the transmiter of the UART in the Intel bus mode, the BAUDCLK pin must be connected to the RCLK pin external to the UART.

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see **Figure 7**). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typically, the oscillator connections are shown in **Figure 7**. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.11 Programmable Baud Rate Generator

The UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up or a reset. Therefore, the BRG must be programmed during initialization to the operating data rate.

FIGURE 8. BAUD RATE GENERATOR



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 4 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 4: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

2.12 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 128 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

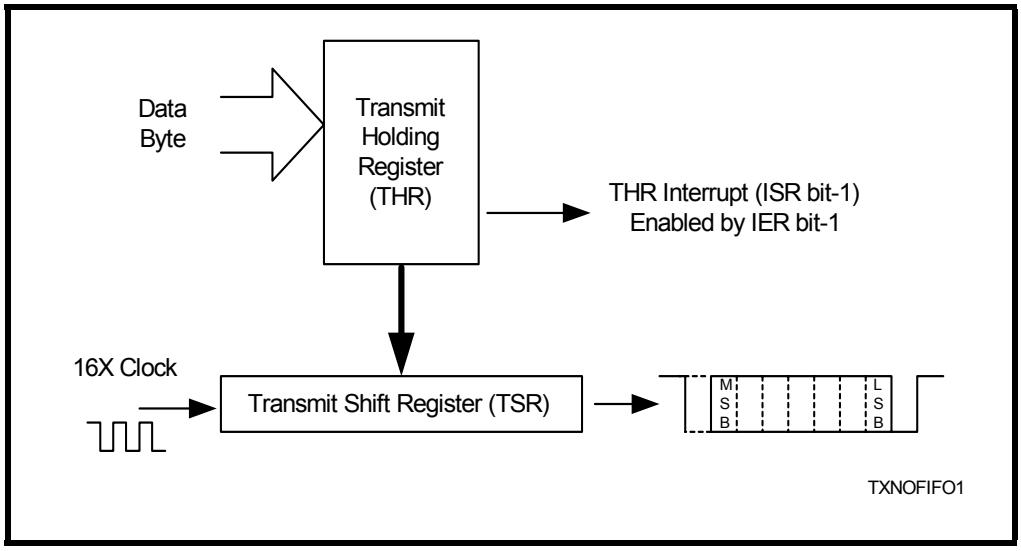
2.12.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 128 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.12.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

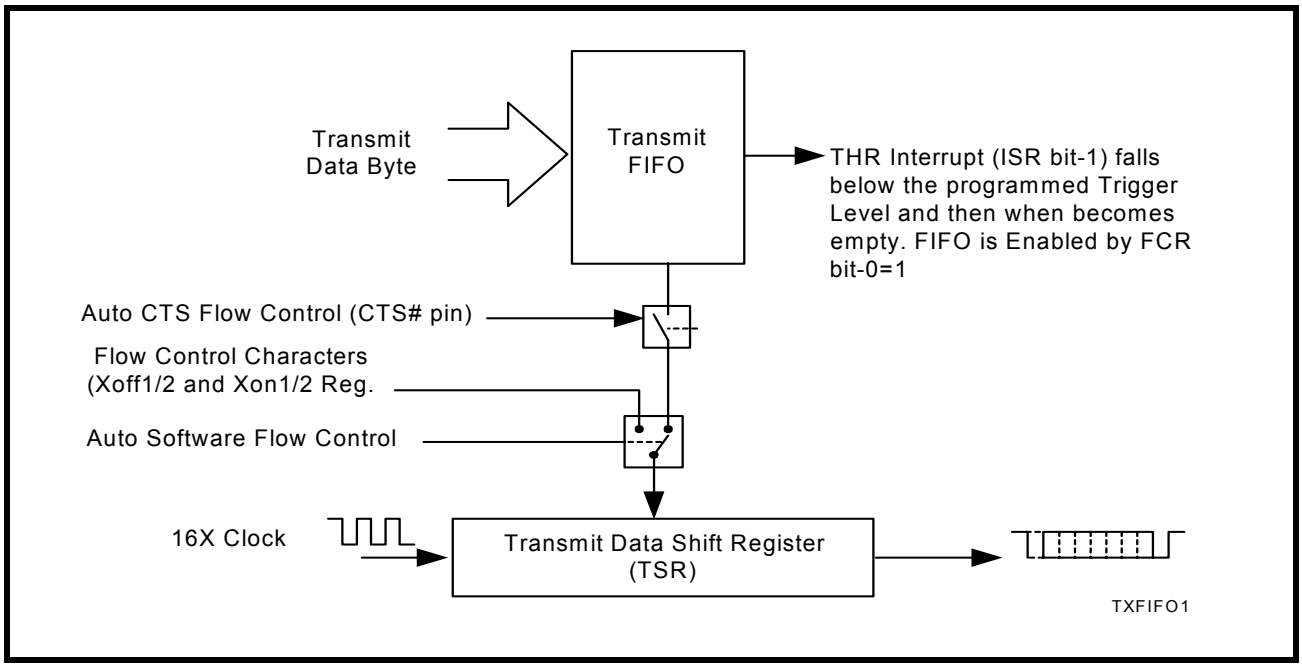
FIGURE 9. TRANSMITTER OPERATION IN NON-FIFO MODE



2.12.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 128 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 10. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.13 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 128 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.13.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 128 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 11. RECEIVER OPERATION IN NON-FIFO MODE

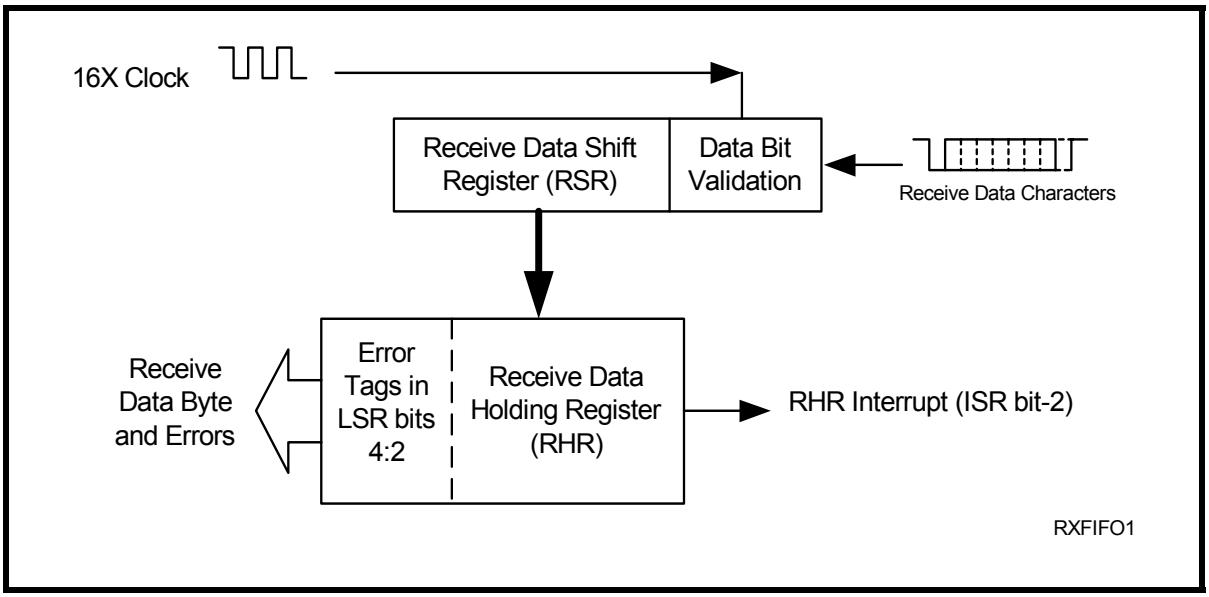
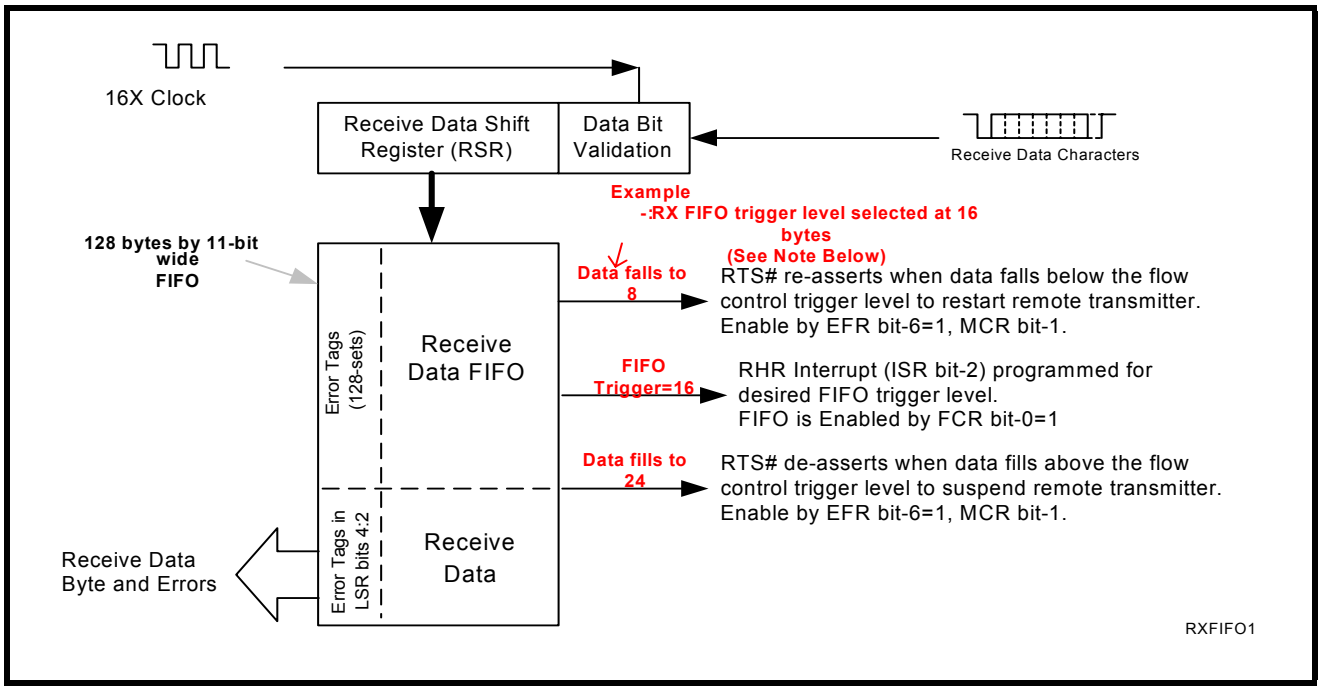


FIGURE 12. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: *Table-B selected as Trigger Table for* **Figure 12** *(Table 10).*

2.14 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 13**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).
- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.15 Auto RTS Hysteresis

The 850 has a new feature that provides flow control trigger hysteresis while it maintains compatibility to 16C650A and 16C550. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS# pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the upper limit of the hysteresis level. The RTS# pin will return to a logic 0 after the RX FIFO is unloaded to the lower limit of the hysteresis level. Under the above described conditions, the 850 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted to a logic 0 (RTS On). For complete details, see **Table 5**.

TABLE 5: AUTO RTS HYSTERESIS

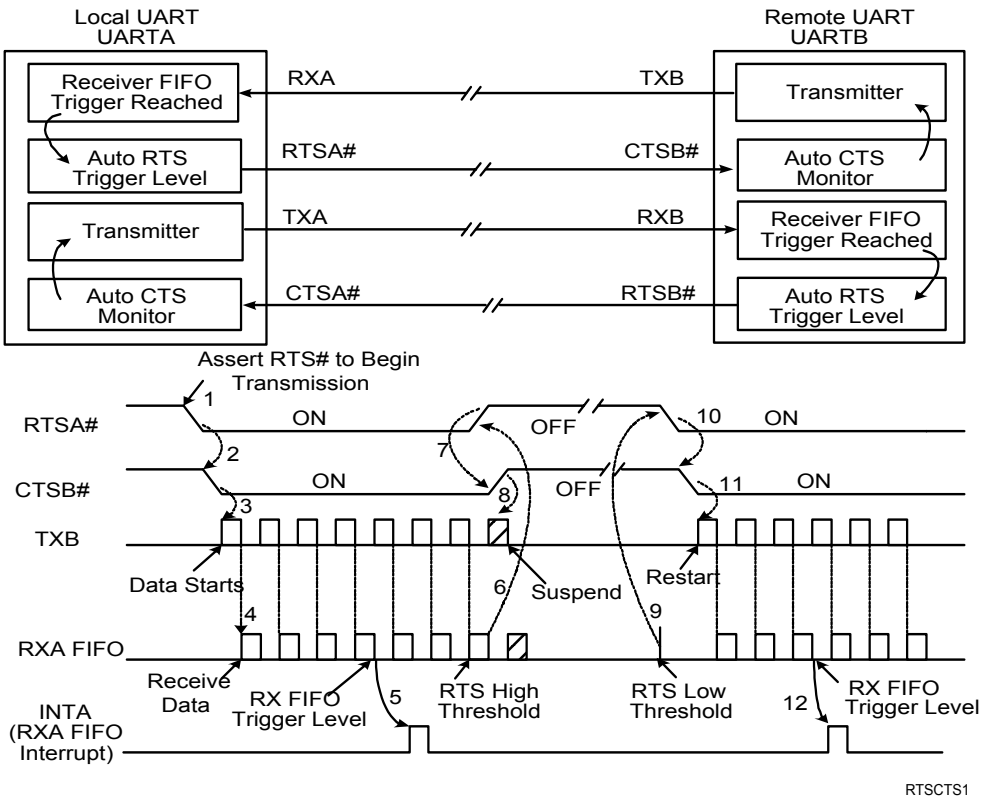
TRIGGER TABLE SELECTED (SEE TABLE 10)	FCTR BIT-1	FCTR BIT-0	TRIGGER LEVEL (CHARACTERS)	RTS HYSTERESIS (CHARACTERS)	INT PIN ACTIVATION	RTS# DE-ASSERTED (CHARACTERS)	RTS# ASSERTED (CHARACTERS)
Trigger Table-A	0	0	1	-	1	4	0
	0	0	4	-	4	8	1
	0	0	8	-	8	14	4
	0	0	14	-	14	14	8
Trigger Table-B	0	0	8	-	8	16	0
	0	0	16	-	16	24	8
	0	0	24	-	24	28	16
	0	0	28	-	28	28	24
Trigger Table-C	0	0	8	-	8	16	0
	0	0	16	-	16	56	8
	0	0	56	-	56	60	16
	0	0	60	-	60	60	56
Trigger Table-D (Programmable)	0	1	N	±4	N	N + 4	N - 4
	1	0	N	±6	N	N + 6	N - 6
	1	1	N	±8	N	N + 8	N - 8

2.16 Auto CTS (Hardware) Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 13**):

- Enable auto CTS flow control using EFR bit-7.
- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

FIGURE 13. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.17 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 14), the 850 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 850 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the 850 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the 850 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 14) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 850 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 850 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 850 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the 850 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS Hysteresis value in **Table 5**. **Table 6** below explains this when Trigger Table-B (See **Table 10**) is selected.

TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.*

2.18 Special Character Detect

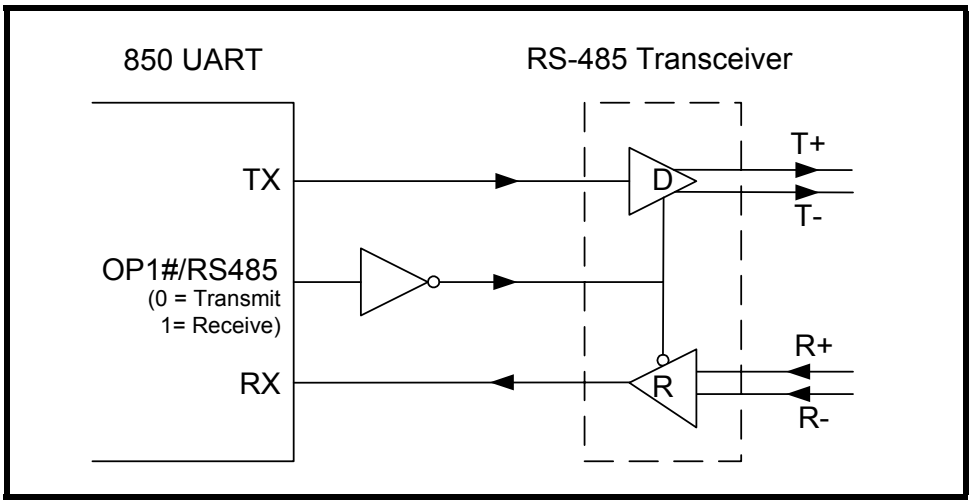
A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 850 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

2.19 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by MCR bit-2. It de-asserts OP1#/RS485 output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts OP1# output prior to sending the data. See **Figure 14**.

FIGURE 14. AUTO RS-485 HALF-DUPLEX CONTROL



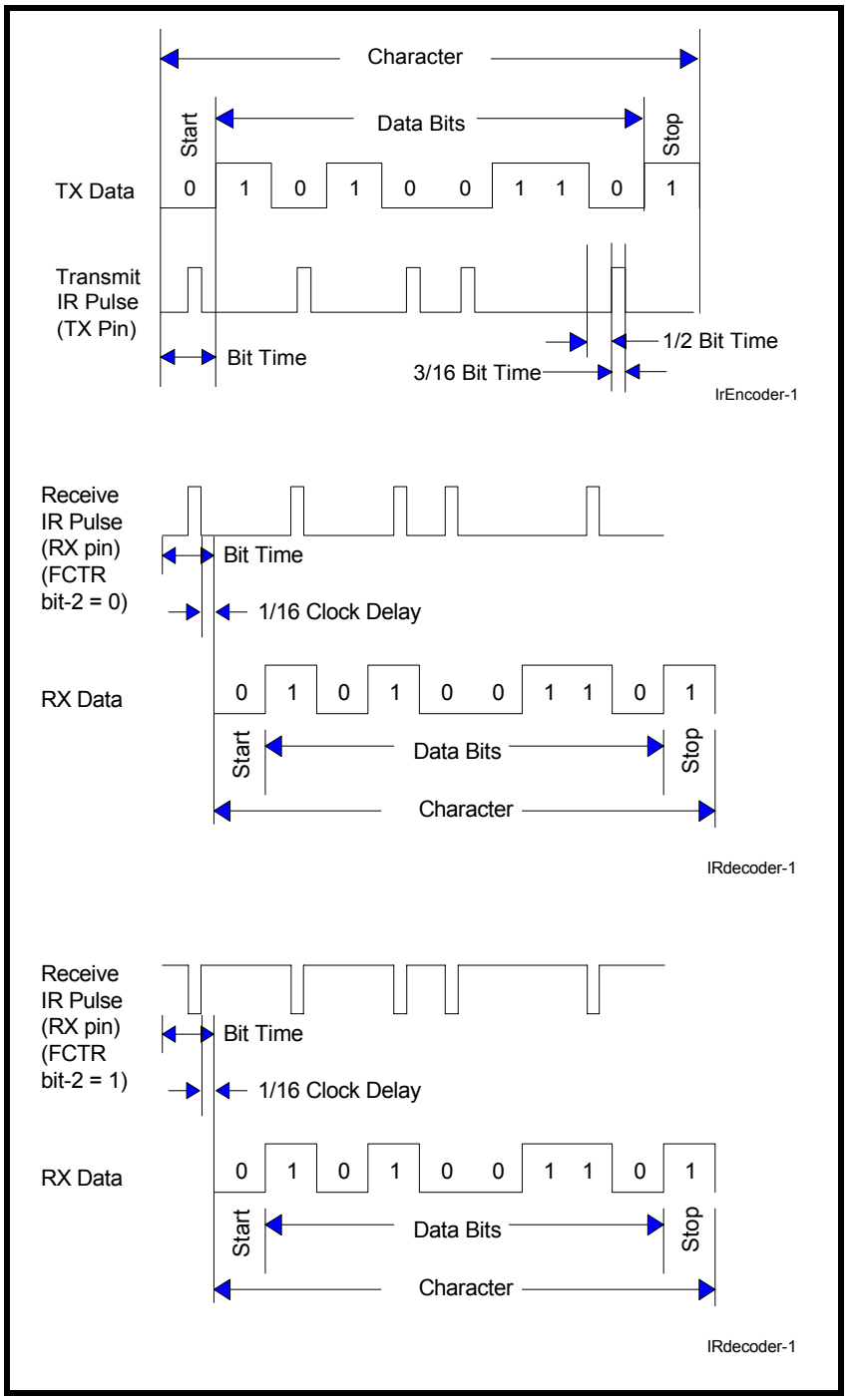
2.20 Infrared Mode

The 850 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 15**.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see **Figure 15**.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream. However, this is not true with some infrared modules on the market which indicate a logic 0 by a light pulse. So the 850 has a provision to invert the input polarity to accomodate this. In this case, the user can enable FCTR bit-2 to invert the incoming infrared RX signal.

FIGURE 15. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.21 Sleep Mode with Auto Wake-Up

The 850 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the 850 to enter sleep mode:

- no interrupts pending for the 850 (ISR bit-0 = 1)
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pin is idling at a logic 1

The 850 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 850 resumes normal operation by any of the following:

- a receive data start bit transition (logic 1 to 0)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the 850 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 850 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The 850 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

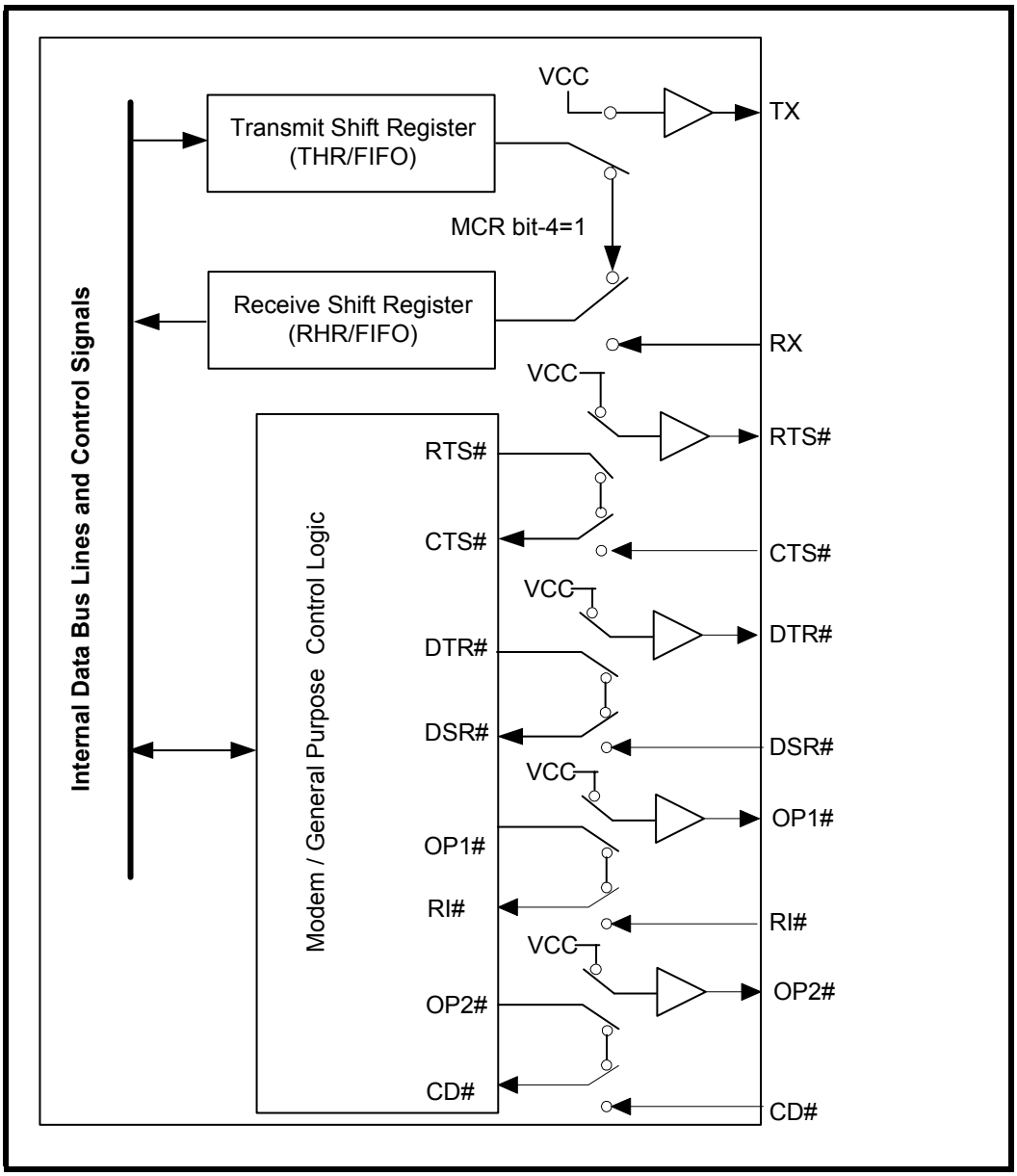
If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, and modem input lines remain steady when the 850 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 42. If the input lines are floating or are toggling while the 850 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX input is idling at logic 1 or “marking” condition during sleep mode. This may not occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on the RX input.

2.22 Internal Loopback

The 850 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 16 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 16. INTERNAL LOOPBACK



3.0 UART INTERNAL REGISTERS

The 850 has a set of configuration registers selected by address lines A0, A1 and A2. The 16C550 compatible registers can be accessed when LCR[7] = 0 and the baud rate generator divisor registers can be accessed when LCR[7] = 1 and LCR ≠ 0xBF. The enhanced registers are accessible only when LCR = 0xBF. The complete register set is shown on Table 7 and Table 8.

TABLE 7: XR16C850 UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Div Latch High Byte	Read/Write	
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR[7] = 0, FCTR[6] = 0
1 1 1	FLVL - TX/RX FIFO Level Counter Register	Read-only	LCR[7] = 0, FCTR[6] = 1
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	
ENHANCED REGISTERS			
0 0 0	TRG - TX/RX FIFO Trigger Level Reg FC - TX/RX FIFO Level Counter Register	Write-only Read-only	LCR = 0xBF
0 0 1	FCTR - Feature Control Reg	Read/Write	
0 1 0	EFR - Enhanced Function Reg	Read/Write	
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	