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GENERAL DESCRIPTION

The XR16C864[1] (864) is an enhanced quad Universal Asynchronous Receiver and Transmitter (UART) each with 128 bytes of transmit and receive FIFOs, transmit and receive FIFO counters and trigger levels, automatic hardware and software flow control, automatic RS-485 half-duplex direction control and data rates of up to 2 Mbps. Each UART has a set of registers that provide the user with operating status and control, receiver error indications, and modem serial interface controls. System interrupts may be tailored to meet design requirements. An internal loopback capability allows onboard diagnostics. The 864 is available in the 100-pin QFP package. The XR16C864 offers faster channel status access by providing separate outputs for TXRDY and RXRDY, offer separate Infrared TX outputs and a separate clock input for channel C (CHCCLK). The XR16C864 is compatible with the industry standard ST16C654 and XR16C854.

NOTE: *1 Covered by U.S. Patent #5,649,122 and #5,949,787.*

FEATURES

Added feature in devices with top mark date code of "F2 YYWW" and newer:

- 5 volt tolerant inputs

- 2.97 to 5.5 Volt Operation
- Pin-to-pin compatible with the industry standard ST16C654 and XR16C854
- Intel or Motorola Data Bus Interface select
- Four independent UART channels
  - Register Set Compatible to 16C550
  - Data rates of up to 2 Mbps
  - Transmit and Receive FIFOs of 128 bytes
  - Programmable TX and RX FIFO Trigger Levels
  - Transmit and Receive FIFO Level Counters
  - Automatic Hardware (RTS/CTS) Flow Control
  - Selectable Auto RTS Flow Control Hysteresis
  - Automatic Software (Xon/Xoff) Flow Control
  - Wireless Infrared (IrDA 1.0) Encoder/Decoder
- Sleep Mode (200 uA typical)
- Crystal oscillator or external clock input

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FIGURE 1. XR16C864 BLOCK DIAGRAM

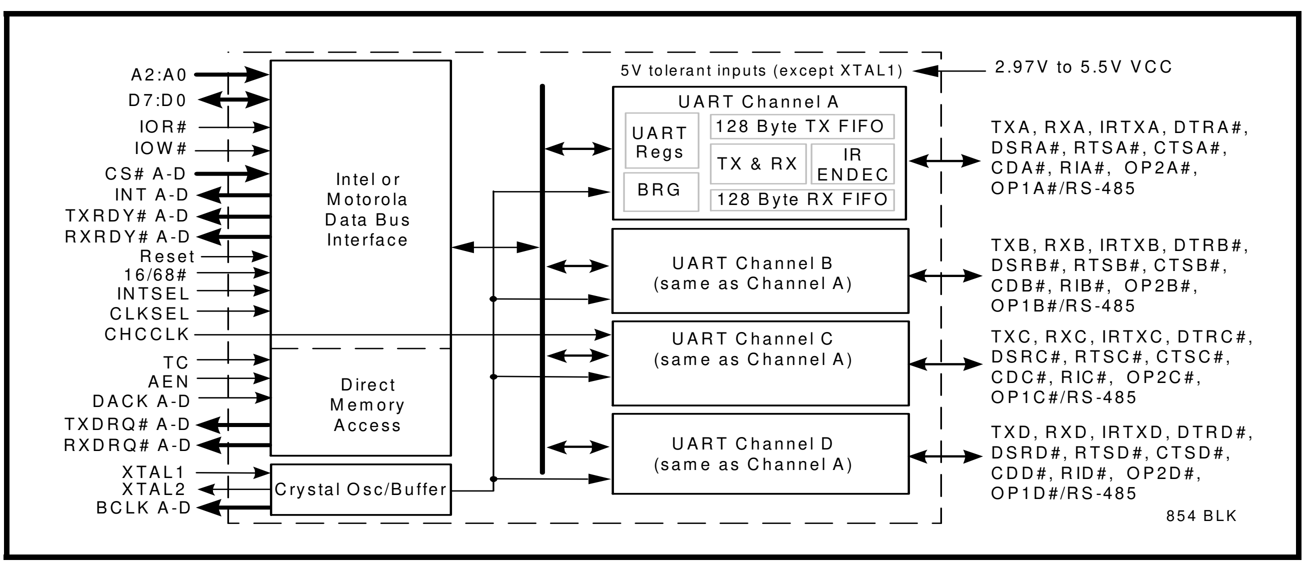
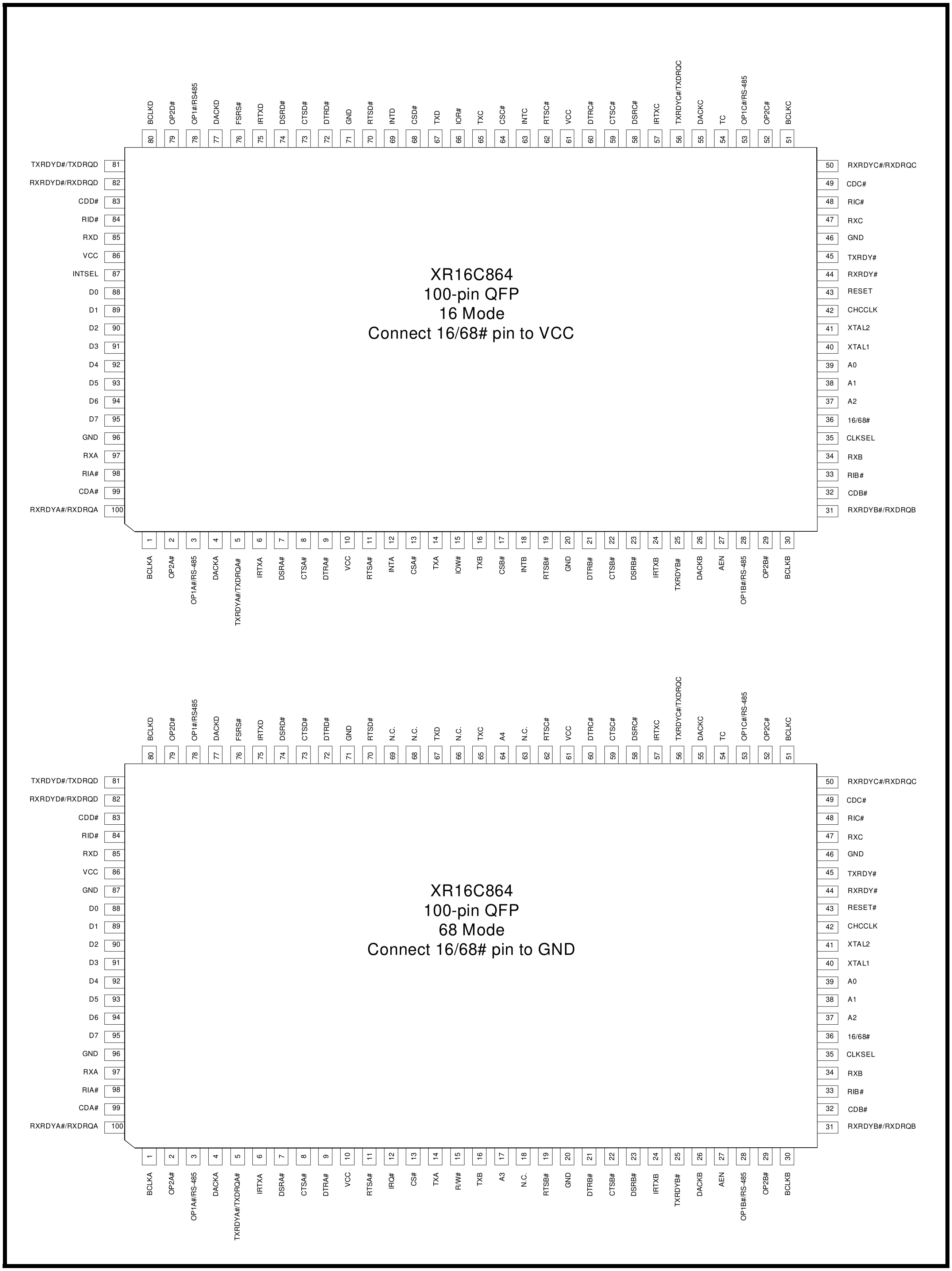


FIGURE 2. XR16C864 PIN OUT ASSIGNMENT IN 16 AND 68 MODE



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16C864CQ-F	100-Lead QFP	0°C to +70°C	Active
XR16C864CQTR-F	100-Lead QFP	0°C to +70°C	Active
XR16C864IQ-F	100-Lead QFP	-40°C to +85°C	Active
XR16C864IQTR-F	100-Lead QFP	-40°C to +85°C	Active

NOTE: TR = Tape and Reel, -F = Green / RoHS

PIN DESCRIPTIONS

Pin Description

NAME	100-QFP PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE			
A2 A1 A0	37 38 39	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channels A-D during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	95 94 93 92 91 90 89 88	I/O	Data bus lines [7:0] (bidirectional).
IOR# (N.C.)	66	I	When 16/68# pin is at logic 1, the Intel bus interface is selected and this input becomes read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When 16/68# pin is at logic 0, the Motorola bus interface is selected and this input is not used.
IOW# (R/W#)	15	I	When 16/68# pin is at logic 1, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is at logic 0, the Motorola bus interface is selected and this input becomes read (logic 1) and write (logic 0) signal.
CSA# (CS#)	13	I	When 16/68# pin is at logic 1, this input is chip select A (active low) to enable channel A in the device. When 16/68# pin is at logic 0, this input becomes the chip select (active low) for the Motorola bus interface.
CSB# (A3)	17	I	When 16/68# pin is at logic 1, this input is chip select B (active low) to enable channel B in the device. When 16/68# pin is at logic 0, this input becomes address line A3 which is used for channel selection in the Motorola bus interface.

Pin Description

Name	100-QFP Pin #	Type	Description
CSC# (A4)	64	I	When 16/68# pin is at logic 1, this input is chip select C (active low) to enable channel C in the device. When 16/68# pin is at logic 0, this input becomes address line A4 which is used for channel selection in the Motorola bus interface.
CSD# (N.C.)	68	I	When 16/68# pin is at logic 1, this input is chip select D (active low) to enable channel D in the device. When 16/68# pin is at logic 0, this input is not used.
INTA (IRQ#)	12	O (OD)	When 16/68# pin is at logic 1 for Intel bus interface, this ouput becomes channel A interrupt output. The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode when MCR[3] is set to a logic 1. INTA is set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3]. When 16/68# pin is at logic 0 for Motorola bus interface, this output becomes device interrupt output (active low, open drain). An external pull-up resistor is required for proper operation.
INTB INTC INTD (N.C.)	18 63 69	O	When 16/68# pin is at logic 1 for Intel bus interface, these ouputs become the interrupt outputs for channels B, C, and D. The output state is defined by the user through the software setting of MCR[3]. The interrupt outputs are set to the active mode when MCR[3] is set to a logic 1 and are set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3]. When 16/68# pin is at logic 0 for Motorola bus interface, these outputs are unused and will stay at logic zero level. Leave these outputs unconnected.
INTSEL	87	I	Interrupt Select (active high, input with internal pull-down). When 16/68# pin is at logic 1 for Intel bus interface, this pin can be used in conjunction with MCR bit-3 to enable or disable the INT A-D pins or override MCR bit-3 and enable the interrupt outputs. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR bit-3 to enable and disable the interrupt output pins. In this mode, MCR bit-3 is set to a logic 1 to enable the continuous output. See MCR bit-3 description for full detail. This pin must be at logic 0 in the Motorola bus interface mode.
TXRDYA# TXRDYB# TXRDYC# TXRDYD#	5 25 56 81	O	UART channels A-D Transmitter Ready (active low). These outputs provide the TX FIFO/THR status for transmit channels A-D. See **Table 5**. If Direct Memory Access is enabled, these outputs become Transmit Direct Memory Access Request outputs. See TXDRQ pin description for more details. If these outputs are unused, leave them unconnected.
RXRDYA# RXRDYB# RXRDYC# RXRDYD#	100 31 50 82	O	UART channels A-D Receiver Ready (active low). These outputs provide the RX FIFO/RHR status for receive channels A-D. See **Table 5**. If Direct Memory Access is enabled, these outputs become Receive Direct Memory Access Request outputs. See RXDRQ pin description for more details. If these outputs are unused, leave them unconnected.
TXRDY#	45	O	Transmitter Ready (active low). This output is a logically wire-ORed status of TXRDY# A-D. See **Table 5**. If this output is unused, leave it unconnected.
RXRDY#	44	O	Receiver Ready (active low). This output is a logically wire-ORed status of RXRDY# A-D. See **Table 5**. If this output is unused, leave it unconnected.

Pin Description

Name	100-QFP Pin #	Type	Description
FSRS#	76	I	FIFO Status Register Select (active low input with internal pull-up). The content of the FSTAT register is placed on the data bus when this pin becomes active. However it should be noted, D0-D3 contain the inverted logic states of TXRDY# A-D pins, and D4-D7 the logic states (un-inverted) of RXRDY# A-D pins. Address line is not required when reading this status register.
DIRECT MEMORY ACCESS INTERFACE			
TC	54	I	Direct Memory Access Terminal Count. A high pulse terminates a Direct Memory Access transaction. If Direct Memory Access is not used, this input should be connected to GND.
AEN	27	I	Address Enable for Direct Memory Access. A high at this input indicates a valid Direct Memory Access cycle. See DACK pin descriptions below for Direct Memory Access cycle description. If Direct Memory Access is not used, this input should be connected to GND.
DACKA DACKB DACKC DACKD	4 26 55 77	I	Direct Memory Access Acknowledge. Direct Memory Access cycle will start processing when CPU/Host sets this input low and AEN high. All writes will be to the TX FIFO and all reads will be from the RX FIFO. A0-A2 and CS# A-D will be ignored. If Direct Memory Access is not used, these inputs should be connected to VCC.
TXDRQA TXDRQB TXDRQC TXDRQD	5 25 56 81	O	Transmit Direct Memory Access Request. A transmit empty request is indicated by a high level on TXDRQ. The TXDRQ line is held high until either TC pulses or the TX FIFO is filled above its trigger level. Transmit Direct Memory Access Request is enabled by setting EMSR register bit-2 = 1. If Direct Memory Access is not used, leave these outputs unconnected.
RXDRQA RXDRQB RXDRQC RXDRQD	100 31 50 82	O	Receive Direct Memory Access Request. A Receive ready request is indicated by a high level on RXDRQ. The RXDRQ line is held high until either TC pulses or the RX FIFO is emptied. Receive Direct Memory Access Request is enabled by setting EMSR register bit-3 = 1. If Direct Memory Access is not used, leave these outputs unconnected.
MODEM OR SERIAL I/O INTERFACE			
TXA TXB TXC TXD	14 16 65 67	O	UART channels A-D Transmit Data and infrared transmit data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be a logic 1 during reset, or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is a logic 0.
IRTXA IRTXB IRTXC IRTXD	6 24 57 75	O	UART channels A-D Infrared Transmit Data. The inactive state (no data) for the Infrared encoder/decoder interface is a logic 0. Regardless of the logic state of MCR bit-6, this pin will be operating in the Infrared mode.
RXA RXB RXC RXD	97 34 47 85	I	UART channels A-D Receive Data or infrared receive data. Normal receive data input must idle at logic 1 condition. The infrared receiver pulses typically idles at logic 0 but can be inverted by software control prior going in to the decoder, see FCTR[2].
RTSA# RTSB# RTSC# RTSD#	11 19 62 70	O	UART channels A-D Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], FCTR[1:0], EMSR[5:4] and IER[6]. Also see **Figure 10**. If these outputs are not used, leave them unconnected.

Pin Description

NAME	100-QFP PIN #	TYPE	DESCRIPTION
CTSA# CTSB# CTSC# CTSD#	8 22 59 73	I	UART channels A-D Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. Also see **Figure 10**. These inputs should be connected to VCC when not used.
DTRA# DTRB# DTRC# DTRD#	9 21 60 72	O	UART channels A-D Data-Terminal-Ready (active low) or general purpose output. If these outputs are not used, leave them unconnected.
DSRA# DSRB# DSRC# DSRD#	7 23 58 74	I	UART channels A-D Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used.
CDA# CDB# CDC# CDD#	99 32 49 83	I	UART channels A-D Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used.
RIA# RIB# RIC# RID#	98 33 48 84	I	UART channels A-D Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used.
OP1A# OP1B# OP1C# OP1D#	3 28 53 78	O	General purpose output or RS-485 direction control signal. RS-485 direction control can be selected via FCTR bit-3. **SEE"AUTO RS485 HALF-DUPLEX CONTROL" ON PAGE 20.** If these outputs are unused, leave them unconnected.
OP2A# OP2B# OP2C# OP2D#	2 29 52 79	O	General purpose output. If these outputs are unused, leave them unconnected.
ANCILLARY SIGNALS			
XTAL1	40	I	Crystal or external clock input. This input is not 5V tolerant.
XTAL2	41	O	Crystal or buffered clock output.
BCLKA BCLKB BCLKC BCLKD	1 30 51 80	O	Baud Rate Generator Output. The baud rate generator clock output is internally connected to the RCLK input. This pin provides the 16X clock of the selected data rate from the baud rate generator.
16/68#	36	I	Intel or Motorola Bus Select (input with internal pull-up). When 16/68# pin is at logic 1, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When 16/68# pin is at logic 0, 68 or Motorola mode, the device will operate in the Motorola bus type of interface.

Pin Description

NAME	100-QFP PIN #	TYPE	DESCRIPTION
CLKSEL	35	I	Baud-Rate-Generator Input Clock Prescaler Select for channels A-D. This input is only sampled during power up or a reset. Connect to VCC for divide by 1 and GND for divide by 4. MCR[7] can override the state of this pin following a reset or initialization. See MCR bit-7 and **Figure 5** in the Baud Rate Generator section.
CHCCLK	42	I	This input provides the clock for UART channel C. An external 16X baud clock or the crystal oscillator's output, XTAL2, must be connected to this pin for normal operation. This input may also be used with MIDI (Musical Instrument Digital Interface) applications when an external MIDI clock is provided.
RESET (RESET#)	43	I	When 16/68# pin is at logic 1 for Intel bus interface, this input becomes the Reset pin (active high). In this case, a 40 ns minimum logic 1 pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held at logic 1, the receiver input will be ignored and outputs are reset during reset period (**Table 19**). When 16/68# pin is at a logic 0 for Motorola bus interface, this input becomes Reset# pin (active low). This pin functions similarly, but instead of a logic 1 pulse, a 40 ns minimum logic 0 pulse will reset the internal registers and outputs.
VCC	10, 61, 86	Pwr	2.97V to 5.5V power supply. All input pins, except XTAL1, are 5V tolerant.
GND	20, 46, 71, 96	Pwr	Power supply common, ground.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

Factory Test Mode

If the IOR#, IOW# and CS# pins are all asserted (at a logic 0), the 864 will enter a Factory Test Mode.

1.0 PRODUCT DESCRIPTION

The XR16C864 (864) integrates the functions of 4 enhanced 16C550 Universal Asynchronous Receiver and Transmitter (UART). Each UART is independently controlled having its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 128-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, FIFO level counters, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 2 Mbps. The XR16C864 can operate at 3.3 or 5 volts. The 864 is fabricated with an advanced CMOS process.

Enhanced FIFO

The 864 QUART provides a solution that supports 128 bytes of transmit and receive FIFO memory, instead of 64 bytes provided in the ST16C654 and 16 bytes in the ST16C554, or one byte in the ST16C454. The 864 is designed to work with high performance data communication systems, that require fast data processing time. Increased performance is realized in the 864 by the larger transmit and receive FIFOs, FIFO trigger level control, FIFO level counters and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C554 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 128 byte FIFO in the 864, the data buffer will not require unloading/loading for 12.2 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

Data Rate

The 864 is capable of operation up to 2 Mbps at 5V with 16x internal sampling clock rate. The device can operate with a crystal oscillator of up to 24 MHz crystal on pins XTAL1 and XTAL2, or external clock source of 32 MHz on XTAL1 pin. With a typical crystal of 14.7456 MHz and through a software option, the user can set the prescaler bit for data rates of up to 921.6 kbps.

Enhanced Features

The rich feature set of the 864 is available through the internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. MCR bit-5 provides a facility for turning off software flow control with any incoming (RX) character. In the 16 mode INTSEL and MCR bit-3 can be configured to provide a software controlled or continuous interrupt capability.

The XR16C864 offers a clock prescaler select pin to allow system/board designers to preset the default baud rate table on power up. The CLKSEL pin selects the div-by-1 or div-by-4 prescaler for the baud rate generator. It can then be overridden following initializatioin by MCR bit-7.

The 864 offers several other enhanced features. These features include a CHCCLK clock input, FSTAT register, separate IrDA TX outputs, separate RXRDY and TXRDY outputs and a Direct Memory Access interface. The CHCCLK must be connected to the XTAL2 pin for normal operation or to external MIDI (Music Instrument Digital Interface) oscillator for MIDI applications. A separate register (FSTAT) is provided for monitoring the real time status of the FIFO signals TXRDY# and RXRDY# for each of the four UART channels (A-D). Separate TXRDY and RXRDY outputs for the individual channels are also provided. For infrared applications, four separate IrDA (Infrared Data Association Standard) TX outputs are provided. These outputs are provided in addition to the standard asynchronous modem data outputs.

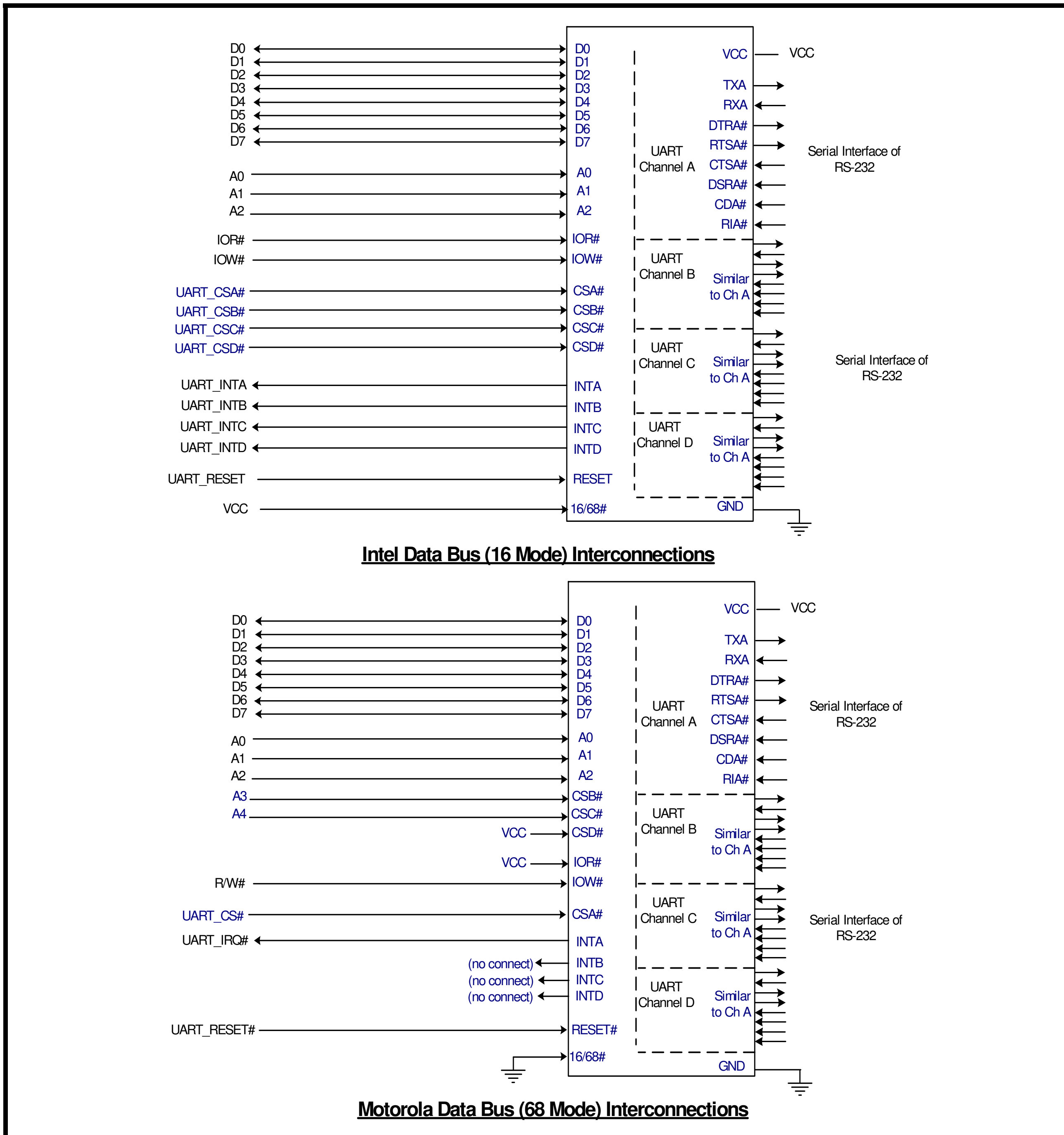
A full Direct Memory Access interface is provided with separate DRQ lines for RX and TX FIFOs of the individual channels.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The 864 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS# A-D, IOR# and IOW# or CS#, R/W#, A4 and A3 inputs. All four UART channels share the same data bus for host operations. A typical data bus interconnection for Intel and Motorola mode is shown in Figure 3.

FIGURE 3. XR16C864 TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS



2.2 5-Volt Tolerant Inputs

For devices that have top mark date code "F2 YYWW" and newer, the 864 can accept a voltage of up to 5.5V on any of its inputs (except XTAL1) when operating from 2.97V to 5.5V. XTAL1 is not 5 volt tolerant. Devices that have top mark date code "DC YYWW" and older do not have 5V tolerant inputs.

2.3 Device Reset

The RESET input resets the internal registers and the serial interface outputs in all four channels to their default state (see Table 19). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device. Following a power-on reset or an external reset, the 864 is software compatible with previous generation of UARTs, 16C454 and 16C554 and 16C654.

2.4 Device Identification and Revision

The XR16C864 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x14 for the XR16C864 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 Channel Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. During Intel Bus Mode (16/68# pin is connected to VCC), a logic 0 on chip select pins, CSA#, CSB#, CSC# or CSD# allows the user to select UART channel A, B, C or D to configure, send transmit data and/or unload receive data to/from the UART. Selecting all four UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from all four uarts simultaneously. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A-D SELECT IN 16 MODE

CSA#	CSB#	CSC#	CSD#	FUNCTION
1	1	1	1	UART de-selected
0	1	1	1	Channel A selected
1	0	1	1	Channel B selected
1	1	0	1	Channel C selected
1	1	1	0	Channel D selected
0	0	0	0	Channels A-D selected

During Motorola Bus Mode (16/68# pin is connected to GND), the package interface pins are configured for connection with Motorola, and other popular microprocessor bus types. In this mode the 864 decodes two additional addresses, A3 and A4, to select one of the four UART ports. The A3 and A4 address decode function is used only when in the Motorola Bus Mode. See Table 2.

TABLE 2: CHANNEL A-D SELECT IN 68 MODE

CS#	A4	A3	FUNCTION
1	N/A	N/A	UART de-selected
0	0	0	Channel A selected
0	0	1	Channel B selected
0	1	0	Channel C selected
0	1	1	Channel D selected

2.6 Channels A-D Internal Registers

Each UART channel in the 864 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scratchpad register (SPR).

Beyond the general 16C550 features and capabilities, the 864 offers enhanced feature registers (EMSR, FLVL, EFR, Xon/Xoff 1, Xon/Xoff 2, FCTR, TRG, FC) that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, automatic RS-485 half-duplex direction output enable/disable, FIFO trigger level control, and FIFO level counters. All the register functions are discussed in full detail later in "Section 3.0, UART Internal Registers" on page 23.

2.7 INT Ouputs for Channels A-D

The interrupt outputs change according to the operating mode and enhanced features setup. Table 3 and 4 summarize the operating behavior for the transmitter and receiver. Also see Figure 19 through 23.

TABLE 3: INT PINS OPERATION FOR TRANSMITTER FOR CHANNELS A-D

	FCTR Bit-3	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)	
			FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
INT Pin	0	0 = a byte in THR 1 = THR empty	0 = FIFO above trigger level 1 = FIFO below trigger level or FIFO empty	0 = FIFO above trigger level 1 = FIFO below trigger level or FIFO empty
INT Pin	1	0 = a byte in THR 1 = transmitter empty	0 = FIFO above trigger level 1 = FIFO below trigger level or transmitter empty	0 = FIFO above trigger level 1 = FIFO below trigger level or transmitter empty

TABLE 4: INT PIN OPERATION FOR RECEIVER FOR CHANNELS A-D

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
INT Pin	0 = no data 1 = 1 byte	0 = FIFO below trigger level 1 = FIFO above trigger level	0 = FIFO below trigger level 1 = FIFO above trigger level

2.8 Direct Memory Access

In this document, Direct Memory Access will not be referred to by its acronym (DMA) to avoid confusion with DMA Mode (a legacy term) that refers to data block transfer operation. Direct Memory Access mode is enabled via EMSR bits 2 and 3. The Direct Memory Access transaction is controlled through the RXDRQ [A-D], TXDRQ [A-D], DACK [A-D], AEN and TC pins.

2.9 DMA Mode

The DMA Mode (a legacy term) in this document doesn't mean "direct memory access" but refers to data block transfer operation. (Since the 864 also supports Direct Memory Access, "Direct Memory Access" will be used instead of "DMA" when explaining Direct Memory Access.) The DMA mode affects the state of the RXRDY# A-D and TXRDY# A-D output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 864 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. The following table show their behavior. Also see **Figure 19** through **23**.

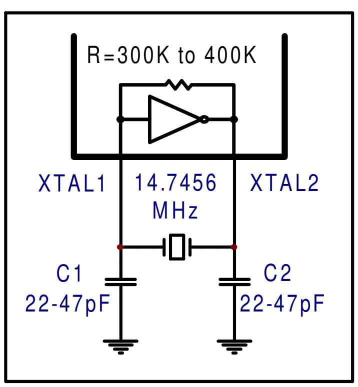
TABLE 5: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE FOR CHANNELS A-D

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY#	0 = 1 byte 1 = no data	0 = at least 1 byte in FIFO 1 = FIFO empty	1 to 0 transition when FIFO reaches the trigger level, or timeout occurs. 0 to 1 transition when FIFO empties.
TXRDY#	0 = THR empty 1 = byte in THR	0 = FIFO empty 1 = at least 1 byte in FIFO	0 = FIFO has at least 1 empty location. 1 = FIFO is full.

2.10 Crystal Oscillator or External Clock Input

The 864 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for all four UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see "Programmable Baud Rate Generator."

FIGURE 4. TYPICAL OSCILATOR CONNECTIONSL



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 4). Typical standard crystal frequencies are: 1.8432, 3.6864, 7.3728, 14.7456, 18.432, and 22.1184 MHz. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typical oscillator connections are shown in Figure 4. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.11 Programmable Baud Rate Generator

Each UART has its own Baud Rate Generator (BRG) with a prescaler. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling rate clock of the serial data rate. The sampling rate clock is used by the transmitter for data bit shifting and receiver for data sampling.

FIGURE 5. BAUD RATE GENERATOR AND PRESCALER

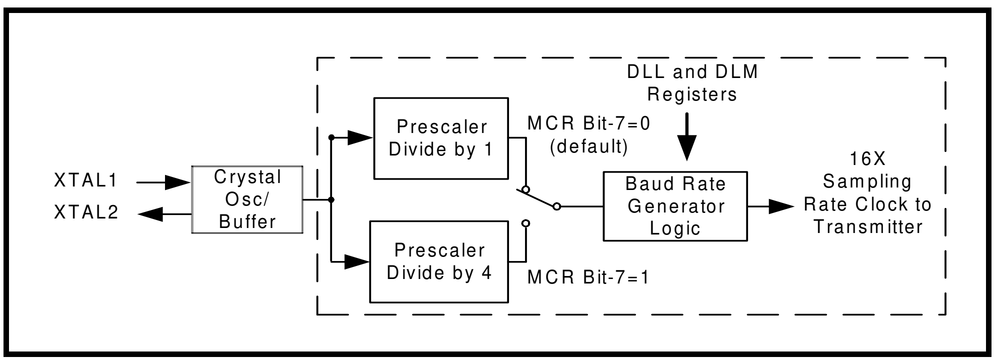


Table 6 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X sampling rate. When using a non-standard frequency crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 6: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0 (DEFAULT)	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

2.12 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 128 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the TX FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

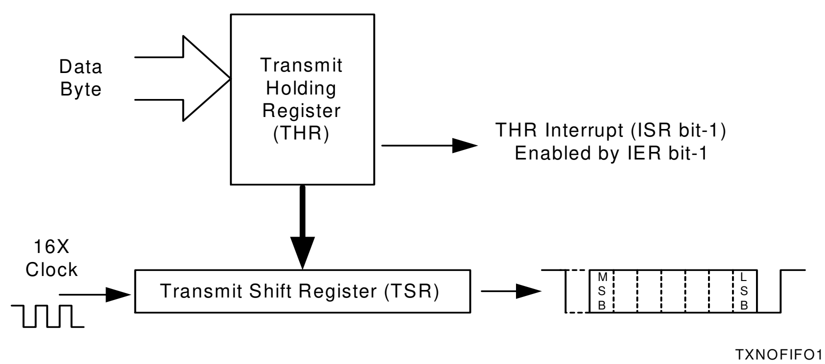
2.12.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 128 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.12.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

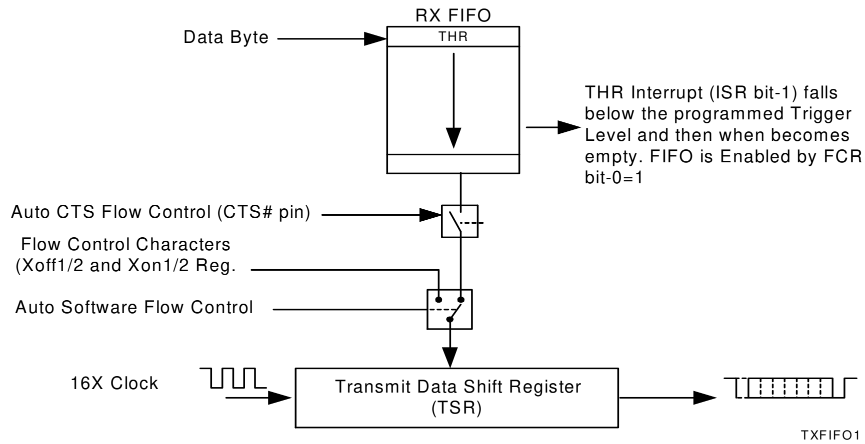
FIGURE 6. TRANSMITTER OPERATION IN NON-FIFO MODE



2.12.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 128 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the TX FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the FIFO becomes empty. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/TX FIFO becomes empty.

FIGURE 7. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.13 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 128 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.13.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 128 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 8. RECEIVER OPERATION IN NON-FIFO MODE

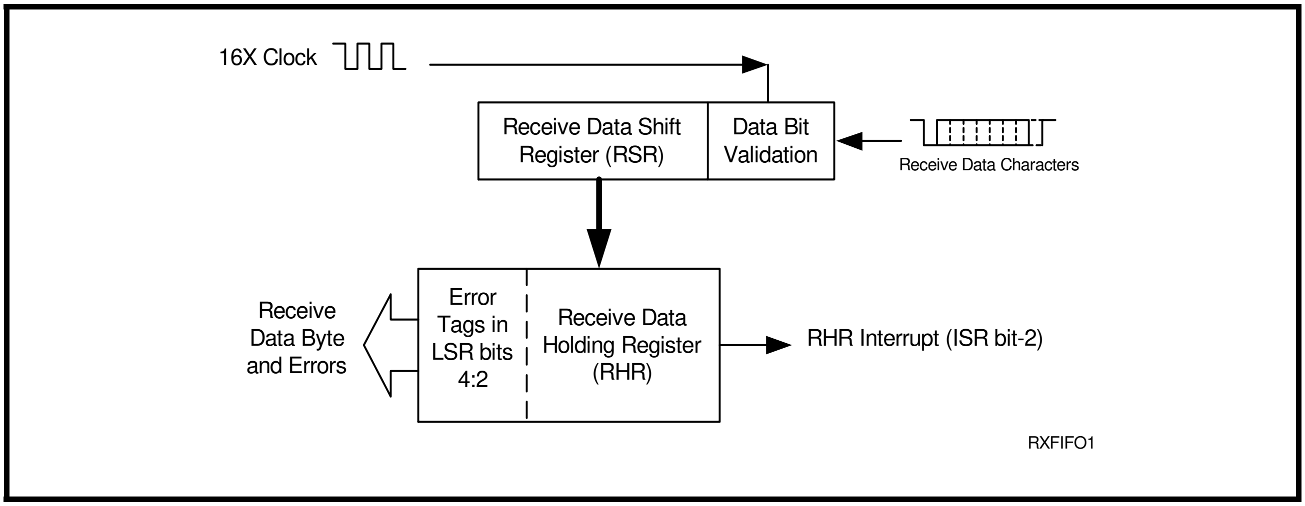
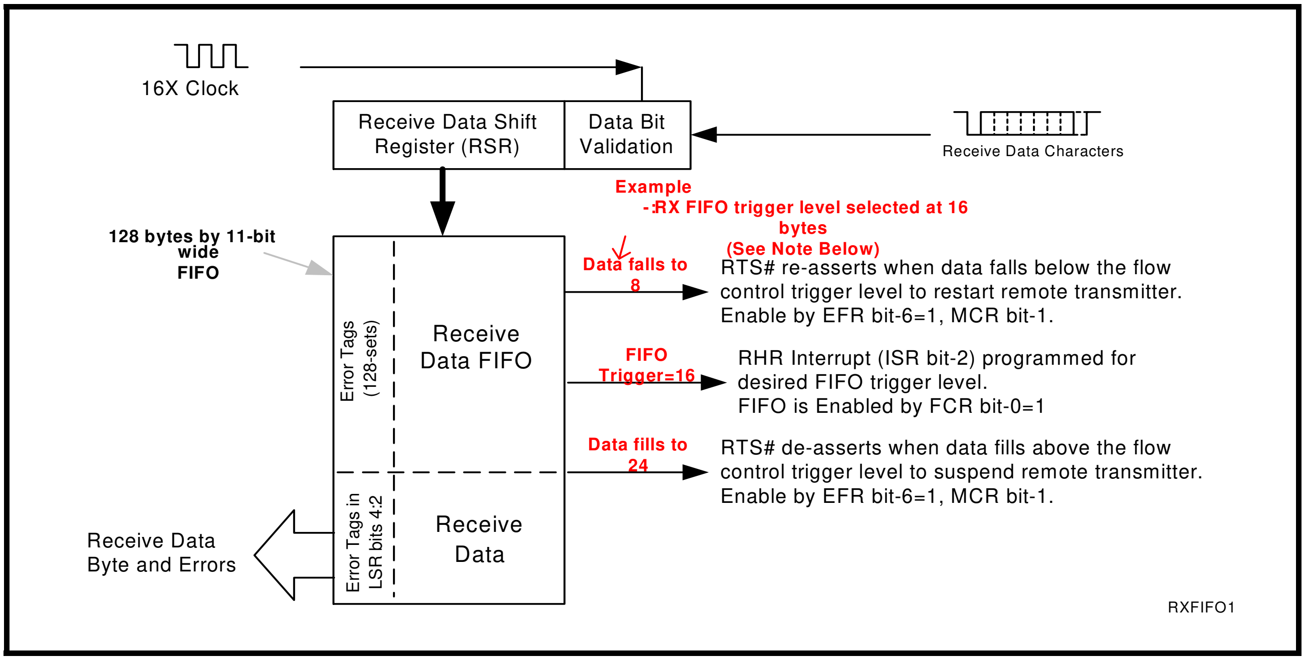


FIGURE 9. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: *Table-B selected as Trigger Table for* **Figure 9** *(***Table 11***).*

2.14 Auto RTS Hardware Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 10**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.15 Auto RTS Hysteresis

The 864 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the XR16C850, ST16C650A and ST16C550 family of UARTs. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS# pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the upper limit of the hysteresis level. The RTS# pin will return to a logic 0 after the RX FIFO is unloaded to the lower limit of the hysteresis level. Under the above described conditions, the 864 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted to a logic 0 (RTS On). **Table 15** shows the complete details for the Auto RTS# Hysteresis levels. Please note that this table is for programmable trigger levels only (Table D). The hysteresis values for Tables A-C are the next higher and next lower trigger levels in Tables A-C (See **Table 11**).

2.16 Auto CTS Flow Control

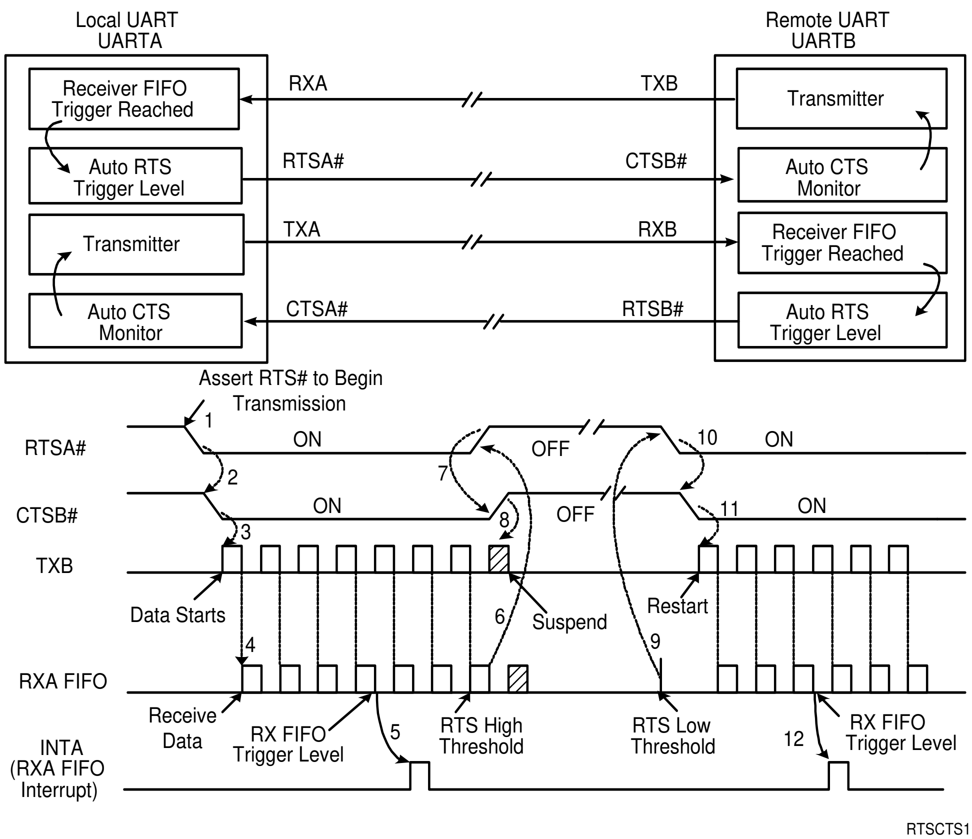
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 10**):

- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

FIGURE 10. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.17 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (**See Table 18**), the 864 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) match the programmed values, the 864 will halt transmission as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the 864 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the 864 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (**See Table 18**) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 864 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 864 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 864 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the 864 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS Hysteresis value in **Table 15**. **Table 7** below explains this when Trigger Table-B (See **Table 11**) is selected.

TABLE 7: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

* *After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2* characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.

2.18 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 864 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

2.19 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit-3. By default, it de-asserts OP1#/RS485 (logic 1) output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts OP1#/RS485 (logic 0) output prior to sending the data.

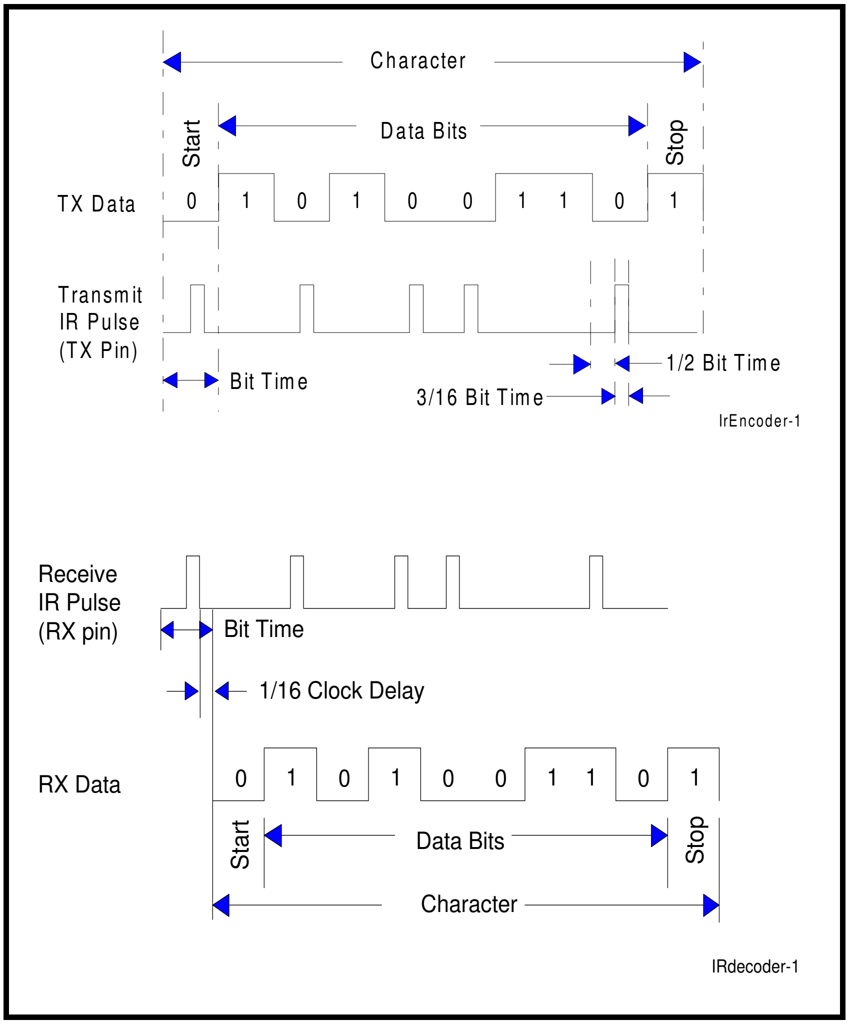
2.20 Infrared Mode

The 864 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each "0" bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 11** below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a '1'. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see **Figure 11**.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream. However, this is not true with some infrared modules on the market which indicate a logic 0 by a light pulse. So the 864 has a provision to invert the input polarity to accomodate this. In this case, user can enable FCTR bit-2 to invert the input signal.

FIGURE 11. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.21 Sleep Mode with Auto Wake-Up

The 864 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the 864 to enter sleep mode:

- no interrupts pending for all four channels of the 864 (ISR bit-0 = 1)
- sleep mode of all four channels are enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idling at a logic 1

The 864 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 864 resumes normal operation by any of the following:

- a receive data start bit transition (logic 1 to 0)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the 864 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 864 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending in any channel. The 864 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

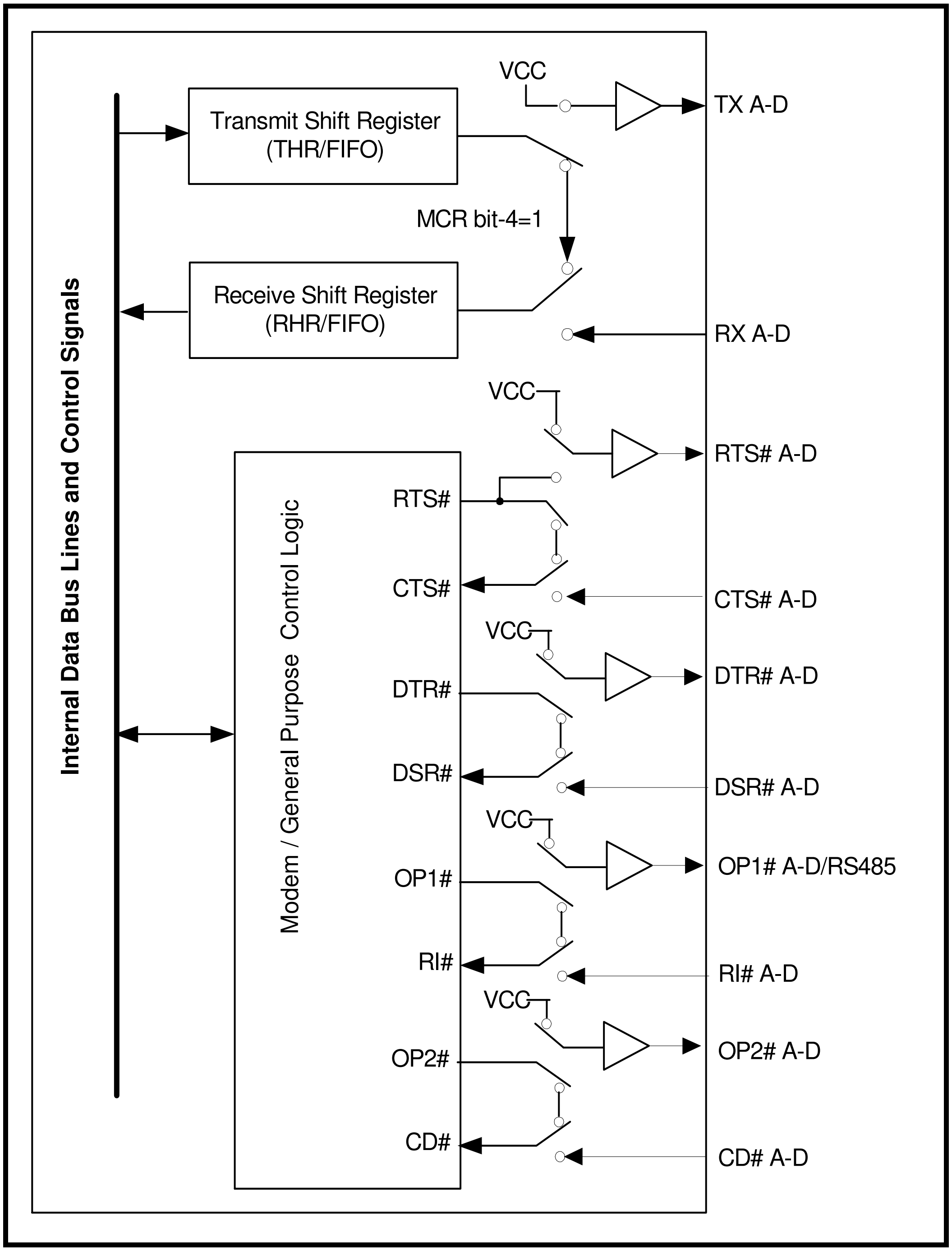
If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, CSC#, CSD# and modem input lines remain steady when the 864 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 42. If the input lines are floating or are toggling while the 864 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX input is idling at logic 1 or “marking” condition during sleep mode. This may not occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on the RX A-D inputs.

2.22 Internal Loopback

The 864 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 12 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 12. INTERNAL LOOP BACK IN CHANNELS A-D



3.0 UART INTERNAL REGISTERS

Each UART channel in the 864 has its own set of configuration registers selected by address lines A0, A1 and A2 with a specific channel selected (See Table 1 and Table 2). The complete register set is shown on Table 8 and Table 9.

TABLE 8: UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
	16C550 COMPATIBLE REGISTERS		
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Div Latch High Byte	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR[7] = 0
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	LCR[7] = 0
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	LCR[7] = 0
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR[7] = 0, FCTR[6] = 0
1 1 1	FLVL - TX/RX FIFO Level Counter Register	Read-only	LCR[7] = 0, FCTR[6] = 1
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	LCR[7] = 0, FCTR[6] = 1
	ENHANCED REGISTERS		
0 0 0	TRG - TX/RX FIFO Trigger Level Reg FC - TX/RX FIFO Level Counter Register	Write-only Read-only	LCR = 0xBF
0 0 1	FCTR - Feature Control Reg	Read/Write	LCR = 0xBF
0 1 0	EFR - Enhanced Function Reg	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	LCR = 0xBF
1 0 1	Xon-2 - Xon Character 2	Read/Write	LCR = 0xBF
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	LCR = 0xBF
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	LCR = 0xBF
X X X	FSTAT - FIFO Status Register	Read-only	FSRS# pin is logic 0

.

TABLE 9: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS# Int. Enable	0/ RTS# Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR[7] = 0
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Mode ENable	0/ XonAny	Internal Lopback Enable	OP2#/ INT Out-put Enable	OP1#/ RS-485 Output Control	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run Error	RX Data Ready	LCR[7] = 0
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 0 FCTR[6]=0
1 1 1	EMSR	WR	Rsvd	Rsvd	Auto RTS Hyst. bit-3	Auto RTS Hyst. bit-2	Enable RX DMA	Enable TX DMA	Rx/Tx FIFO Count	Rx/Tx FIFO Count	LCR[7] = 0 FCTR[6]=1
1 1 1	FLVL	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 9: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR≠0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	1	0	1	0	0	
Enhanced Registers											
0 0 0	TRG	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
0 0 0	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	FCTR	RD/WR	RX/TX Mode	SCPAD Swap	Trig Table Bit-1	Trig Table Bit-0	Auto RS485 Direction Control	RX IR Input Inv.	Auto RTS Hyst Bit-1	Auto RTS Hyst Bit-0	
0 1 0	EFR	RD/WR	Auto CTS# Enable	Auto RTS# Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5]	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
X X X	FSTAT	RD	RX-RDYD#	RX-RDYC#	RX-RDYB#	RX-RDYA#	TX-RDYD#	TX-RDYC#	TX-RDYB#	TX-RDYA#	FSRS# pin is a logic 0. No address lines required.