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XR16L2750

2.25V TO 5.5V DUART WITH 64-BYTE FIFO

APRIL 2005 *REV. 1.2.1*

GENERAL DESCRIPTION

The XR16L2750[1] (2750) is a low voltage dual universal asynchronous receiver and transmitter (UART) with 5 Volt tolerant inputs. The device operates from 2.25 to 5.5 Volt supply range and is pin-to-pin compatible to Exar's ST16C2550 and XR16C2850 except the 48-TQFP package. The 2750 register set is compatible to the ST16C2550 and the XR16C2850 enhanced features. It supports the Exar's enhanced features of 64 bytes of TX and RX FIFOs, programmable FIFO trigger level and FIFO level counters, automatic hardware (RTS/CTS) and software flow control, automatic RS-485 half duplex direction control output and a complete modem interface. Onboard registers provide the user with operational status and data error flags. An internal loopback capability allows system diagnostics. Independent programmable baud rate generators are provided in each channel to select data rates up to 6.25 Mbps at 5 Volt and 8X sampling clock. The 2750 is available in 48-pin TQFP and 44-pin PLCC packages.

NOTE: *1 Covered by U.S. Patent #5,649,122 and #5,949,787*

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FEATURES

- **2.25 to 5.5 Volt Operation**
- **5 Volt Tolerant Inputs**
- Pin-to-pin compatible to Exar's ST16C2550 and TI's TL16C752B on the 48-TQFP package
- Pin alike XR16C2850 48-TQFP package but without CLK8/16, CLKSEL and HDCNTL inputs
- Two independent UART channels
  - Reg set compatible to 16C2550 and 16C2850
  - Up to 6.25 Mbps at 5 Volt, 4 Mbps at 3.3 Volt, and 3 Mbps at 2.5 Volt with 8X sampling rate
  - Transmit and Receive FIFOs of 64 bytes
  - Programmable TX and RX FIFO Trigger Levels
  - Transmit and Receive FIFO Level Counters
  - Automatic Hardware (RTS/CTS) Flow Control
  - Selectable Auto RTS Flow Control Hysteresis
  - Automatic Software (Xon/Xoff) Flow Control
  - Automatic RS-485 Half-duplex Direction Control Output via RTS#
  - Wireless Infrared (IrDA 1.0) Encoder/Decoder
  - Automatic sleep mode
  - Full modem interface
- Device Identification and Revision
- Crystal oscillator or external clock input
- Industrial and commercial temperature ranges
- 48-TQFP and 44-PLCC packages

FIGURE 1. XR16L2750 BLOCK DIAGRAM

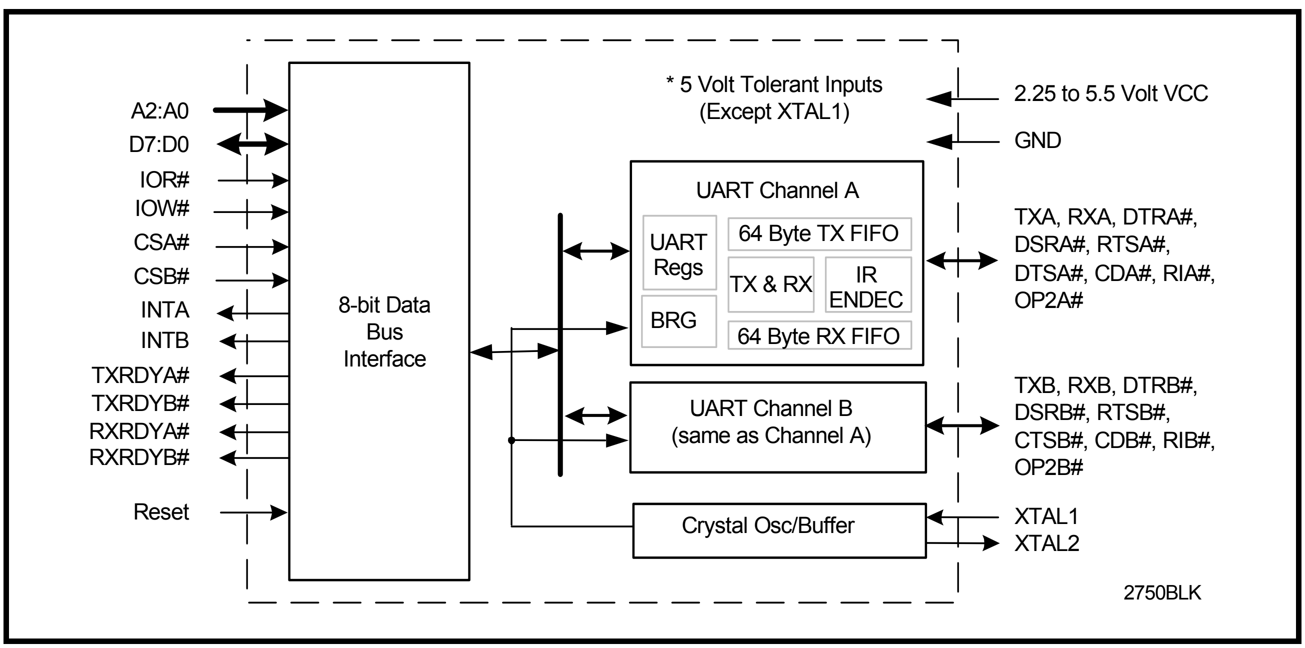
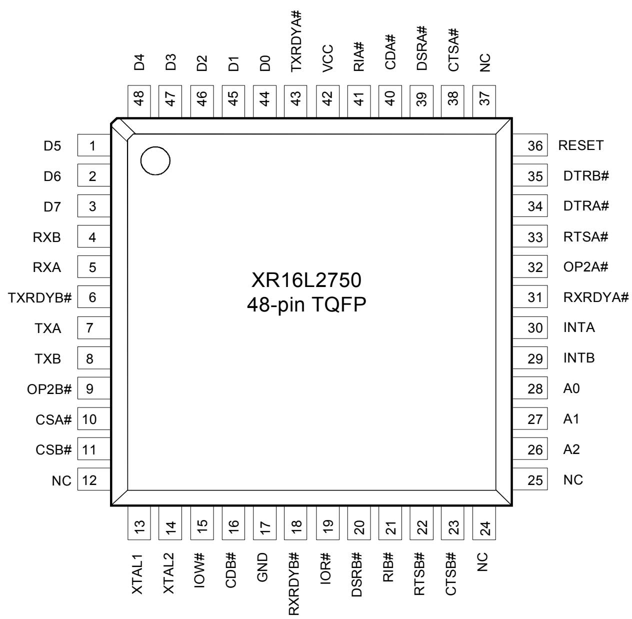
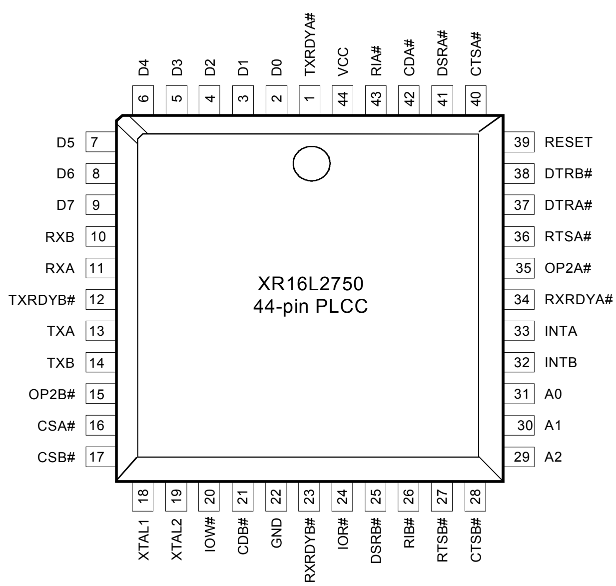


FIGURE 2. PIN OUT ASSIGNMENT





ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16L2750CJ	44-Lead PLCC	0°C to +70°C	Active
XR16L2750IJ	44-Lead PLCC	-40°C to +85°C	Active
XR16L2750CM	48-Lead TQFP	0°C to +70°C	Active
XR16L2750IM	48-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE				
A2 A1 A0	29 30 31	26 27 28	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A/B during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	9 8 7 6 5 4 3 2	3 2 1 48 47 46 45 44	I/O	Data bus lines [7:0] (bidirectional).
IOR#	24	19	I	Input/Output Read Strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed to by the address lines [A2:A0]. The data byte is placed on the data bus to allow the host processor to read it on the rising edge.
IOW#	20	15	I	Input/Output Write Strobe (active low). The falling edge instigates an internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines.
CSA#	16	10	I	UART channel A select (active low) to enable UART channel A in the device for data bus operation.
CSB#	17	11	I	UART channel B select (active low) to enable UART channel B in the device for data bus operation.
INTA	33	30	O	UART channel A Interrupt output. The output state is defined by the user through the software setting of MCR[3]. INTA is set to the active mode and OP2A# output LOW when MCR[3] is set to a logic 1. INTA is set to the three state mode and OP2A# output HIGH when MCR[3] is set to a logic 0 (default). See MCR[3].
INTB	32	29	O	UART channel B Interrupt output. The output state is defined by the user through the software setting of MCR[3]. INTB is set to the active mode and OP2B# output LOW when MCR[3] is set to a logic 1. INTB is set to the three state mode and OP2B# output HIGH when MCR[3] is set to a logic 0 (default). See MCR[3].
TXRDYA#	1	43	O	UART channel A Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel A. See Table 2. If it is not used, leave it unconnected.
RXRDYA#	34	31	O	UART channel A Receiver Ready (active low). This output provides the RX FIFO/RHR status for receive channel A. See Table 2. If it is not used, leave it unconnected.
TXRDYB#	12	6	O	UART channel B Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel B. See Table 3. If it is not used, leave it unconnected.

Pin Description

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
RXRDYB#	23	18	O	UART channel B Receiver Ready (active low). This output provides the RX FIFO/RHR status for receive channel B. See Table 2. If it is not used, leave it unconnected.
				MODEM OR SERIAL I/O INTERFACE
TXA	13	7	O	UART channel A Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be HIGH during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is LOW. If it is not used, leave it unconnected.
RXA	11	5	I	UART channel A Receive Data or infrared receive data. Normal receive data input must idle HIGH. The infrared receiver pulses typically idles at LOW but can be inverted by software control prior going in to the decoder, see MCR[6] and FCTR[2]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSA#	36	33	O	UART channel A Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], FCTR[1:0], EMSR[5:4] and IER[6]. For auto RS485 half-duplex direction control, see FCTR[3] and EMSR[3].
CTSA#	40	38	I	UART channel A Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. This input should be connected to VCC when not used.
DTRA#	37	34	O	UART channel A Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRA#	41	39	I	UART channel A Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDA#	42	40	I	UART channel A Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIA#	43	41	I	UART channel A Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
OP2A#	35	32	O	Output Port 2 Channel A - The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode and OP2A# output LOW when MCR[3] is set to a logic 1. INTA is set to the three state mode and OP2A# output HIGH when MCR[3] is set to a logic 0. See MCR[3]. This output should not be used as a general output else it will disturb the INTA output functionality.
TXB	14	8	O	UART channel B Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be HIGH during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is LOW. If it is not used, leave it unconnected.

Pin Description

NAME	44-PLCC PIN #	48-TQFP PIN #	TYPE	DESCRIPTION
RXB	10	4	I	UART channel B Receive Data or infrared receive data. Normal receive data input must idle HIGH. The infrared receiver pulses typically idles at logic 0 but can be inverted by software control prior going in to the decoder, see MCR[6] and FCTR[2]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSB#	27	22	O	UART channel B Request-to-Send (active low) or general purpose output. This port must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], FCTR[1:0], EMSR[5:4] and IER[6]. For auto RS485 half-duplex direction control, see FCTR[3] and EMSR[3].
CTSB#	28	23	I	UART channel B Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. This input should be connected to VCC when not used.
DTRB#	38	35	O	UART channel B Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRB#	25	20	I	UART channel B Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDB#	21	16	I	UART channel B Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIB#	26	21	I	UART channel B Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
OP2B#	15	9	O	Output Port 2 Channel B - The output state is defined by the user and through the software setting of MCR[3]. INTB is set to the active mode and OP2B# output LOW when MCR[3] is set to a logic 1. INTB is set to the three state mode and OP2B# output HIGH when MCR[3] is set to a logic 0. See MCR[3]. This output should not be used as a general output else it will disturb the INTB output functionality.
ANCILLARY SIGNALS				
XTAL1	18	13	I	Crystal or external clock input. Caution: this input is not 5V tolerant.
XTAL2	19	14	O	Crystal or buffered clock output.
RESET	39	36	I	Reset (active high) - A longer than 40 ns HIGH pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (see External Reset Conditions).
VCC	44	42	Pwr	2.25V to 5.5V power supply. All input pins, except XTAL1, are 5V tolerant.
GND	22	17	Pwr	Power supply common, ground.
N.C.	none	12, 24, 25, 37		No Connection.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The XR16L2750 (2750) integrates the functions of 2 enhanced 16C550 Universal Asynchronous Receiver and Transmitter (UART). Each UART is independently controlled having its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 64-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, FIFO level counters, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 6.25 Mbps with 8X sampling clock rate or 3.125 Mbps in the 16X rate. The XR16L2750 is a 2.25 to 5.5V device with 5 volt tolerant inputs. The 2750 is fabricated with an advanced CMOS process.

Enhanced Features

The 2750 DUART provides a solution that supports 64 bytes of transmit and receive FIFO memory, instead of 128 bytes provided in the XR16C2850 and 16 bytes in the ST16C2550, or one byte in the ST16C2450. The 2750 is designed to work with low supply voltage and high performance data communication systems, that require fast data processing time. Increased performance is realized in the 2750 by the larger transmit and receive FIFOs, FIFO trigger level control, FIFO level counters and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C2550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2 Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 64 byte FIFO in the 2750, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU’s bandwidth requirement, increases performance, and reduces power consumption.

The 2750 supports a half-duplex output direction control signaling pin, RTS# A/B, to enable and disable the external RS-485 transceiver operation. It automatically switches the logic state of the output pin to the receive state after the last stop-bit of the last character has been shifted out of the transmitter. After receiving, the logic state of the output pin switches back to the transmit state when a data byte is loaded in the transmitter. The auto RS-485 direction control pin is not activated after reset. To activate the direction control function, user has to set FCTR Bit-3 to “1”. This pin is normally high for receive state, low for transmit state.

Data Rate

The 2750 is capable of operation up to 3.125 Mbps at 5V with 16X internal sampling clock rate, and 6.25 Mbps at 5V with 8X sampling clock rate. The device can operate with an external 24 MHz crystal on pins XTAL1 and XTAL2, or external clock source of up to 50 MHz on XTAL1 pin. With a typical crystal of 14.7456 MHz and through a software option, the user can set the prescaler bit for data rates of up to 1.84 Mbps.

The rich feature set of the 2750 is available through the internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features.

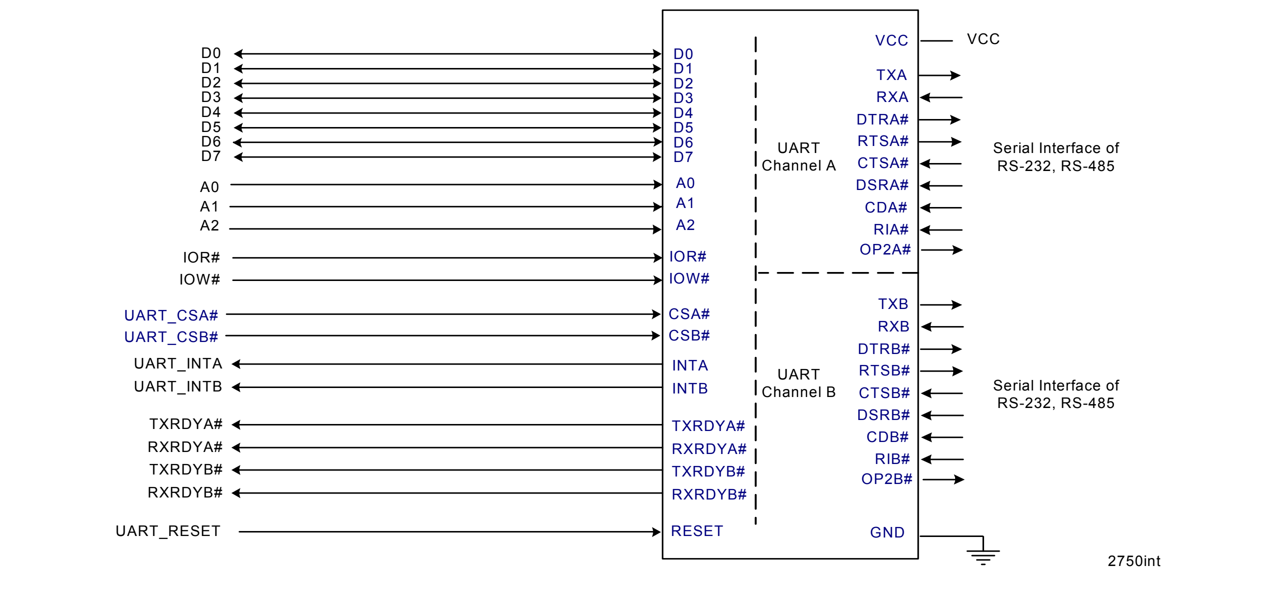
Following a power on reset or an external reset, the 2750 is software compatible with previous generation of UARTs, 16C450, 16C550 and 16C650A as well as the 16C850.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The 2750 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# signals. Both UART channels share the same data bus for host operations. The data bus interconnections are shown in Figure 3.

FIGURE 3. XR16L2750 DATA BUS INTERCONNECTIONS



2.2 5-Volt Tolerant Inputs

The 2750 can accept up to 5V inputs even when operating at 3.3V or 2.5V. But note that if the 2750 is operating at 2.5V, its V_{OH} may not be high enough to meet the requirements of the V_{IH} of a CPU or a serial transceiver that is operating at 5V. Caution: XTAL1 is not 5 volt tolerant.

2.3 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 16). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Device Identification and Revision

The XR16L2750 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x0A for the XR16L2750 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 Channel A and B Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. A logic 0 on chip select pins, CSA# or CSB#, allows the user to select UART channel A or B to configure, send transmit data and/or unload receive data to/from the UART. Selecting both UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from both uarts simultaneously. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A AND B SELECT

CSA#	CSB#	FUNCTION
1	1	UART de-selected
0	1	Channel A selected
1	0	Channel B selected
0	0	Channel A and B selected

2.6 Channel A and B Internal Registers

Each UART channel in the 2750 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550 and dual ST16C2550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible Scratchpad Register (SPR).

Beyond the general 16C2550 features and capabilities, the 2750 offers enhanced feature registers (EMSR, FLVL, EFR, Xon/Xoff 1, Xon/Xoff 2, FCTR, TRG, FC) that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, automatic RS-485 half-duplex direction output enable/disable, FIFO trigger level control, and FIFO level counters. All the register functions are discussed in full detail later in "Section 3.0, UART INTERNAL REGISTERS" on page 20.

2.7 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document doesn't mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A/B and TXRDY# A/B output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 2750 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the 2750 sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior. Also see Figures 18 through 23.

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY# A/B	LOW = 1 byte. HIGH = no data.	LOW = at least 1 byte in FIFO. HIGH = FIFO empty.	HIGH to LOW transition when FIFO reaches the trigger level, or time-out occurs. LOW to HIGH transition when FIFO empties.
TXRDY# A/B	LOW = THR empty. HIGH = byte in THR.	LOW = FIFO empty. HIGH = at least 1 byte in FIFO.	LOW = FIFO has at least 1 empty location. HIGH = FIFO is full.

2.8 INTA and INTB Outputs

The INTA and INTB interrupt output changes according to the operating mode and enhanced features setup. Table 3 and 4 summarize the operating behavior for the transmitter and receiver. Also see Figures 18 through 23.

TABLE 3: INTA AND INTB PINS OPERATION FOR TRANSMITTER

	AUTO RS485 MODE	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	NO	LOW = a byte in THR HIGH = THR empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty
INTA/B Pin	YES	LOW = a byte in THR HIGH = transmitter empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or transmitter empty

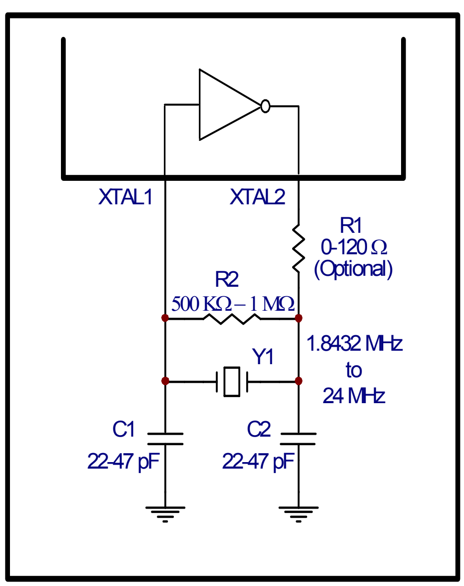
TABLE 4: INTA AND INTB PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	LOW = no data HIGH = 1 byte	LOW = FIFO below trigger level HIGH = FIFO above trigger level

2.9 Crystal Oscillator or External Clock Input

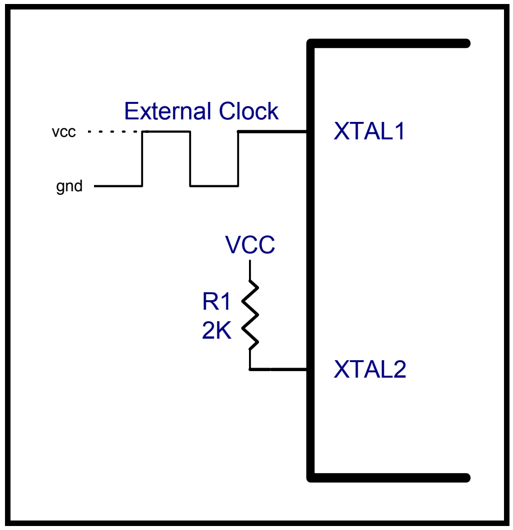
The 2750 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Please note that the input XTAL1 is not 5V tolerant and so the maximum at the pin should be VCC. For programming details, see “Programmable Baud Rate Generator.”

FIGURE 4. TYPICAL OSCILLATOR CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100 ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 4). The programmable Baud Rate Generator is capable of operating with a crystal oscillator frequency of up to 24 MHz. However, with an external clock input on XTAL1 pin and a 2K ohms pull-up resistor on XTAL2 pin (as shown in Figure 5) it can extend its operation up to 50 MHz (6.25 Mbps serial data rate) at 5V with an 8X sampling rate.

FIGURE 5. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE

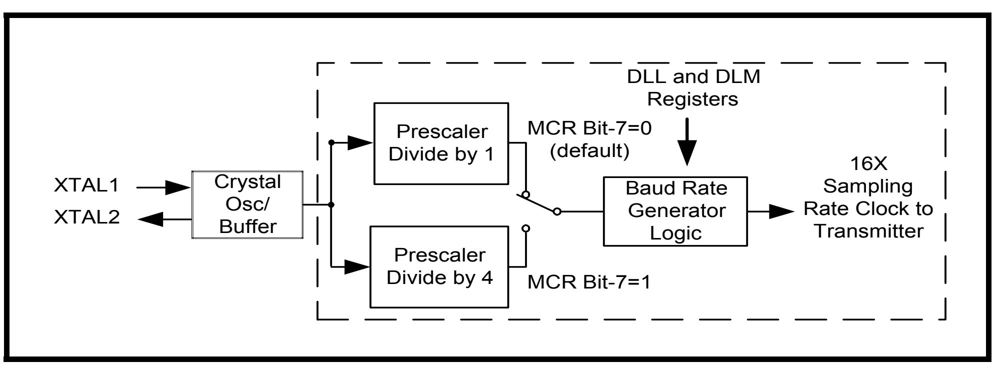


For further reading on the oscillator circuit please see the Application Note DAN108 on the EXAR web site at http://www.exar.com.

2.10 Programmable Baud Rate Generator

Each UART has its own Baud Rate Generator (BRG) with a prescaler. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling rate clock of the serial data rate. The sampling rate clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor defaults to the maximum baud rate (DLL = 0x01 and DLM = 0x00) upon power up.

FIGURE 6. BAUD RATE GENERATOR AND PRESCALER



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 5 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X sampling rate clock rate. A 16X sampling clock is typically used. However, user can select the 8X sampling clock rate mode (EMSR bit-7=0) to double the operating data rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), with 16XMode [EMSR bit-7] = 1
divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 8), with 16XMode [EMSR bit-7] = 0

TABLE 5: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0 (DEFAULT)	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

2.11 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X internal clock. A bit time is 16 (8) clock periods (see EMSR bit-7). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

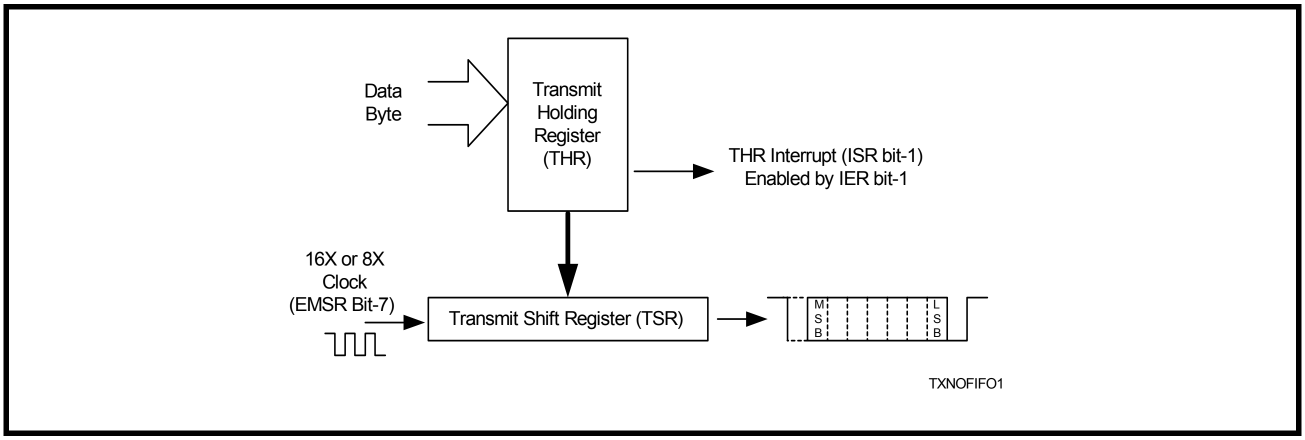
2.11.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.11.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

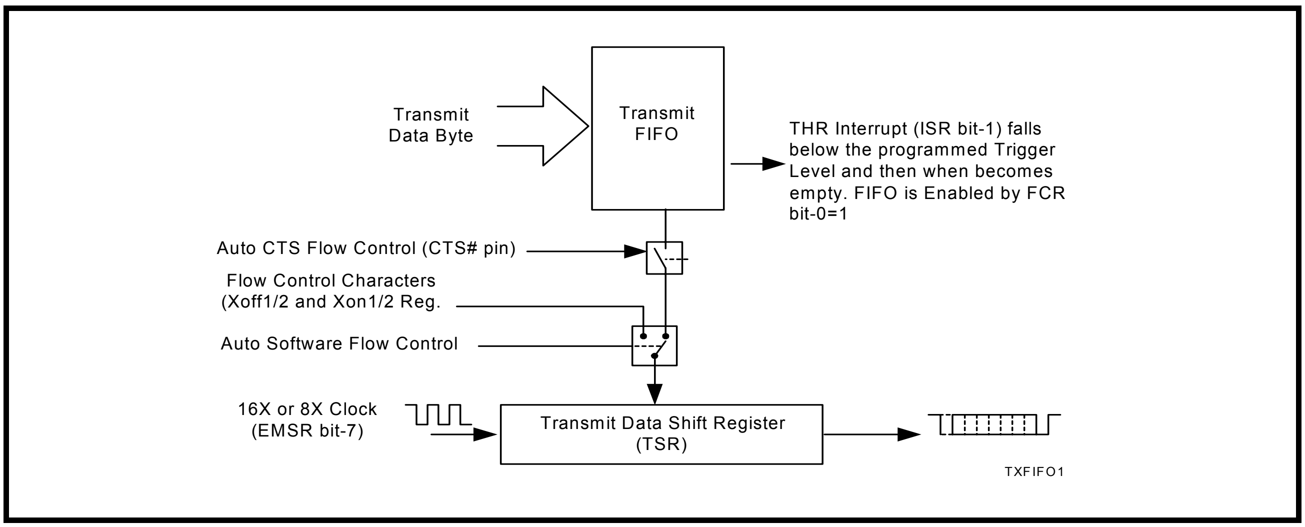
FIGURE 7. TRANSMITTER OPERATION IN NON-FIFO MODE



2.11.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 8. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.12 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X clock (EMSR bit-7) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X clock rate. After 8 clocks (or 4 if 8X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1,0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.12.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 9. RECEIVER OPERATION IN NON-FIFO MODE

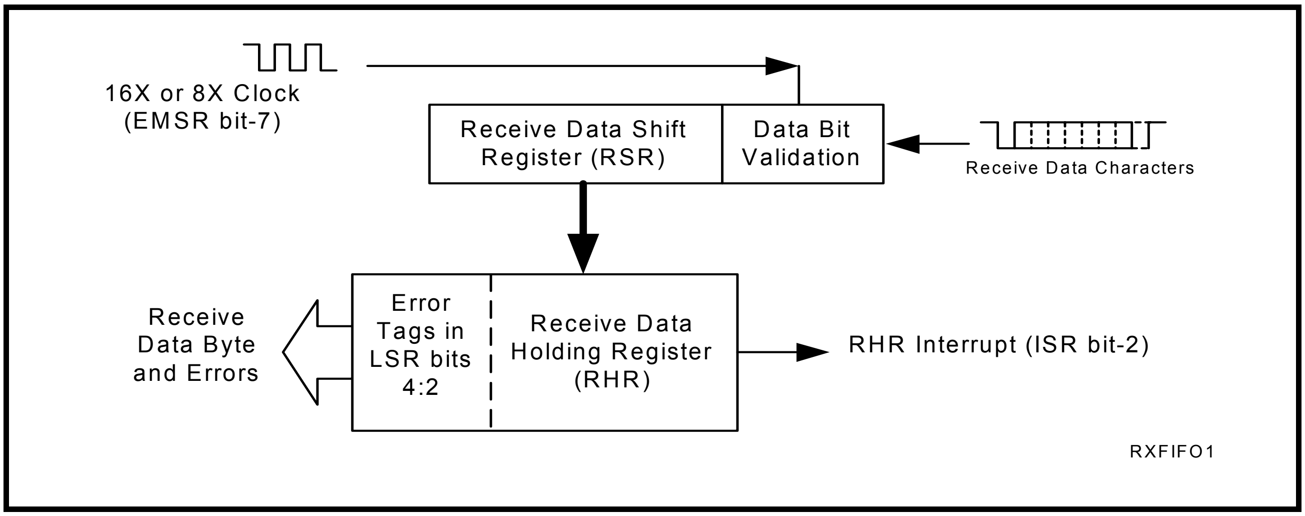
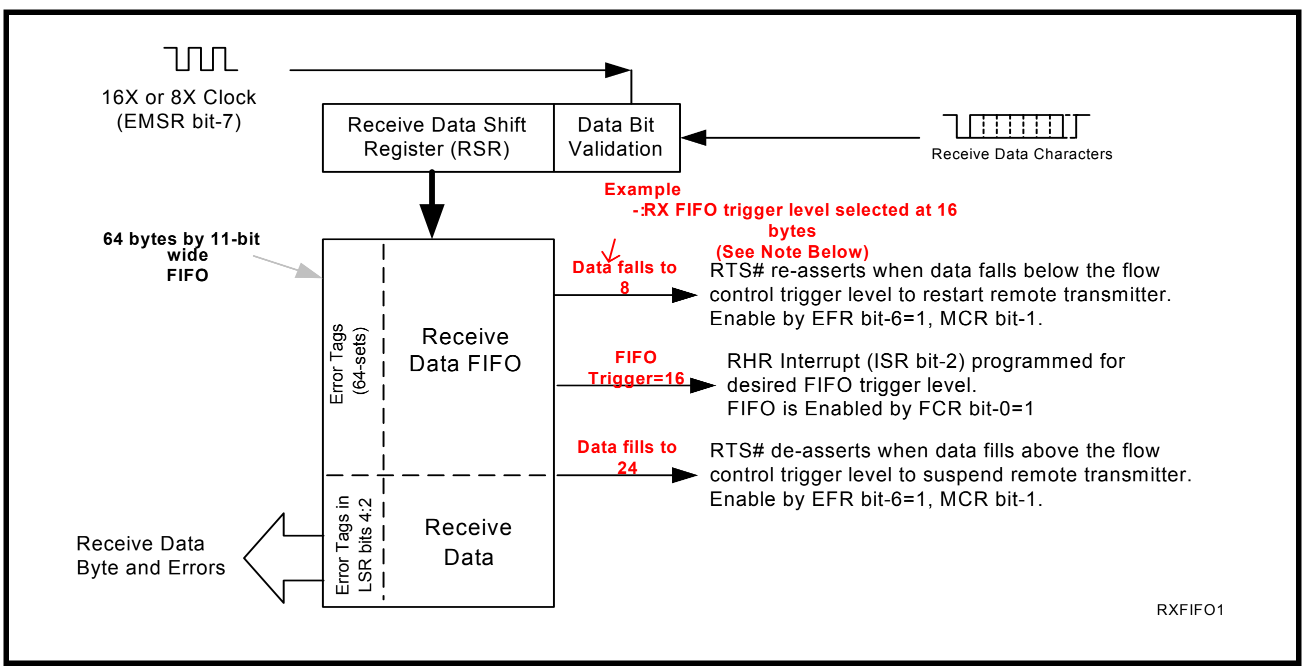


FIGURE 10. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: *Table-B selected as Trigger Table for Figure 10 (Table 10).*

2.13 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 11):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.14 Auto RTS Hysteresis

The 2750 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the XR16C850, ST16C650A and ST16C550 family of UARTs. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches the upper limit of the hysteresis level. The RTS# pin will return LOW after the RX FIFO is unloaded to the lower limit of the hysteresis level. Under the above described conditions, the 2750 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On). Table 13 shows the complete details for the Auto RTS# Hysteresis levels. Please note that this table is for programmable trigger levels only (Table D). The hysteresis values for Tables A-C are the next higher and next lower trigger levels in the corresponding table.

2.15 Auto CTS Flow Control

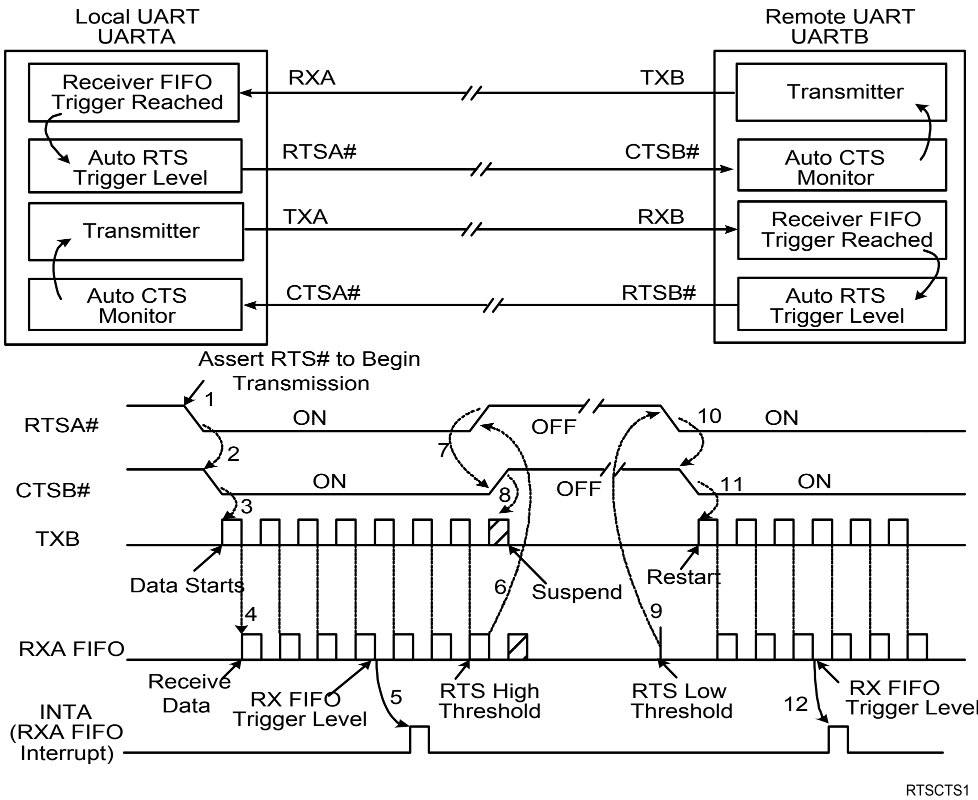
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see Figure 11):

- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 11. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.16 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 15), the 2750 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 2750 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the 2750 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the 2750 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 15) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 2750 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 2750 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 2750 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the 2750 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS Hysteresis value in Table 14. Table 6 below explains this when Trigger Table-B (See Table 10) is selected.

TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.*

2.17 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 2750 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

2.18 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit-3. By default, it de-asserts RTS# (HIGH) output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts RTS# (LOW) output prior to sending the data. The RS485 half-duplex direction control output can be inverted by enabling EMSR bit-3.

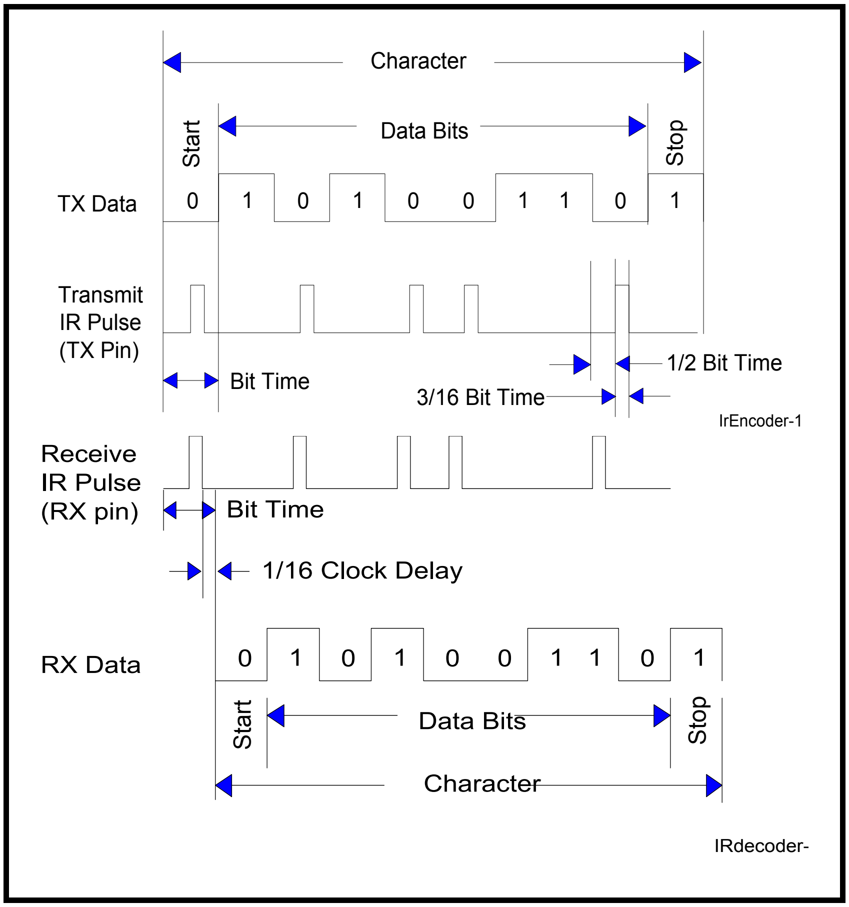
2.19 Infrared Mode

The 2750 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each "0" bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 12 below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a '1'. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see Figure 12.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream. However, this is not true with some infrared modules on the market which indicate a logic 0 by a light pulse. So the 2750 has a provision to invert the input polarity to accommodate this. In this case user can enable FCTR bit-2 to invert the input signal.

FIGURE 12. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.20 Sleep Mode with Auto Wake-Up

The 2750 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the 2750 to enter sleep mode:

- no interrupts pending for both channels of the 2750 (ISR bit-0 = 1)
- sleep mode of both channels are enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idling HIGH

The 2750 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 2750 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the 2750 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 2750 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from channel A or B. The 2750 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

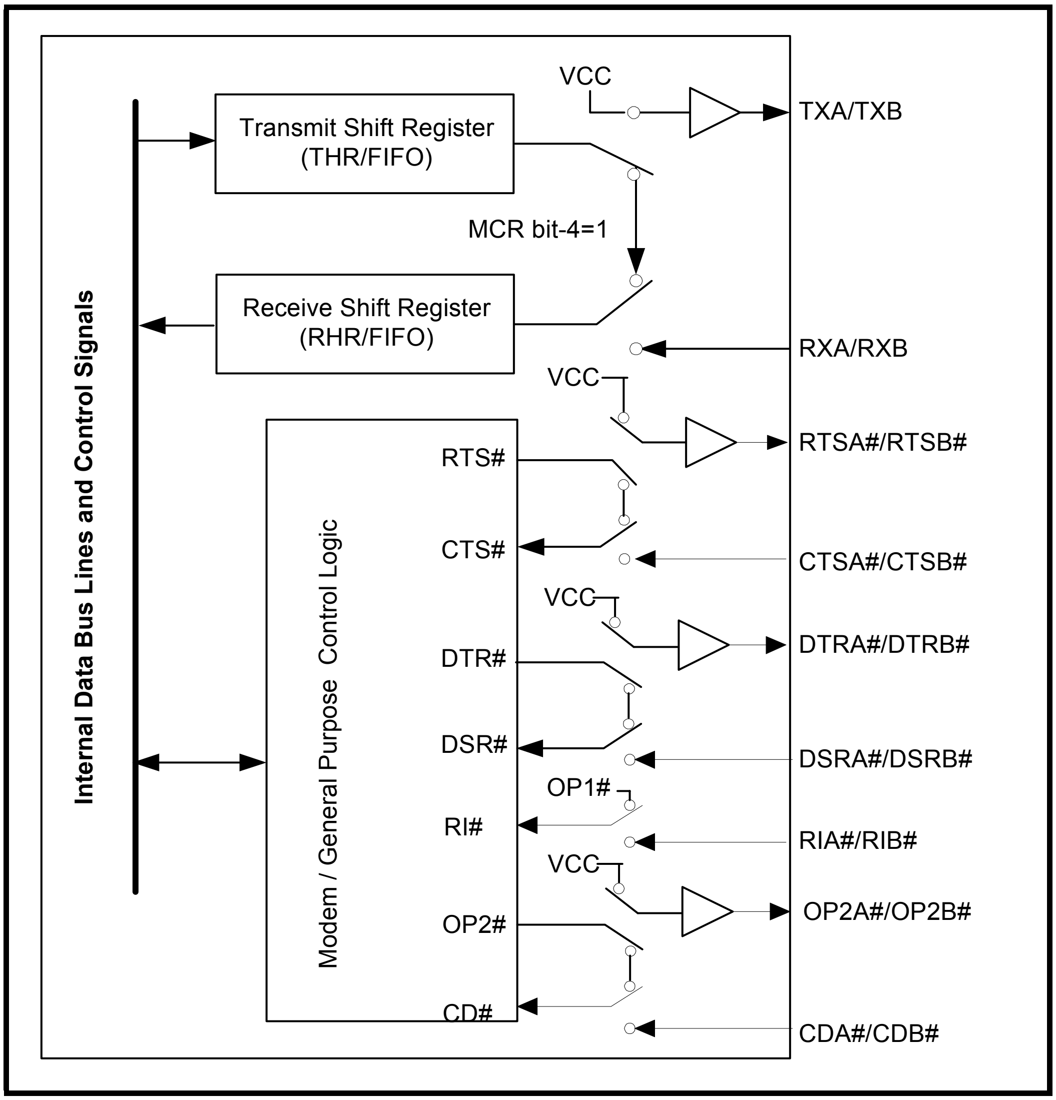
If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, and modem input lines remain steady when the 2750 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 37. If the input lines are floating or are toggling while the 2750 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current. As an alternative, please refer to the XR16L2751 which is pin-to-pin and software compatible with the 2750 but with (some additional pins and) the PowerSave feature that eliminates any unnecessary external buffer.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate. Also, it is important to keep RX A/B inputs idling HIGH or “marking” condition during sleep mode to avoid receiving a “break” condition upon the restart. This may occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the designer can use a 47k-100k ohm pull-up resistor on the RXA and RXB pins.

2.21 Internal Loopback

The 2750 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 13 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held while the CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input pin must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal. Also, Auto RTS/CTS flow control is not supported during internal loopback.

FIGURE 13. INTERNAL LOOP BACK IN CHANNEL A AND B



3.0 UART INTERNAL REGISTERS

Each of the UART channel in the 2750 has its own set of configuration registers selected by address lines A0, A1 and A2 with CSA# or CSB# selecting the channel. The complete register set is shown on Table 7 and Table 8.

TABLE 7: UART CHANNEL A AND B UART INTERNAL REGISTERS

ADDRESSES A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
	16C550 COMPATIBLE REGISTERS		
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low Byte	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Div Latch High Byte	Read/Write	
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR ≠ 0xBF
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register Reserved	Read-only Write-only	
1 1 0	MSR - Modem Status Register Reserved	Read-only Write-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR ≠ 0xBF, FCTR[6] = 0
1 1 1	FLVL - RX/TX FIFO Level Counter Register	Read-only	LCR ≠ 0xBF, FCTR[6] = 1
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	
	ENHANCED REGISTERS		
0 0 0	TRG - RX/TX FIFO Trigger Level Register FC - RX/TX FIFO Level Counter Register	Write-only Read-only	LCR = 0xBF
0 0 1	FCTR - Feature Control Register	Read/Write	
0 1 0	EFR - Enhanced Function Register	Read/Write	
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR $\neq$ 0xBF
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Mode ENable	0/ XonAny	Internal Lopback Enable	OP2#/INT Output Enable	Rsrvd (OP1#)	RTS# Output Control	DTR# Output Control	LCR $\neq$ 0xBF
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR $\neq$ 0xBF FCTR[6]=0
1 1 1	EMSR	WR	16X Sam-pling Rate Mode	LSR Error Inter-rupt. Imd/Dly#	Auto RTS Hyst. bit-3	Auto RTS Hyst. bit-2	Auto RS485 Output Inversion	Rsrvd	Rx/Tx FIFO Count	Rx/Tx FIFO Count	LCR $\neq$ 0xBF FCTR[6]=1
1 1 1	FLVL	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR≠0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	1	0	1	0	
Enhanced Registers											
0 0 0	TRG	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
0 0 0	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	FCTR	RD/WR	RX/TX Mode	SCPAD Swap	Trig Table Bit-1	Trig Table Bit-0	Auto RS485 Direction Control	RX IR Input Inv.	Auto RTS Hyst Bit-1	Auto RTS Hyst Bit-0	
0 1 0	EFR	RD/WR	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5]	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

See “Receiver” on page 12.

4.2 Transmit Holding Register (THR) - Write-Only

See “Transmitter” on page 11.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16L2750 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO (default). Instead, LSR bits 2-4 can be programmed to generate an interrupt immediately, by setting EMSR bit-6 to a logic 1.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt. (default)
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from low to high.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from low to high.

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 9, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty in auto RS-485 control).
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.
- CTS# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS flow control.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff interrupt is cleared by a read to ISR or when Xon character(s) is received.
- Special character interrupt is cleared by a read to ISR or after the next character is received.
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register.

TABLE 9: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or Special character)
7	1	0	0	0	0	0	CTS#, RTS# change of state
-	0	0	0	0	0	1	None (default)

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 9).

ISR[5:4]: Interrupt Status

These bits are enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s). Note that once set to a logic 1, the ISR bit-4 will stay a logic 1 until a Xon character is received. ISR bit-5 indicates that CTS# or RTS# has changed state.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.