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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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GENERAL DESCRIPTION

The XR16L651[1] (651) is a 2.25 to 5.5 volt Universal Asynchronous Receiver and Transmitter (UART) with 5 volt tolerant inputs. This device supports Intel and Motorola data bus interfaces and is software compatible to industry standard 16C450, 16C550, ST16C580 and ST16C650A UARTs.

The 651 has 32 bytes of TX and RX FIFOs and is capable of operating up to serial data rates of 3.125 Mbps at 5 volt supply voltage. The internal registers include the 16C550 register set plus Exar's enhanced registers for additional features to support today's highly demanding data communication needs. The enhanced features include automatic hardware and software flow control, selectable TX and RX trigger levels, and wireless infrared (IrDA) encoder/decoder.

The device provides a new capability to give user the ability to program the wireless infrared encoder output pulse width, hence reducing the power consumption of a handheld unit.

The XR16L651 device comes in a small 7x7x1mm 48-pin TQFP package in both the commercial and industrial temperature ranges.

NOTE: *1 Covered by US patents #5,649,122.*

FEATURES

Added feature in devices with top mark date code of "C2 YYWW" and newer:

- 0 ns address hold time

- 2.25 to 5.5 Volt Operation w/ 5 Volt Tolerant Inputs
- ST16C450/550/580/650A Software Compatible
- Intel, Motorola or PC Mode 8-bit Bus Interface
- Up to 3.125 Mbps Data Rate at 5 Volt Operation
- 32-byte Transmit and Receive FIFOs
- Automatic RS485 Half-Duplex Control Output
- Automatic Hardware (RTS/CTS) Flow Control
- Hardware Flow Control Hysteresis
- Automatic Software (Xon/Xoff) Flow Control
- Infrared (IrDA) Encoder/Decoder Enable Input
- Programmable Infrared Encoder Pulse Width
- Sleep Mode with Wake-up Indicator via interrupt

APPLICATIONS

- Battery Operated Electronics
- Internet Appliances
- Handheld Terminal
- Personal Digital Assistants
- Cellular Phones DataPort
- Wireless Infrared Data Communications Systems

FIGURE 1. BLOCK DIAGRAM

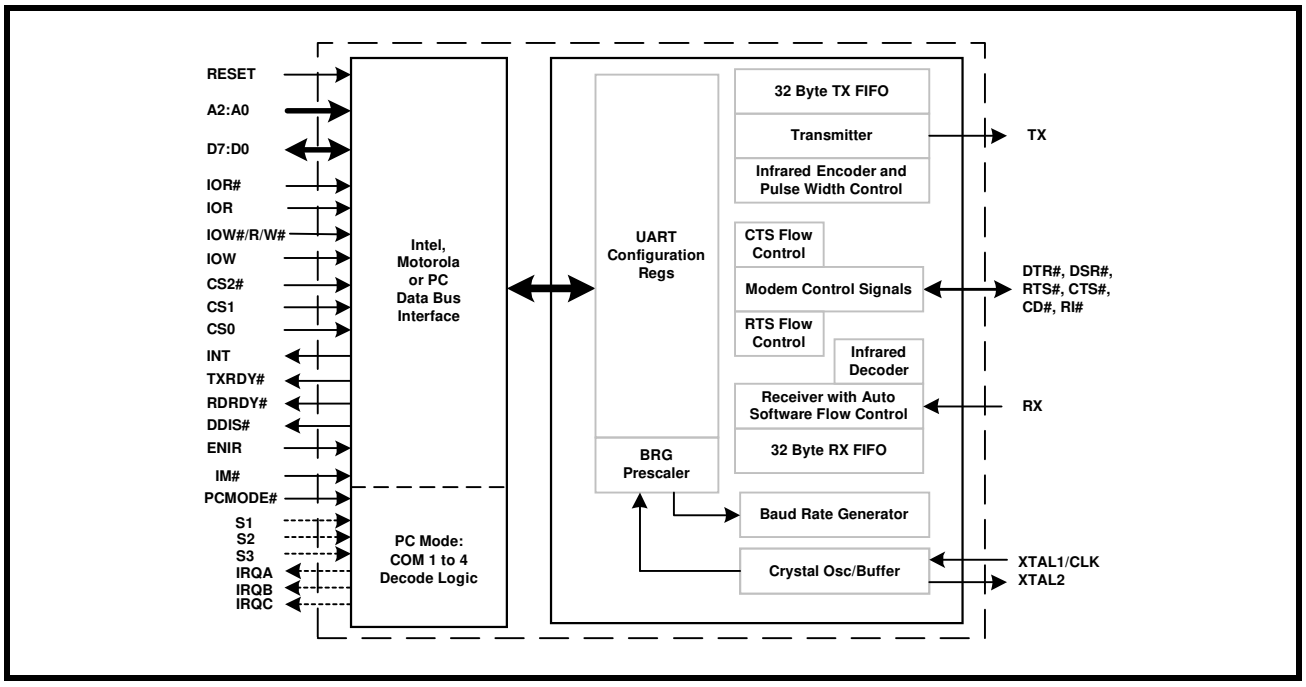
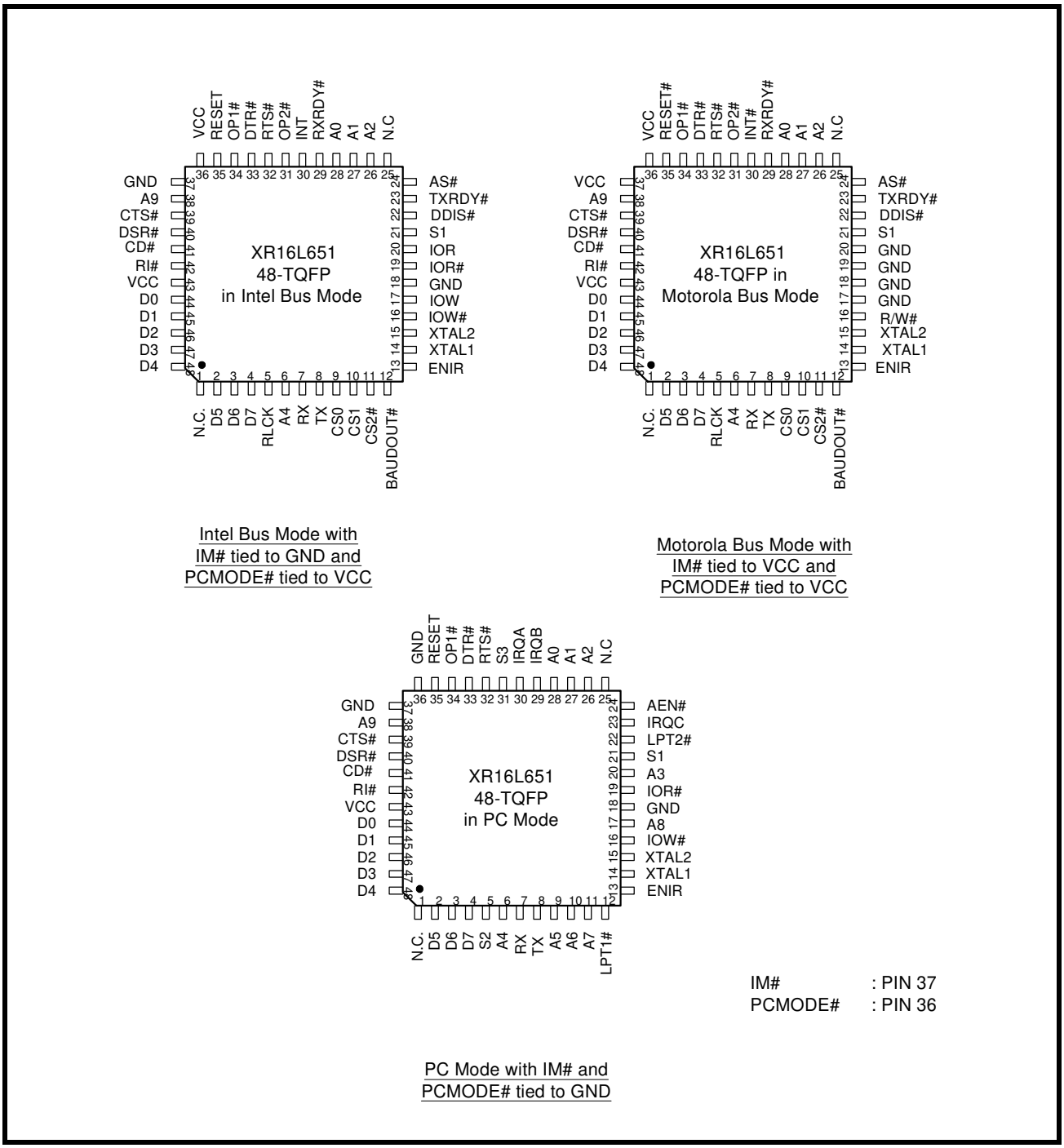


FIGURE 2. INTEL, MOTOROLA AND PC MODE PIN OUT



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16L651CM	48-Lead TQFP	0°C to +70°C	Active
XR16L651IM	48-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
16 (Intel) or 68 (Motorola) MODE DATA BUS INTERFACE. The PCMODE# pin is connected to VCC.			
A2 A1 A0	26 27 28	I	**Address bus lines [2:0]** A2:A0 selects internal UART's configuration registers.
D7 D6 D5 D4 D3 D2 D1 D0	4 3 2 48 47 46 45 44	IO	**Data bus lines [7:0] (bidirectional)**
IOR#	19	I	**Input/Output Read (active low)** When IM# pin is at logic 0, it selects Intel bus interface and this input is read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], places it on the data bus to allow the host processor to read it on the leading edge. When IM# pin is at logic 1, it selects Motorola bus interface and the IOR# input is not used and it should be connected to GND to minimize supply current. Its function is the same as IOR, except it is active low. Either an active IOR# or IOR is required to transfer data from 651 to CPU during a read operation. If this input is unused in the Intel bus mode (IM# pin is at logic 0), it should be connected to VCC to minimize supply current.
IOR	20	I	**Input/Output Read (active high)** Same as IOR# but active high. When IM# pin is at logic 1 for Motorola bus mode, this pin is not used and should be connected to GND to minimize supply current. If this input is unused in the Intel bus mode (IM# pin is at logic 0), it should be connected to GND to minimize supply current.
IOW# (R/W#)	16	I	**Input/Output Write (active low) - Intel bus mode** When IM# pin is at logic 0, it selects the Intel bus interface and this input becomes the write strobe (active low). The falling edge instigates the internal write cycle and the trailing edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0]. Its function is the same as IOW, except it is active low. Either an active IOW# or IOW is required to transfer data from 651 to the Intel type CPU during a write operation. If this input is unused (in the Intel bus mode), it should be connected to VCC to minimize supply current. **Read/Write Strobe - Motorola bus mode** When IM# pin is at logic 1, it selects Motorola bus interface and this input becomes R/W# signal for read (logic 1) and write (logic 0).
IOW	17	I	**Input/Output Write (active high)** Same as IOW# but active high. When IM# pin is at logic 1 for Motorola bus mode, this pin must be connected to GND to allow IOW# input to function correctly. If this input is unused in the Intel bus mode (IM# pin is at logic 0), it should be connected to GND to minimize supply current.

NAME	PIN #	TYPE	DESCRIPTION
CS0	9	I	**Chip Select 0 input (active high)** This input selects the XR16L651 device. If CS1 or CS2# is used as the chip select then this pin must be connected to VCC. The 651 is selected when all three chip selects are active. See Figure 3 through Figure 5.
CS1	10	I	**Chip Select 1 input (active high)** This input selects the XR16L651 device. If CS0 or CS2# is used as the chip select then this pin must be connected to VCC. The 651 is selected when all three chip selects are active. See Figure 3 through Figure 5.
CS2#	11	I	**Chip Select 2 input (active low)** This input selects the XR16L651 device. If CS0 or CS1 is used as the chip select then this pin must be connected to GND. The 651 is selected when all three chip selects are active. See Figure 3 through Figure 5.
INT (INT#)	30	O	**Interrupt Output** This output becomes active whenever the transmitter, receiver, line and/or modem status register has an active condition. See interrupt section for more details. When IM# pin is at logic 0 (Intel bus mode), this interrupt output may be set to normal active high or active high open source to provide wire-OR capability by connecting a 1k to 10k ohms resistor between this pin and ground. When IM# pin is at logic 1 (Motorola bus mode), this interrupt output becomes an open drain, active low output. It requires an external pull-up resistor of 1K-10K ohms to operate properly. The output may be wire-OR'ed with other devices in the system to form a single interrupt request to the host processor and have the software driver poll all devices to determine the interrupting condition(s).
AS#	24	I	**Address Strobe input (active low)** In the Intel bus mode, the leading-edge transition of AS# latches the chip selects (CS0, CS1, CS2#) and the address lines A0, A1 and A2. This input is used when the address lines are not stable for the duration of a read or write operation. In devices with top mark date code of "C2 YYWW" and newer, the address bus is latched even if this input is not used. These devices feature a '0 ns' address hold time. See "AC Electrical Characteristics" . If not required, this input can be permanently tied to GND. This input is not used in the Motorola mode.
TXRDY#	23	O	**UART Transmitter Ready (active low)** The output provides the TX FIFO/THR status. See Table 2. If it is not used, leave it unconnected.
RXRDY#	29	O	**UART Receiver Ready (active low)** This output provides the RX FIFO/RHR status for receive channel A. See Table 2. If it is not used, leave it unconnected.
PC Mode Interface Signals. Connect PCMODE# pin to GND and IM# pin to GND to select PC Mode.			
A3 A4 A5 A6 A7 A8 A9	20 6 9 10 11 17 38	I	**PC mode additional Address Lines** In the PC mode, these are the additional address lines from the host address bus. They are inputs to the on-board chip select decode function for COM 1-4 and LPT ports. See Table 1 for details. The pins A4 and A9 have internal 100kΩ pull-up resistors.

NAME	PIN #	TYPE	DESCRIPTION
AEN#	24	I	**Address Enable input (active low)** When AEN# transition to logic 0, it decodes and validates COM 1-4 ports address per S1, S2 and S3 inputs.
S1 S2 S3	21 5 31	I	**Select 1 to 3** These are the standard PC COM 1-4 ports and IRQ selection inputs. See Table 1 and Table 3 for details. The S1 pin has an internal 100kΩ pull-up resistor.
IRQA IRQB IRQC	30 29 23	O	**Interrupt Request A, B and C Outputs (active high, tri-state)** These are the interrupt outputs associated with COM 1-4 to be connected to the host data bus. See interrupt section for details. The Interrupt Requests A, B or C functions as IRQx to the PC bus. IRQx is enabled by setting MCR bit-3 to logic 1 and the desired interrupt(s) in the interrupt enable register (IER).
LPT1#	12	O	**Line Printer Port-1 Decode Logic Output (active low)** This pin functions as the PC standard LPT-1 printer port address decode logic output, see Table 1. The baud rate generator clock output, BAUDOUT#, is internally connected to the RCLK input in the PC mode.
LPT2#	22	O	**Line Printer Port-2 Decode Logic Output (active low)** This pin functions as the PC standard LPT-2 printer port address decode logic output, see Table 1.
MODEM OR SERIAL I/O INTERFACE			
TX	8	O	**Transmit Data or wireless infrared transmit data** This output is active low in normal standard serial interface operation (RS-232, RS-422 or RS-485) and active high in the infrared mode. Infrared mode can be enabled by connecting pin ENIR to VCC or through software setting after power up.
RX	7	I	**Receive Data or wireless infrared receive data** Normal received data input idles at logic 1 condition and logic 0 in the infrared mode. The wireless infrared pulses are applied to the decoder. This input must be connected to its idle logic state in either normal, logic 1, or infrared mode, logic 0, else the receiver may report “receive break” and/or “error” condition(s).
RTS#	32	O	**Request to Send or general purpose output (active low)** This port may be used for one of two functions: 1) automatic hardware flow control, see EFR bit-6, MCR bit-1and IER bit-6. 2) RS485 half-duplex direction control, see XFR bits 2 and 5. RTS# output must be asserted before auto RTS flow control can start.
CTS#	39	I	**Clear to Send or general purpose input (active low)** If used for automatic hardware flow control, data transmission will be stopped when this pin is de-asserted and will resume when this pin is asserted again. See EFR bit-7 and IER bit-7.
DTR#	33	O	**Data Terminal Ready or general purpose output (active low)**
DSR#	40	I	**Data Set Ready input or general purpose input (active low)**
CD#	41	I	**Carrier Detect input or general purpose input (active low)**
RI#	42	I	**Ring Indicator input or general purpose input (active low)**
ANCILLARY SIGNALS			

NAME	PIN #	TYPE	DESCRIPTION
XTAL1	14	I	**Crystal or external clock input. Caution: this input is not 5V tolerant.**
XTAL2	15	O	**Crystal or buffered clock output**
RCLK	5	I	**Receiver Clock** This input is used as external 16X clock input to the receiver section. Connect the BAUDOUT# pin to this input externally.
BAUDOUT#	12	O	**Baud Rate Generator Output (active low)** This pin provides the 16X clock of the selected data rate from the baud rate generator. The RCLK pin must be connected externally to BAUDOUT# when the receiver is operating at the same data rate. When the PC mode is selected, the baud rate generator clock output is internally connected to the RCLK input. This pin then functions as the LPT-1 printer port decode logic output, see Table 3.
PCMODE#	36	I	**PC Mode Select (active low)** When this input is at logic 0, it enables the on-board chip select decode function according to PC ISA bus COM[4:1] and IRQ[4:3] port definitions. See Table 3 for details. This pin has an internal 100kΩ pull-up resistor.
DDIS#	22	O	**Drive Disable Output** This pin goes to a logic 0 whenever the host CPU is reading data from the 651. It can control the direction of a data bus transceiver between the CPU and 651 or other logic functions.
ENIR	13	I	**Enable Infrared Mode (active high)** This pin can be used to start up the UART in wireless infrared mode. This input is sampled when the reset input signal (RESET or RESET#) is deasserted. The TX output would idle at logic 0 instead of normal logic 1. The software infrared enable bit (MCR bit-6) will have full enable/disable control after the power up.
RESET (RESET#)	35	I	**Reset Input** A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held at logic 1 (if ENIR pin is at a logic 0), the receiver input will be ignored and outputs are reset. See UART Reset Conditions in Table 13. When IM# pin is at a logic 0, Intel bus mode, reset input is active high. When IM# pin is at a logic 1, Motorola bus mode, reset input is active low.
IM#	37	I	**Intel or Motorola data bus interface select** A logic 0 selects Intel bus interface and a logic 1 selects Motorola interface. This input affects the functionality of IOR#, IOW#, CS# and INT pins.
OP1#	34	O	**Output Port 1** General purpose output.
OP2#	31	O	**Output Port 2** General purpose output.
VCC	43	Pwr	**2.25V to 5.5V supply voltage** All inputs, except XTAL1, are 5V tolerant.
GND	18	Pwr	**Power supply common ground.**
NC	1,25	-	**No Connect**

Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The XR16L651 (651) is an industry first multi-voltage UART that can operate from 2.25V to 5.5V power supplies. Its inputs are 5V tolerant to facilitate interconnection to transceiver devices of RS-232, RS-422 or RS-485. The 651 is software compatible to the industry standard 16C550 with some additional enhanced features.

The 651 provides serial asynchronous receive data synchronization, parallel-to-serial data conversion for the transmitter section and serial-to-parallel data conversions for receiver section. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmitted data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The XR16L651 represents such an integration with greatly enhanced features. The 651 is fabricated with an advanced CMOS process.

The 651 supports standard 8-bit Intel, Motorola or PC bus interfaces through 2 input selection pins. The Intel bus uses separate input/output read and write signals for all bus transactions while the Motorola bus uses a read/write signal and chip select to conduct the same transactions. The PC bus mode associates with the PC ISA bus and follow the industry standard PC definitions for COM 1-4 serial port addresses. The 651 includes on-board chip select decode logic and selection for the proper interrupt request. This eliminates the need for an external logic array device.

The 651 has 32-bytes each of transmit and receive FIFOs, automatic RTS/CTS hardware flow control with hysteresis, automatic Xon/Xoff and special character software flow control, selectable transmit and receive FIFO trigger levels, wireless infrared encoder and decoder (IrDA ver. 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rates up to 3.125 Mbps with a 16X sampling clock rate.

The 651 is an upward solution that provides 32 bytes of transmit and receive FIFO memory, instead of 16 bytes provided in the 16C550, or none in the 16C450. The 651 is designed to work with high speed communication devices, that require fast data processing time. Increased performance is realized in the 651 by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the standard ST16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 32 byte FIFO in the 651, the data buffer will not require unloading/loading for 3.05 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The rich feature set of the 651 is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/ decoder interface, modem interface controls, and a sleep mode are all standard features. In the PC mode, two tri-state interrupt lines (IRQB and IRQC) and one selectable open source interrupt output (IRQA) are available. The open source interrupt scheme allows multiple interrupts to be combined in a “wire-OR” operation, thus reducing the number of interrupt lines in larger systems. Following a power on reset or an external reset, the 651 is software compatible with previous generation of UARTs, 16C450, 16C550 and ST16C650A.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Host Data Bus Interface

The host interface is 8 data bits wide with 3 address lines and control signals to execute bus read and write transactions. The 651 supports 3 type of host interfaces: Intel, Motorola and PC mode. The Intel and Motorola interfaces provide support for their respective microcontroller or processor. This facilitates the hardware design and interconnections. The Intel bus interface is selected by connecting IM# to logic 0 and PCMODE# to logic 1. The Intel bus interconnections are shown in Figure 3. The Motorola bus is selected with the IM# input connected to logic 1 and PCMODE# input ties to logic 1. The Motorola bus interconnections are shown in Figure 4. The special PC mode is selected when IM# and PCMODE# are connected to logic 0. The PC mode interconnections are shown in Figure 5.

FIGURE 3. XR16L651 INTEL BUS INTERCONNECTIONS

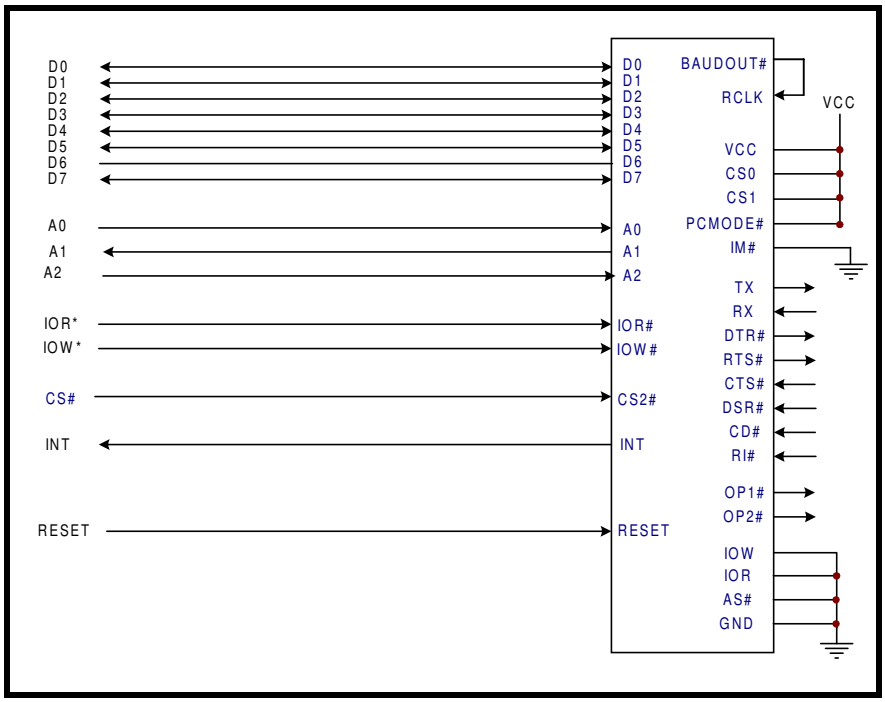


FIGURE 4. XR16L651 MOTOROLA BUS INTERCONNECTIONS.

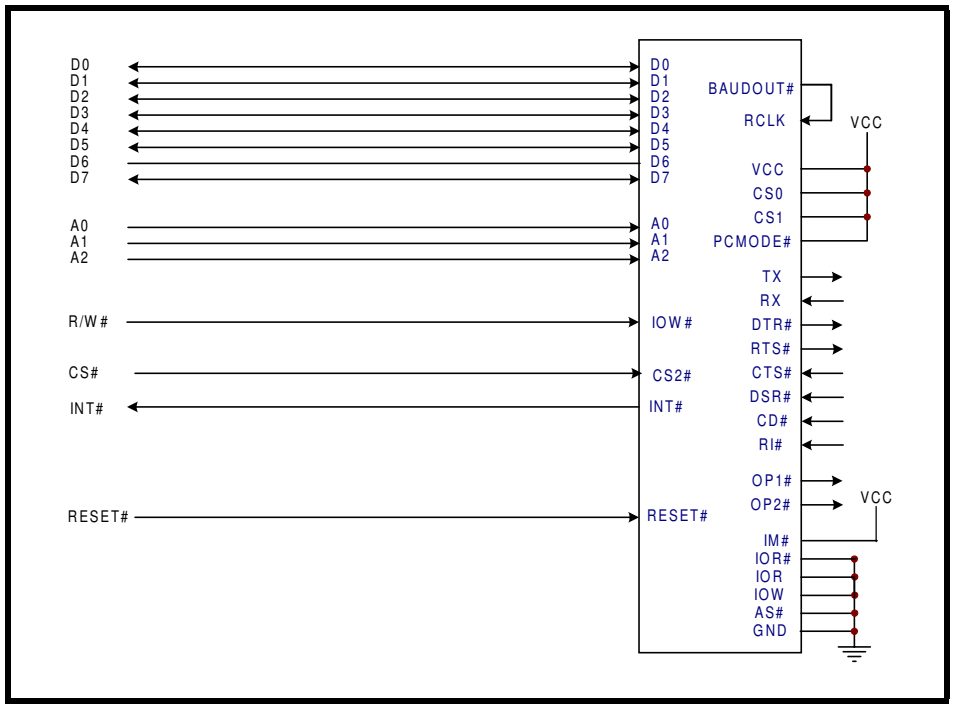
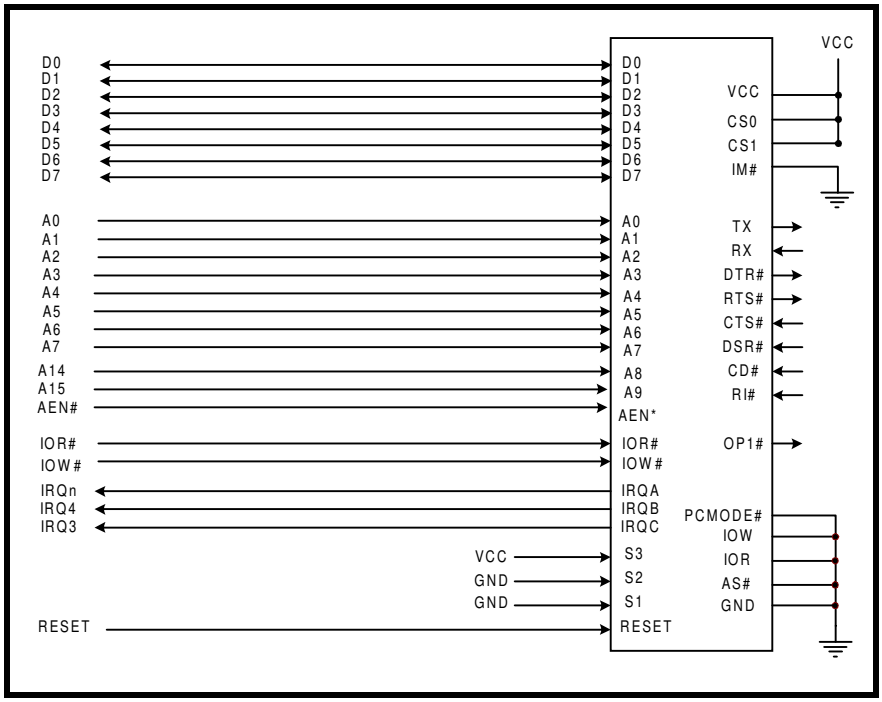


FIGURE 5. XR16L651 PC MODE INTERCONNECTIONS



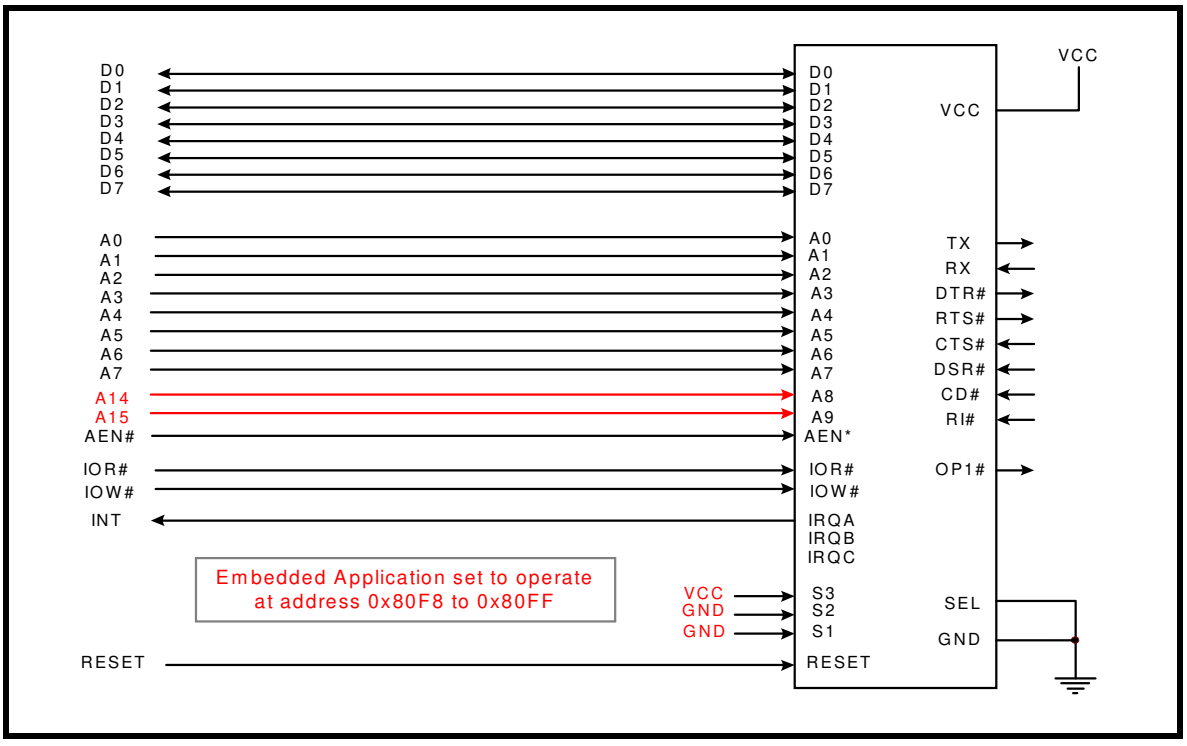
2.1.1 PC MODE

The PC mode interface includes an on-chip address decoder and interrupt selection function for the standard PC COM 1-4 port addresses. The selection is made through three input signals: S1, S2 and S3. The selection summary is shown in Table 1. Although the on-chip address decoder was designed for PC applications ranging from 0x278 to 0x3FF, it can fit into an embedded applications by offsetting the address lines to the 651. An example is shown in Figure 6 where the UART is operating from 0x80F8 to 0x80FF address space. Operating in the PC mode eliminates external address decode components.

TABLE 1: PC MODE INTERFACE ON-CHIP ADDRESS DECODER AND INTERRUPT SELECTION.

PCMODE# INPUT	S3, S2, S1 INPUTS	A9-A3 ADDRESS LINES TO ON-CHIP DECODER	COM/LPT PORT SELECTION	IRQ OUTPUT SELECTION
0	0 0 0	0x3F8 - 0x3FF	COM-1	IRQB (for PC's IRQ4)
0	0 0 1	0x2F8 - 0x2FF	COM-2	IRQC (for PC's IRQ3)
0	0 1 0	0x3E8 - 0x3EF	COM-3	IRQB (for PC's IRQ4)
0	0 0 0	0x3F8 - 0x3FF	COM-4	IRQB (for PC's IRQ4)
0	1 0 0	0x2F8 - 0x2FF	COM-1	IRQA (for PC's IRQn
0	1 0 1	0x3E8 - 0x3EF	COM-2	IRQA (for PC's IRQn)
0	1 1 0	0x2E8 - 0x2EF	COM-3	IRQA (for PC's IRQn)
0	1 1 1	0x3F8 - 0x3FF	COM-4	IRQA (for PC's IRQn)
0	- - -	0x278 - 0x27F	LPT-2	N/A
0	- - -	0x378 - 0x37F	LPT-1	N/A

FIGURE 6. PC MODE INTERFACE IN AN EMBEDDED APPLICATION.



2.2 5-Volt Tolerant Inputs

The 651 can acccept up to 5V inputs even when operating at 3.3V or 2.5V. But note that if the 651 is operating at 2.5V, its V_{OH} may not be high enough to meet the requirements of the V_{IH} of a CPU or a serial transceiver that is operating at 5V. Caution: XTAL1 is not 5 volt tolerant.

2.3 Device Reset

The RESET input resets the internal registers and the serial interface outputs to their default state (see Figure 13). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Device Identification and Revision

The XR16L651 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x04 for the XR16L651 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document does not mean “direct memory access” but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# and TXRDY# output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 651 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the 651 sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior. Also see Figures 26 through 31.

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR BIT-3 = 0 (DMA MODE DISABLED)	FCR BIT-3 = 1 (DMA MODE ENABLED)
RXRDY#	0 = 1 byte. 1 = no data.	0 = at least 1 byte in FIFO 1 = FIFO empty.	1 to 0 transition when FIFO reaches the trigger level, or timeout occurs. 0 to 1 transition when FIFO empties.
TXRDY#	0 = THR empty. 1 = byte in THR.	0 = FIFO empty. 1 = at least 1 byte in FIFO.	0 = FIFO has at least 1 empty location. 1 = FIFO is full.

2.6 Interrupt

The output function of interrupt, INT, output changes according to the operating bus type and various factors. Table 3 summarizes its behavior in Intel, Motorola and PC mode of operation. Multiple interrupts can be wire-OR'ed. This is accomplished by setting MCR bit-5 to a logic 1 and connecting a 1KΩ to 10KΩ resistor between this pin and ground to provide an acceptable logic 0 level.

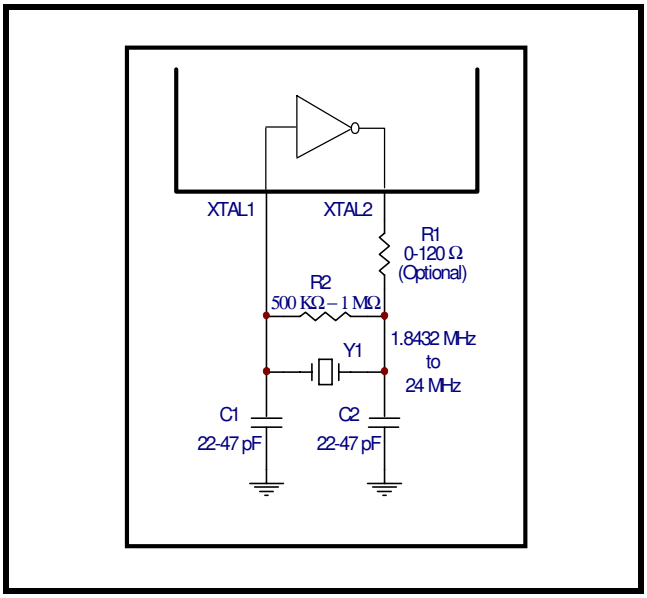
TABLE 3: INTERRUPT OUTPUT (INT, INT# AND IRQA) FUNCTIONS

IM# INPUT (INTEL/ MOTOROLA)	PCMODE# INPUT	S3 INPUT	MCR BIT-5 (INT TYPE SELECT)	MCR BIT-3 (IRQN ENABLE)	INTERRUPT OUTPUT (INT, INT# OR IRQA)
Intel Bus Mode					
0	1	don't care	0	don't care	INT is logic 0 for inactive interrupt. INT is logic 1 for active interrupt (active high)
0	1	don't care	1	don't care	INT is three-state for inactive interrupt INT is logic 1 for active interrupt (open source). Requires a 1K-10KΩ resistor to GND.
Motorola Bus Mode					
1	1	don't care	0	don't care	INT# is three-state for inactive interrupt. INT# is logic 0 for active interrupt (active low, open drain). Requires a 1K-10KΩ resistor to VCC.
1	1	don't care	1	don't care	INT# is three-state.
PC Mode					
0	0	0	don't care	don't care	IRQA is three-state. Either IRQB or IRQC is used, see Table 1.
0	0	1	don't care	0	IRQA is three-state.
0	0	1	0	1	IRQA is logic 0 for inactive interrupt. IRQA is logic 1 for active interrupt (active high).
0	0	1	1	1	IRQA is three-state for no interrupt. IRQA is logic 1 for active interrupt (active high, open source).

2.7 Crystal Oscillator or External Clock

The 651 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Caution if external clock is used: XTAL1 input is not 5 Volt tolerant. For programming details, see "Programmable Baud Rate Generator."

FIGURE 7. TYPICAL OSCILLATOR CONNECTIONS

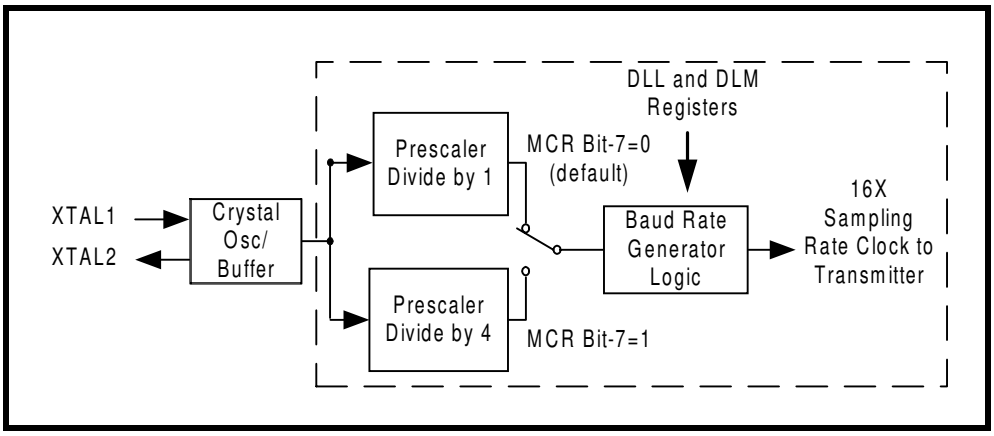


The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100 ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 7). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typically, the oscillator connections are shown in Figure 7. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.8 Programmable Baud Rate Generator

The UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up or a reset. Therefore, the BRG must be programmed during initialization to the operating data rate.

FIGURE 8. BAUD RATE GENERATOR



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 4 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 4: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

2.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 32 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

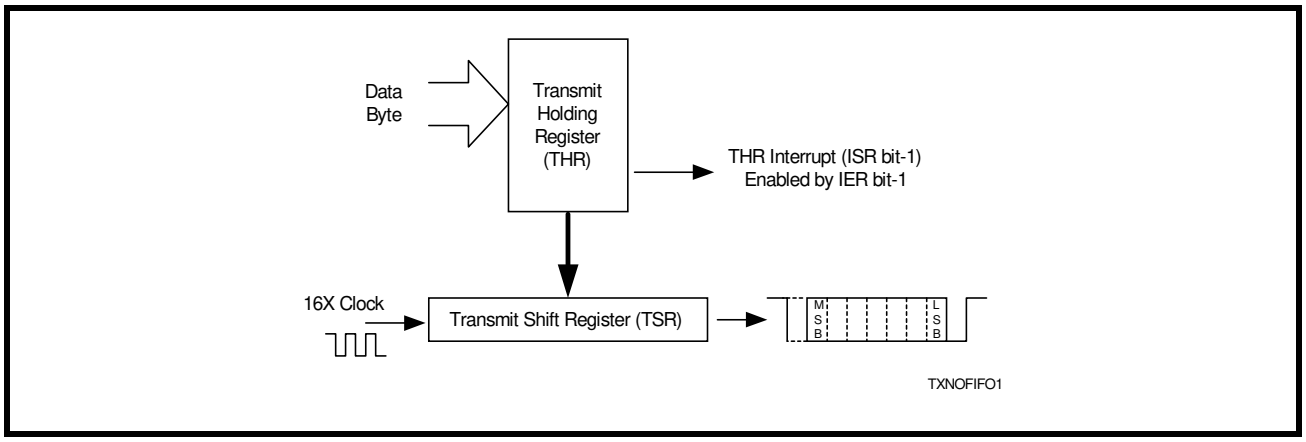
2.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including a start bit, data bits, parity bit and stop bit(s). The least-significant-bit (Bit-0) is the first data bit to go out. The THR is the input register to the transmit FIFO of 32 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

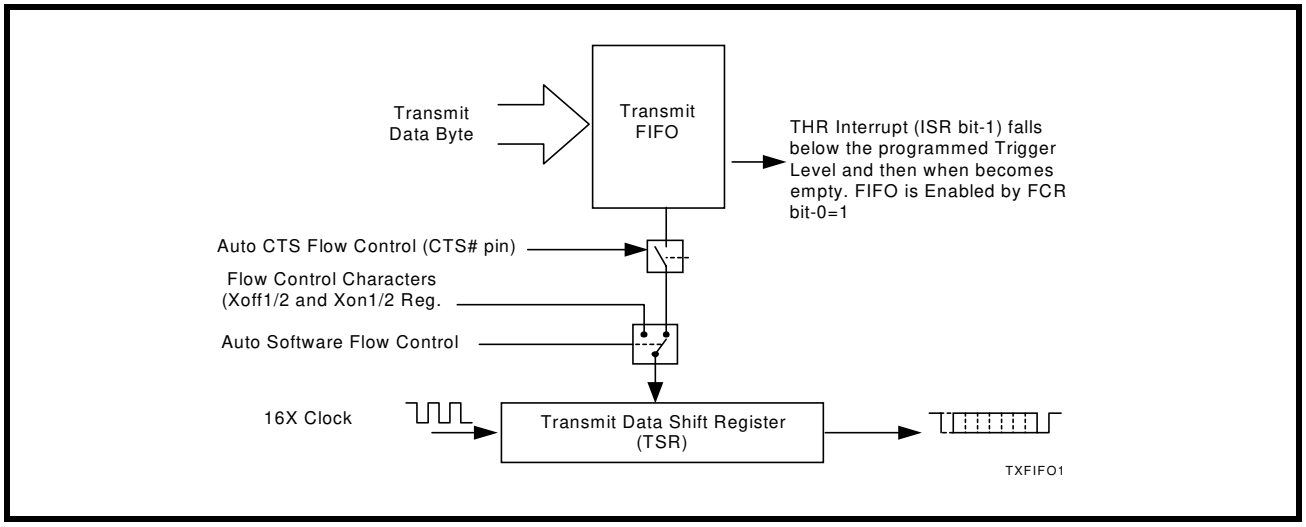
FIGURE 9. TRANSMITTER OPERATION IN NON-FIFO MODE



2.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 32 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 10. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 32 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in the RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level (XFR bit-3). Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 32 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 11. RECEIVER OPERATION IN NON-FIFO MODE

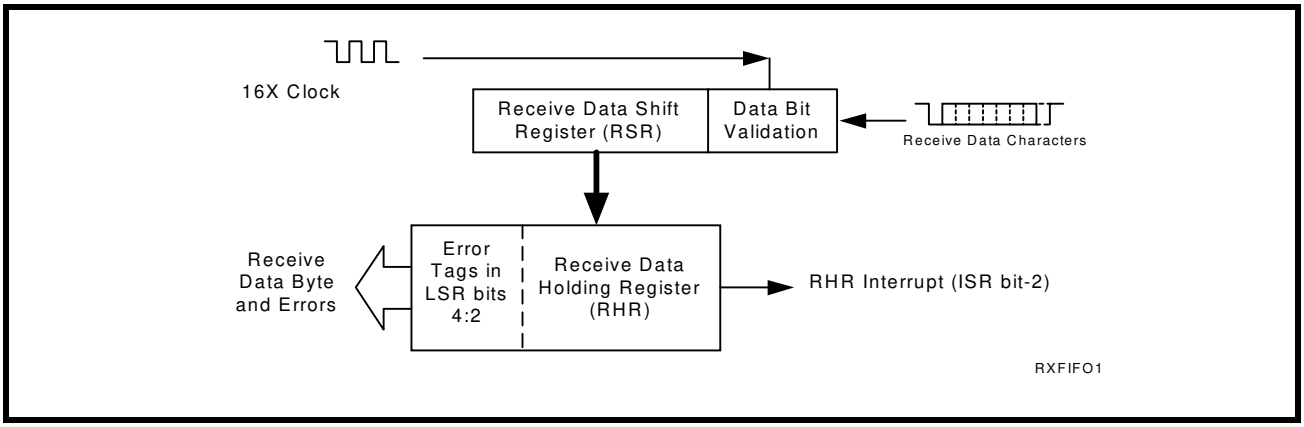
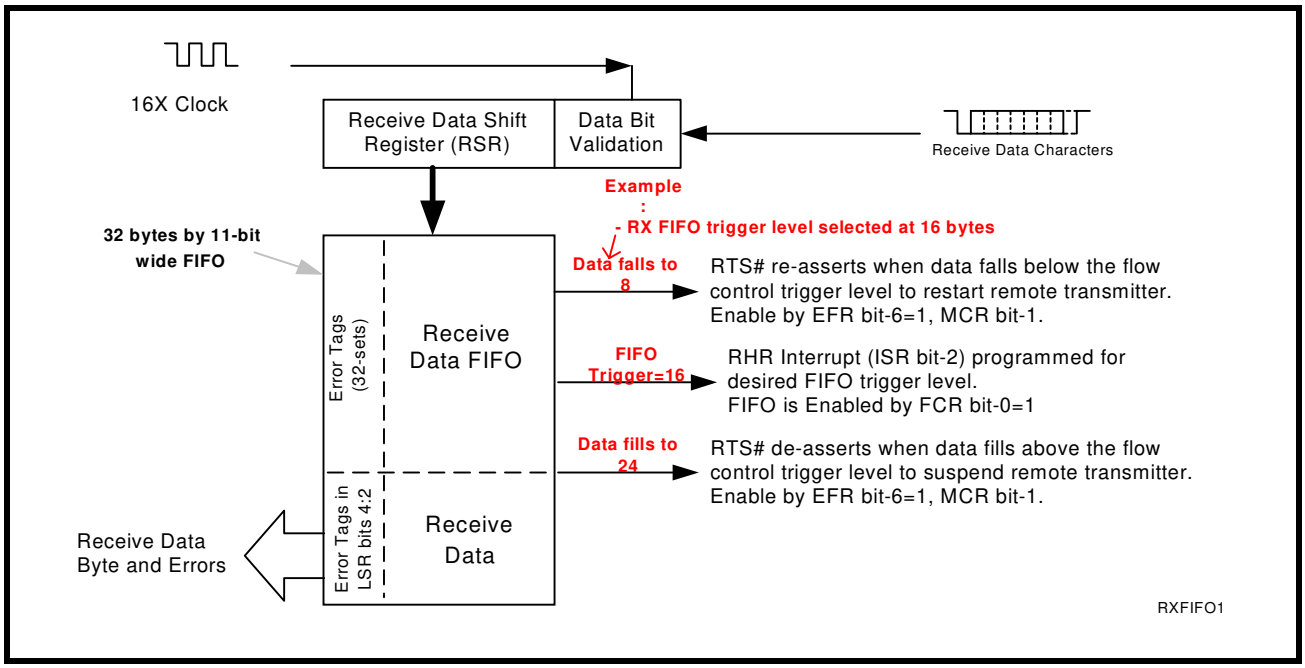


FIGURE 12. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.11 Automatic RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 13):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS output pin (MCR bit-1 to logic 1 after it is enabled).

With the Auto RTS function enabled, the RTS# output pin will not be de-asserted (logic 1) when the receive FIFO reaches the programmed trigger level, but will be de-asserted when the FIFO reaches the next trigger level (See Table 10). The RTS# output pin will be asserted again after the FIFO is unloaded to the next trigger level below the programmed trigger level. However, even under these conditions, the 651 will continue to accept data until the receive FIFO is full if the remote UART transmitter continues to send data.

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin is de-asserted (logic 1) during Auto RTS flow control mode: ISR bit-5 will be set to logic 1.

2.12 Auto CTS Flow Control

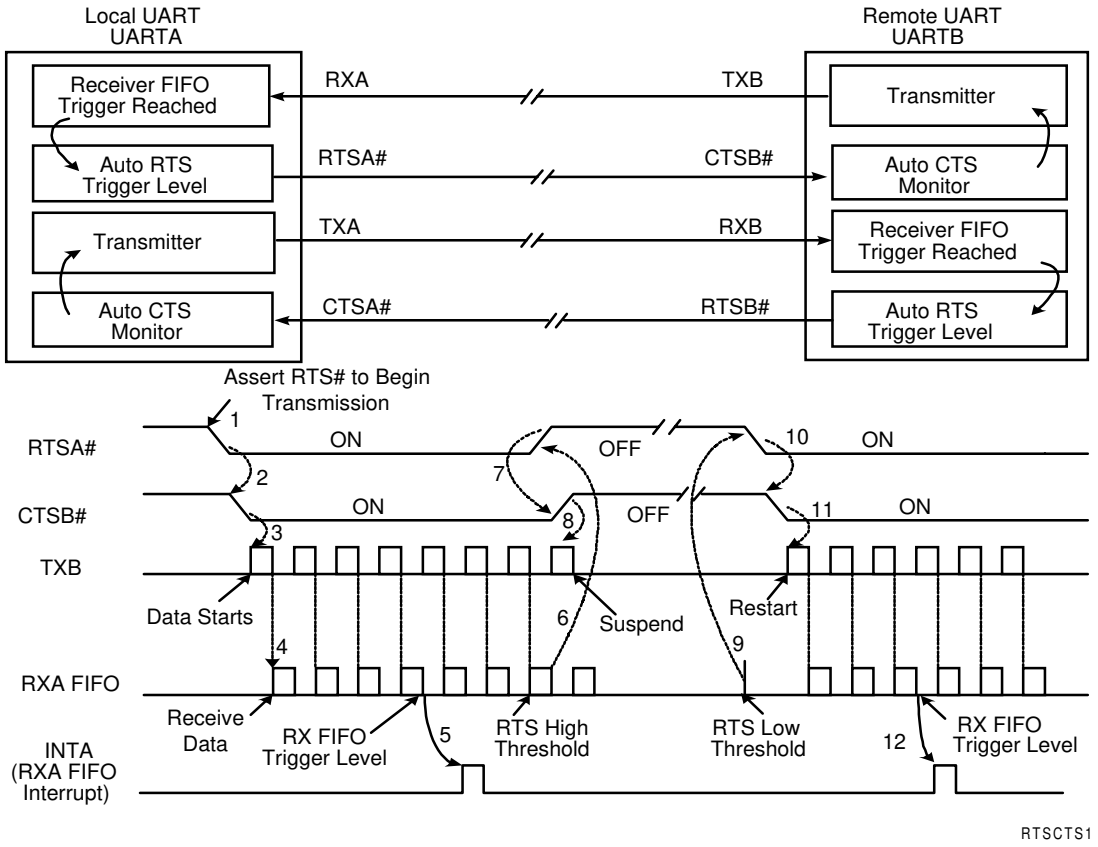
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see Figure 13):

- Enable auto CTS flow control using EFR bit-7.

With the Auto CTS function enabled, the UART will suspend transmission as soon as the stop bit of the character in the Transmit Shift Register has been shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1) during Auto CTS flow control mode: ISR bit-5 will be set to 1.

FIGURE 13. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.13 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 12), the 651 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If received character(s) (RX) match the programmed values, the 651 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character values, the 651 will monitor the receive data stream for a match to the Xon-1,2 character value(s). If a match is found, the 651 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 12) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 651 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 651 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 651 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the 651 will transmit the programmed Xon-1,2 characters as soon as receive FIFO drops to one trigger level below the programmed trigger level. Table 5 below explains this:

TABLE 5: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.*

2.14 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 651 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of a special character.

Although the Internal Register Table shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the X-registers corresponds with the LSB bit for the receive character.

2.15 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by XFR bit-3. By default, it asserts RTS# (logic 0) output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts RTS# (logic 1) output prior to sending the data. The RS485 half-duplex direction control output polarity can be inverted by enabling XFR bit-5.

TABLE 6: RS485 HALF-DUPLEX CONTROL

XFR BIT-2	XFR BIT-5	RTS# PIN
0	X	RS485 Half-Duplex control disabled
1	0	Logic 1 = TX Logic 0 = RX
1	1	Logic 1 = RX Logic 0 = TX

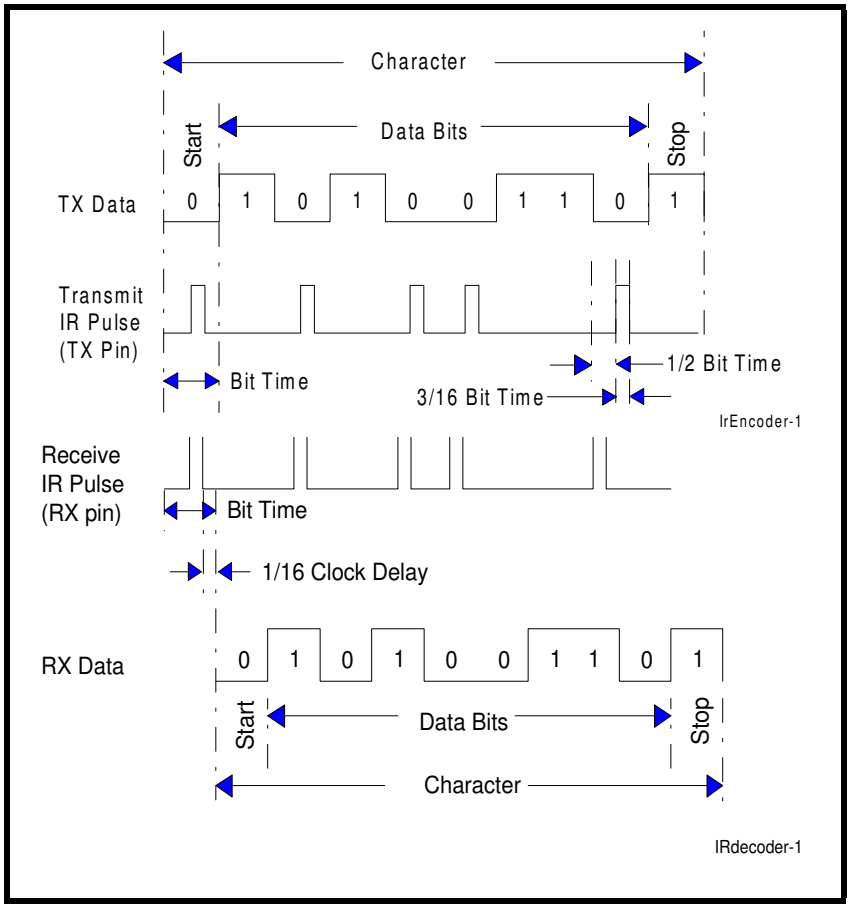
2.16 Infrared Mode

The 651 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The input pin ENIR conveniently activates the infrared mode. Activating the ENIR pin prior to power up prevents the infrared light emitting diode (LED) from turning on and drawing large amount of supply current while the system is powering up. The ENIR pin is sampled after the reset signal (RESET or RESET#) has been de-asserted. The ENIR pin also sets the MCR register bit-6 to a '1'. After a reset, the software can overwrite MCR bit-6 if so desired. In the infrared mode, the user can choose to send/receive data either half-duplex or full-duplex. The half-duplex mode is chosen by setting bit-0 of XFR register to a '1'. This prevents echoed data from reaching the receiver. When the infrared feature is enabled, the transmit data outputs, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero, see Figure 14.

The IrDA standard defines the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each "0" bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 14 below. The 651 has an additional feature to allow user to vary the transmit pulse width further reducing power consumption of the system where application permits (see IRPW register for details).

The wireless infrared decoder receives the input pulse from the infrared sensing diode on RX pin. Each time it senses a light pulse, it returns a logic 0 to the data bit stream. The 651 also includes another feature - inversion of the IR pulse (XFR register bit-1), where a LOW IR pulse in the receive data stream is recognized as a '0' bit.

FIGURE 14. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.17 Sleep Mode & Wake-up Indicator

The 651 is designed to operate with low power consumption. A special sleep mode is included to further reduce power consumption when the chip is not being used. All of these conditions must be satisfied for the 651 to enter sleep mode:

- no interrupts pending 651 (ISR bit-0 = 1)
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pin is idling at a logic 1

The 651 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 651 resumes normal operation by any of the following:

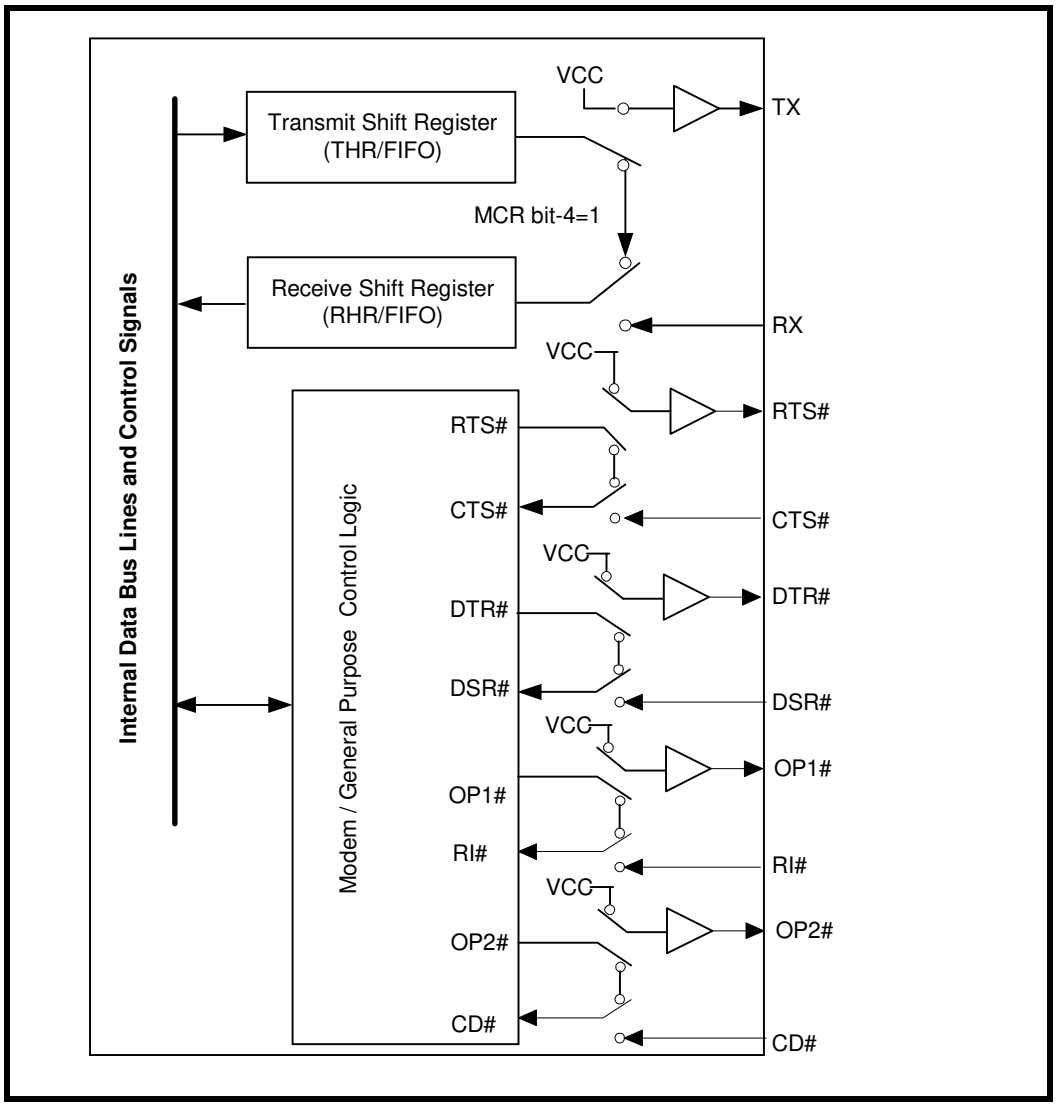
- a receive data start bit transition (logic 1 to 0)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the sleep mode is enabled and the 651 is awakened by one of the conditions described above, an interrupt is issued by the 651 to signal to the CPU that it is awake. The lower nibble of the interrupt source register (ISR) will read a value of 0x1 for this interrupt and reading the ISR clears this interrupt. Since the same value (0x1) is also used to indicate no pending interrupt, users should exercise caution while using the sleep mode. Once awakened, the 651 will return to the sleep mode automatically after any other interrupting condition (the true cause of waking up the 651) has been serviced. If the 651 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The 651 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

2.18 Internal Loopback

The 651 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 15 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal. Also, Auto RTS/CTS is not supported during internal loopback.

FIGURE 15. INTERNAL LOOP BACK



3.0 UART CONFIGURATION REGISTERS

The 651 has a set of configuration registers selected by address lines A0 to A2. The based page registers are 16C550 compatible with EXAR enhanced feature registers located on the second page (mirror) addresses. The second page registers are only accessible by setting LCR register to a value of 0xBF. The register set is shown on Table 7 and Table 8. .

TABLE 7: XR16L651 UART CONFIGURATION REGISTERS

ADDRESS	REGISTER	READ/WRITE	COMMENTS
A2 A1 A0			
16550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor Latch Low	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor Latch High	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 0	DREV - Device Revision Code	Read-only	LCR[7] = 1, LCR ≠ 0xBF, DLL, DLM = 0x00
0 0 1	DVID - Device Identification Code	Read-only	LCR[7] = 1, LCR ≠ 0xBF, DLL, DLM = 0x00
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR[7] = 0
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register	Read-only	LCR[7] = 0
	XFR - Extra Feature Register	Write-only	LCR[7] = 0, EFR[4] = 1
1 1 0	MSR - Modem Status Register	Read-only	LCR[7] = 0
	IRPW - Infrared Pulse Width Register	Write-only	LCR[7] = 0, EFR[4] = 1
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR[7] = 0
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Register	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	LCR = 0xBF
1 0 1	Xon-2 - Xon Character 2	Read/Write	LCR = 0xBF
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	LCR = 0xBF
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	LCR = 0xBF

TABLE 8: UART CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1.

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR[7] = 0
0 1 0	FCR	WR	RX FIFO Trigger	RX FIFO Trigger	0/ TX FIFO Trigger	0/ TX FIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Prescaler	0/ IR Mode ENable	0/ INT Type Select	Internal Loopback Enable	OP2#/ IRQn Output Enable	OP1#	RTS# Output Control	DTR# Output Control	
1 0 1	LSR	RD	RX FIFO Error	TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Data Overrun Error	RX Data Ready	
	XFR	WR	Rsrvd	Rsrvd	Invert RS485 Control Output	Enable XonAny	LSR INT Mode	Auto RS485 Enable	Invert IR RX Input	Enable Half-duplex IR	LCR[7]=0
1 1 0	MSR	RD	CD	RI	DSR	CTS	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
	IRPW	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 8: UART CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1.

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR ≠ 0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	0	1	0	0	
Enhanced Registers											
0 1 0	EFR	R/W	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5] MSR[7:4] IRPW[7:0] XFR[7:0]	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	LCR=0xBF
1 0 0	XON1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read-Only

See “Receiver” on page 16.

4.2 Transmit Holding Register (THR) - Write-Only

See “Transmitter” on page 14.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) register.

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR bit-0 = a logic 1) and receive interrupts (IER bit-0 = logic 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR bit-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.