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GENERAL DESCRIPTION

The XR16M752/XR68M752[1] (M752) is a high performance dual universal asynchronous receiver and transmitter (UART) with 64 byte TX and RX FIFOs. The M752 operates from 1.62 to 3.63 volts. It is pin-to-pin and software compatible to the TL16C752B and SC16C752B, but with additional features such as a programmable fractional baud rate generator, automatic RS-485 half-duplex direction control, infrared mode and 8X and 4X sampling rate. The standard features include 16 selectable TX and RX FIFO trigger levels, automatic hardware (RTS/CTS) and software (Xon/Xoff) flow control, and a complete modem interface. Onboard registers provide the user with operational status and data error flags. An internal loopback capability allows system diagnostics. Each channel is independently programmable for data rates up to 16 Mbps at 3.3V with a 4X sampling rate. The XR68M752 has an additional 16/68# pin to select between the Intel and Motorola bus interface. The M752 is available in the 48-pin TQFP, 32-pin QFN and 49-pin STBGA packages.

NOTE: *1 Covered by U.S. Patent #5,649,122*

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FEATURES

- 1.62 to 3.6 Volt Operation
- Pin-to-pin and software compatible to TI's TL16C752B and Philips' SC16C752B in the 48-TQFP package
- Two independent UART channels
  - Data rate of up to **16 Mbps at 3.3 V**
  - Data rate of up to **12.5 Mbps at 2.5 V**
  - Data rate of up to **8 Mbps at 1.8 V**
  - Fractional Baud Rate Generator
  - Data sampling rates of 16X, 8X and 4X
  - Transmit and Receive FIFOs of 64 bytes
  - Programmable TX and RX FIFO Trigger Levels
  - Automatic Hardware (RTS/CTS) Flow Control
  - Automatic Software (Xon/Xoff) Flow Control
  - Halt and Resume Transmission Control
  - Automatic RS-485 Half-duplex Direction Control Output via RTS#
  - Wireless Infrared (IrDA 1.0) Encoder/Decoder
  - Automatic sleep mode
  - Full modem interface
- Crystal oscillator (up to 24MHz) or external clock (up to 64MHz) input
- 48-TQFP, 32-QFN and 49-STBGA packages

FIGURE 1. XR16M752 BLOCK DIAGRAM

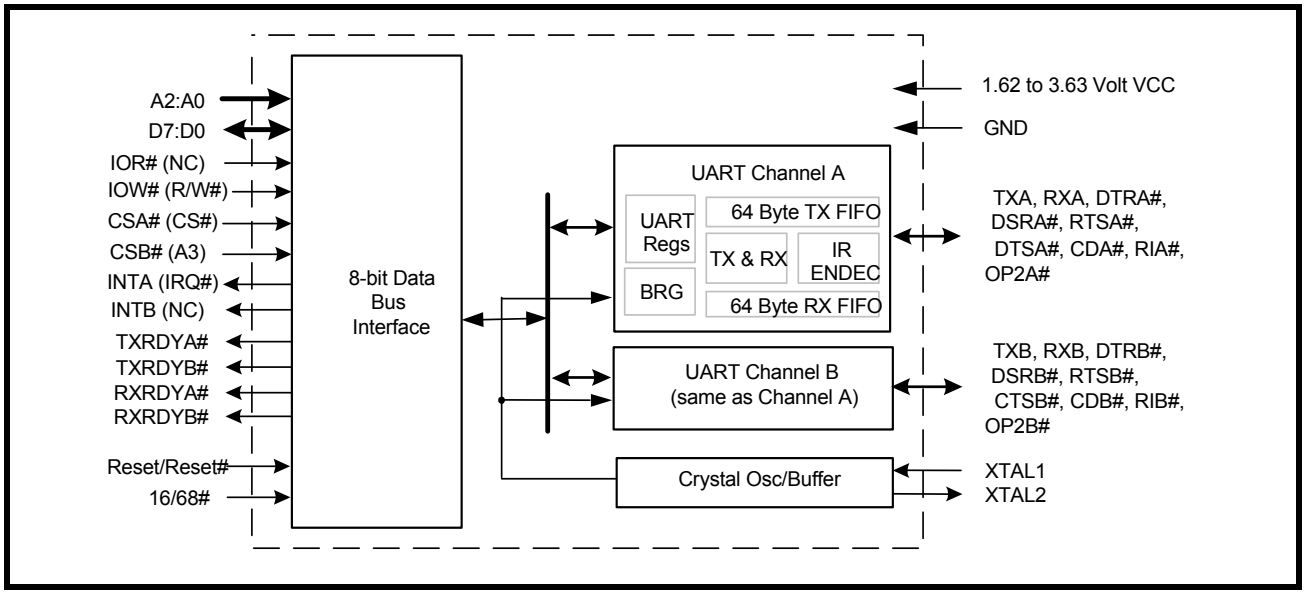


FIGURE 2. PIN OUT ASSIGNMENT - TQFP AND QFN PACKAGES

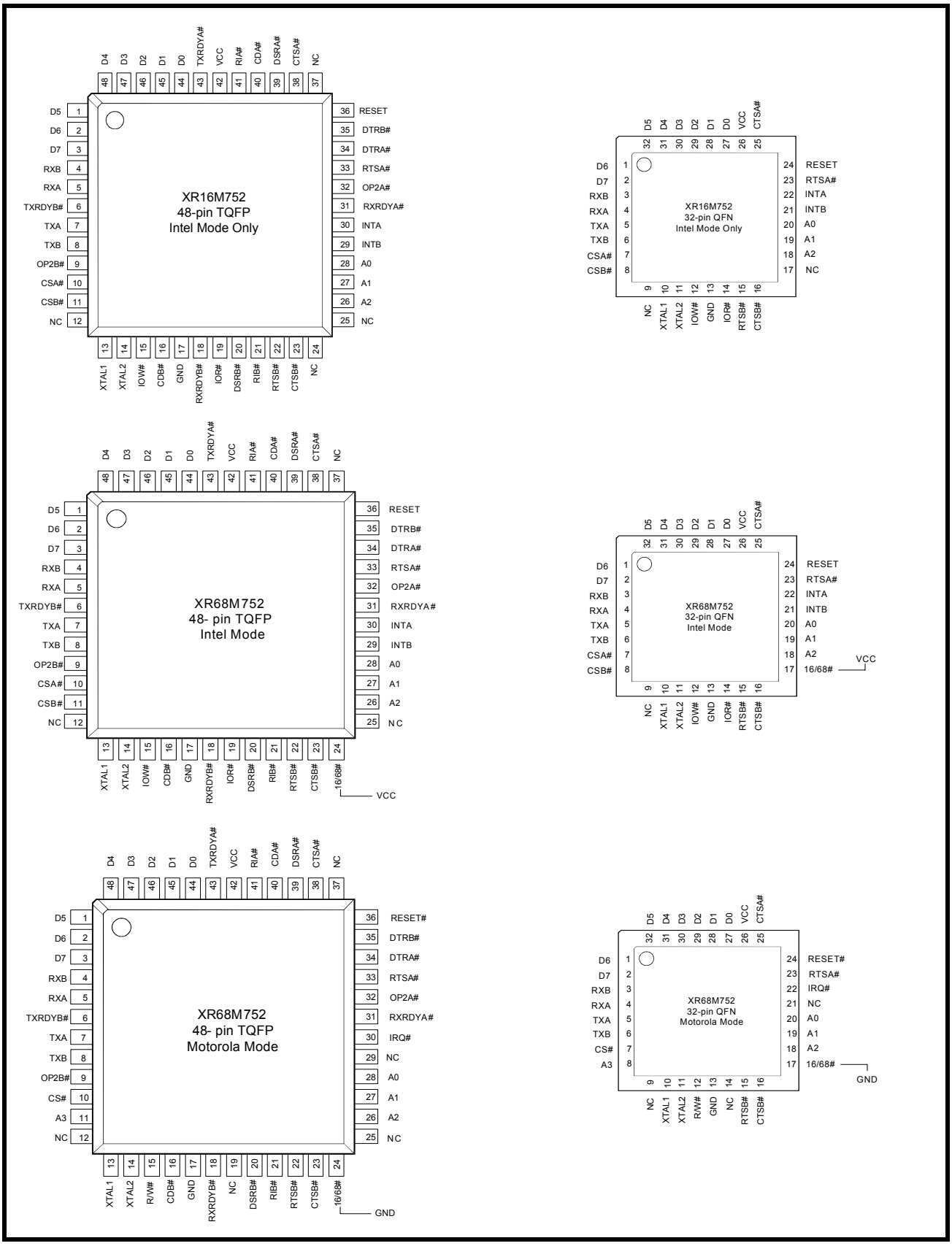
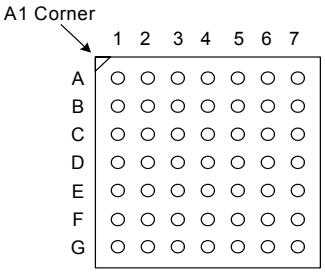


FIGURE 3. PIN OUT ASSIGNMENT - STBGA PACKAGE



Transparent Top View

NC	D3	D0	RIA#	CTSA#	RS485#	DTRA#
D5	D4	D1	D2	VCC	DSRA#	RESET
D6	D7	RXB	TXRDYA#	CDA#	OP2A#	DTRB#
TXB	RXA	TXA	TXRDYB#	RTSA#	INTA	INTB
CSB#	CSA#	OP2B#	RIB#	RXRDYA#	A0	A1
PWRSAVE	IOW#	CDB#	RXRDYB#	DSRB#	CTSB#	ENIR#
XTAL1	XTAL2	GND	IOR#	RTSB#	16/68#	A2

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16M752IL32	32-pin QFN	-40°C to +85°C	Active
XR16M752IM48	48-Lead TQFP	-40°C to +85°C	Active
XR68M752IL32	32-pin QFN	-40°C to +85°C	Active
XR68M752IM48	48-Lead TQFP	-40°C to +85°C	Active
XR68M752IB49	49-pin STBGA	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	32-QFN PIN #	48-TQFP PIN #	49-STBGA PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE					
A2 A1 A0	18 19 20	26 27 28	G7 E7 E6	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A/B during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	2 1 32 31 30 29 28 27	3 2 1 48 47 46 45 44	C2 C1 B1 B2 A2 B4 B3 A3	I/O	Data bus lines [7:0] (bidirectional).
IOR# (NC)	14	19	G4	I	When 16/68# pin is HIGH, the Intel bus interface is selected and this input becomes read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When 16/68# pin is LOW, the Motorola bus interface is selected and this input is not used.
IOW# (R/W#)	12	15	F2	I	When 16/68# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is LOW, the Motorola bus interface is selected and this input becomes read (HIGH) and write (LOW) signal.
CSA# (CS#)	7	10	E2	I	When 16/68# pin is HIGH, this input is chip select A (active low) to enable channel A in the device. When 16/68# pin is LOW, this input becomes the chip select (active low) for the Motorola bus interface.
CSB# (A3)	8	11	E1	I	When 16/68# pin is HIGH, this input is chip select B (active low) to enable channel B in the device. When 16/68# pin is LOW, this input becomes address line A3 which is used for channel selection in the Motorola bus interface. Input logic 0 selects channel A and logic 1 selects channel B.

Pin Description

NAME	32-QFN PIN #	48-TQFP PIN #	49-STBGA PIN #	TYPE	DESCRIPTION
INTA (IRQ#)	22	30	D6	O	When 16/68# pin is HIGH for Intel bus interface, this output becomes channel A interrupt output. The output state is defined by the user through the software setting of MCR[3]. INTA is set to the active mode and OP2A# output LOW when MCR[3] is set to a logic 1. INTA is set to the three state mode and OP2A# to HIGH when MCR[3] is set to a logic 0. See MCR[3]. When 16/68# pin is LOW for Motorola bus interface, this output becomes device interrupt output (active low, open drain). An external pull-up resistor is required for proper operation.
INTB (NC)	21	29	D7	O	When 16/68# pin is HIGH for Intel bus interface, this output becomes channel B interrupt output. The output state is defined by the user through the software setting of MCR[3]. INTB is set to the active mode and OP2A# output to LOW when MCR[3] is set to a logic 1. INTA is set to the three state mode and OP2A# to HIGH when MCR[3] is set to a logic 0. See MCR[3]. When 16/68# pin is LOW for Motorola bus interface, this output is not used.
TXRDYA#	-	43	C4	O	UART channel A Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel A. See **Table 3**. If it is not used, leave it unconnected.
RXRDYA#	-	31	E5	O	UART channel A Receiver Ready (active low). This output provides the RX FIFO/RHR status for receive channel A. See **Table 3**. If it is not used, leave it unconnected.
TXRDYB#	-	6	D4	O	UART channel B Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel B. See **Table 4**. If it is not used, leave it unconnected.
RXRDYB#	-	18	F4	O	UART channel B Receiver Ready (active low). This output provides the RX FIFO/RHR status for receive channel B. See **Table 3**. If it is not used, leave it unconnected.
MODEM OR SERIAL I/O INTERFACE					
TXA	5	7	D3	O	UART channel A Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be HIGH during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is LOW. If it is not used, leave it unconnected.

Pin Description

NAME	32-QFN PIN #	48-TQFP PIN #	49-STBGA PIN #	TYPE	DESCRIPTION
RXA	4	5	D2	I	UART channel A Receive Data or infrared receive data. Normal receive data input must idle HIGH. The infrared receiver pulses typically idles at LOW but can be inverted by software control prior going in to the decoder, see MCR[6]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSA#	23	33	D5	O	UART channel A Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6] and IER[6]. For auto RS485 half-duplex direction control, see DLD[6].
CTSA#	25	38	A5	I	UART channel A Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7] and IER[7]. This input should be connected to VCC or GND when not used.
DTRA#	-	34	A7	O	UART channel A Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRA#	-	39	B6	I	UART channel A Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC or GND when not used.
CDA#	-	40	C5	I	UART channel A Carrier-Detect (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RIA#	-	41	A4	I	UART channel A Ring-Indicator (active low) or general purpose input. This input should be connected to VCC or GND when not used.
OP2A#	-	32	C6	O	Output Port 2 Channel A - The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode and OP2A# output LOW when MCR[3] is set to a logic 1. INTA is set to the three state mode and OP2A# output HIGH when MCR[3] is set to a logic 0. See MCR[3]. If INTA is used, this output should not be used as a general output else it will disturb the INTA output functionality.
TXB	6	8	D1	O	UART channel B Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be HIGH during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is LOW. If it is not used, leave it unconnected.
RXB	3	4	C3	I	UART channel B Receive Data or infrared receive data. Normal receive data input must idle HIGH. The infrared receiver pulses typically idles at logic 0 but can be inverted by software control prior going in to the decoder, see MCR[6]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor.

Pin Description

NAME	32-QFN PIN #	48-TQFP PIN #	49-STBGA PIN #	TYPE	DESCRIPTION
RTSB#	15	22	G5	O	UART channel B Request-to-Send (active low) or general purpose output. This port must be asserted prior to using auto RTS flow control, see EFR[6] and IER[6]. For auto RS485 half-duplex direction control, see DLD[6].
CTSB#	16	23	F6	I	UART channel B Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7] and IER[7]. This input should be connected to VCC or GND when not used.
DTRB#	-	35	C7	O	UART channel B Data-Terminal-Ready (active low) or general purpose output. If it is not used, leave it unconnected.
DSRB#	-	20	F5	I	UART channel B Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC or GND when not used.
CDB#	-	16	F3	I	UART channel B Carrier-Detect (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RIB#	-	21	E4	I	UART channel B Ring-Indicator (active low) or general purpose input. This input should be connected to VCC or GND when not used.
OP2B#	-	9	E3	O	Output Port 2 Channel B - The output state is defined by the user and through the software setting of MCR[3]. INTB is set to the active mode and OP2B# output LOW when MCR[3] is set to a logic 1. INTB is set to the three state mode and OP2B# output HIGH when MCR[3] is set to a logic 0. See MCR[3]. If INTB is used, this output should not be used as a general output else it will disturb the INTB output functionality.
ANCILLARY SIGNALS					
XTAL1	10	13	G1	I	Crystal or external clock input.
XTAL2	11	14	G2	O	Crystal or buffered clock output.
PwrSave	-	-	F1	I	PowerSave (active high, internal pull-down resistor). This feature isolates the 752's data bus interface from the host preventing other bus activities that cause higher power drain during sleep mode. See Sleep Mode with Auto Wake-up and PowerSave Feature section for details.
16/68#	17	24	G6	I	Intel or Motorola Bus Select (internal pull-up resistor). This pin is not available for the XR16M752. This pin is available for the XR68M752 only. When 16/68# pin is HIGH, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When 16/68# pin is LOW, 68 or Motorola mode, the device will operate in the Motorola bus type of interface.

Pin Description

NAME	32-QFN PIN #	48-TQFP PIN #	49-STBGA PIN #	TYPE	DESCRIPTION
RESET (RESET#)	24	36	B7	I	When 16/68# pin is HIGH for Intel bus interface, this input becomes RESET (active high). When 16/68# pin is LOW for Motorola bus interface, this input becomes RESET# (active low). A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs of channel A and B. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (see **Table 16**).
EN485#	-	-	A6	I	Auto RS-485 half-duplex direction output enable for channel A and B (active low, internal pull-up resistor). Connect this pin to VCC or leave unconnected for normal RTS# A/B function. Connect to GND for auto RS-485 half-duplex direction output via the RTS# A/B pins. The Auto RS-485 half-duplex direction output control feature can be disabled via DLD[6] after power-up. **SEE "AUTO RS485 HALF-DUPLEX CONTROL" ON PAGE 18.**
ENIR#	-	-	F7	I	IR mode enable for channel A and B (active low, internal pull-up resistor). Connect this pin to VCC or leave unconnected for normal TX and RX. Connect to GND for both channel A and B to power up in the IR mode. The IR mode can be disabled via DLD[7] after power-up. **SEE "INFRARED MODE" ON PAGE 20.**
VCC	26	42	B5	Pwr	1.62V to 3.63V power supply.
GND	13	17	G3	Pwr	Power supply common, ground.
GND	Center Pad	-	-	Pwr	The center pad on the backside of the QFN package is metallic and should be connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.
NC	9	12, 25, 37	A1		No Connection.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The XR16M752/XR68M752 (M752) integrates the functions of 2 enhanced 16C550 Universal Asynchronous Receiver and Transmitter (UART). Each UART is independently controlled having its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 64-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, infrared encoder and decoder (IrDA ver 1.0), programmable fractional baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 16 Mbps with 4X sampling clock rate. The XR16M752 is a 1.62V to 3.63V device. The M752 is fabricated with an advanced CMOS process.

Enhanced Features

The M752 DUART provides a solution that supports 64 bytes of transmit and receive FIFO memory, instead of 16 bytes in the industry standard 16C550. The M752 is designed to work with low supply voltage and high performance data communication systems, that require fast data processing time. Increased performance is realized in the M752 by the larger transmit and receive FIFOs, FIFO trigger level control and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the 16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2 Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 64 byte FIFO in the M752, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

The M752 supports a half-duplex output direction control signaling pin, RTS# A/B, to enable and disable the external RS-485 transceiver operation. It automatically switches the logic state of the output pin to the receive state after the last stop-bit of the last character has been shifted out of the transmitter. After receiving, the logic state of the output pin switches back to the transmit state when a data byte is loaded in the transmitter. The auto RS-485 direction control pin is not activated after reset. To activate the direction control function, user has to set DLD Bit-6 to "1". This pin is HIGH for receive state and LOW for transmit state.

Data Rate

The M752 is capable of operation up to 16 Mbps at 3.3V with 4X internal sampling clock rate, 8 Mbps at 3.3V with 8X sampling clock rate, and 4 Mbps at 3.3V with 16X internal sampling clock rate. The device can operate with an external 24 MHz crystal on pins XTAL1 and XTAL2, or external clock source of up to 64 MHz on XTAL1 pin. With a typical crystal of 14.7456 MHz and through a software option, the user can set the prescaler bit for data rates of up to 3.68 Mbps.

The rich feature set of the M752 is available through the internal registers. Automatic hardware/software flow control, programmable transmit and receive FIFO trigger levels, programmable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features.

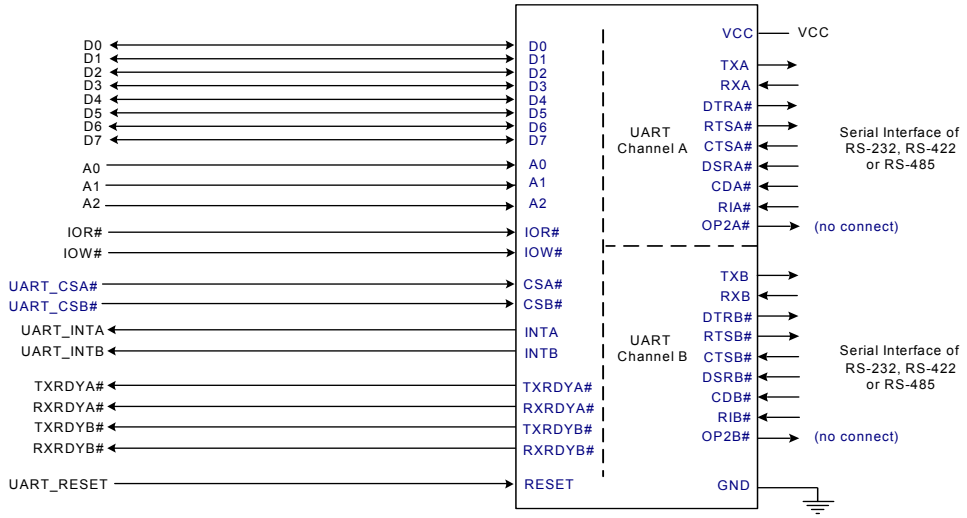
Following a power on reset or an external reset, the M752 is software compatible with previous generation of UARTs, 16C450, 16C550 and 16C2550.

2.0 FUNCTIONAL DESCRIPTIONS

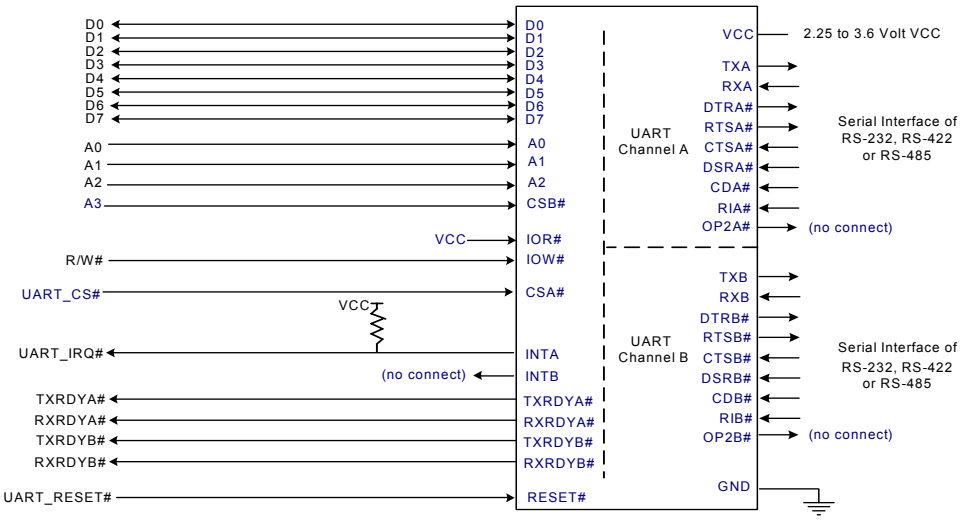
2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The XR16M752 data interface supports the Intel compatible types of CPUs while the XR68M752 supports both the Intel and Motorola compatible data interfaces. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# signals. Both UART channels share the same data bus for host operations. The data bus interconnections are shown in Figure 4.

FIGURE 4. XR16M752/XR68M752 DATA BUS INTERCONNECTIONS



Intel Data Bus Interconnections



Motorola Data Bus Interconnections

2.2 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 16). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.3 Channel A and B Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. During Intel Bus Mode (16/68# pin connected to VCC), a logic 0 on chip select pins, CSA# or CSB#, allows the user to select UART channel A or B to configure, send transmit data and/or unload receive data to/from the UART. Selecting both UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from both UARTs simultaneously. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A AND B SELECT IN 16 MODE

CSA#	CSB#	FUNCTION
1	1	UART de-selected
0	1	Channel A selected
1	0	Channel B selected
0	0	Channel A and B selected

During Motorola Bus Mode (16/68# pin connected to GND), the package interface pins are configured for connection with Motorola, and other popular microprocessor bus types. In this mode the M752 decodes an additional address, A3, to select one of the UART ports. The A3 address decode function is used only when in the Motorola Bus Mode. See Table 2.

TABLE 2: CHANNEL A AND B SELECT IN 68 MODE

CS#	A3	FUNCTION
1	N/A	UART de-selected
0	0	Channel A selected
0	1	Channel B selected

2.4 Channel A and B Internal Registers

Each UART channel in the M752 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550 and dual ST16C2550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM/DLD), and a user accessible Scratchpad Register (SPR).

Beyond the general 16C550 features and capabilities, the M752 offers enhanced feature registers (EFR, Xon/Xoff 1, Xon/Xoff 2, TCR, TLR and DLD) that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, automatic RS-485 half-duplex direction output enable/disable, and programmable FIFO trigger level control. All the register functions are discussed in full detail later in **"Section 3.0, UART Internal Registers" on page 24**.

2.5 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document doesn't mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A/B and TXRDY# A/B output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the M752 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the M752 sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior. Also see Figures 20 through 25.

TABLE 3: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY# A/B	LOW = 1 byte. HIGH = no data.	LOW = at least 1 byte in FIFO. HIGH = FIFO empty.	HIGH to LOW transition when FIFO reaches the trigger level, or time-out occurs. LOW to HIGH transition when FIFO empties or LSR[7] = 1.
TXRDY# A/B	LOW = THR empty. HIGH = byte in THR.	LOW = FIFO empty. HIGH = at least 1 byte in FIFO.	LOW = FIFO is below the trigger level. HIGH = FIFO is full.

2.6 INTA and INTB Outputs

The INTA and INTB interrupt output changes according to the operating mode and enhanced features setup. Table 4 and 5 summarize the operating behavior for the transmitter and receiver. Also see Figures 20 through 25.

TABLE 4: INTA AND INTB PINS OPERATION FOR TRANSMITTER

	Auto RS485 Mode	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	NO	LOW = a byte in THR HIGH = THR empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty
INTA/B Pin	YES	LOW = a byte in THR HIGH = transmitter empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or transmitter empty

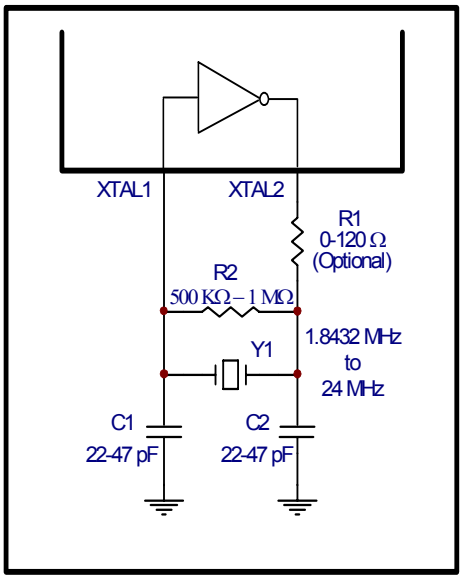
TABLE 5: INTA AND INTB PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	LOW = no data HIGH = 1 byte	LOW = FIFO below trigger level HIGH = FIFO above trigger level

2.7 Crystal Oscillator or External Clock Input

The M752 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Please note that the input XTAL1 is not 5V tolerant and so the maximum at the pin should be VCC. For programming details, see "**Section 2.8, Programmable Baud Rate Generator with Fractional Divisor" on page 13**."

FIGURE 5. TYPICAL OSCILLATOR CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100 ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see **Figure 5**). The programmable Baud Rate Generator is capable of operating with a crystal oscillator frequency of up to 24 MHz. However, with an external clock input on XTAL1 pin, it can extend its operation up to 64 MHz (16 Mbps serial data rate) at 3.3V with an 4X sampling rate. For further reading on the oscillator circuit please see the Application Note DAN108 on the EXAR web site at **http://www.exar.com.**

2.8 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X, 8X or 4X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon reset. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the dvisior. The four lower bits of the DLD are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. **Table 6** shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in **Table 6**. At 8X sampling rate, these data rates would double and at 4X sampling rate, these data rates would quadruple. Also, when using 8X sampling mode, the bit time will have a jitter of ± 1/16 whenever the DLD is non-zero and is an odd number.

When using 4X sampling mode, the bit time will have a jitter of ± 1/8 whenever DLD is non-zero, odd and not a multiple of 4. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal)=(XTAL1 clock frequency / prescaler) /(serial data rate x 16), with 16X mode, **DLD[5:4]='00'**
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 8), with 8X mode, **DLD[5:4] = '01'**
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 4), with 4X mode, **DLD[5:4] = '10'**

The closest divisor that is obtainable in the M752 can be calculated using the following formula:

ROUND((Required Divisor - TRUNC(Required Divisor))*16)/16 + TRUNC(Required Divisor), where

DLM = TRUNC(Required Divisor) >> 8
DLL = TRUNC(Required Divisor) & 0xFF
DLD = ROUND((Required Divisor-TRUNC(Required Divisor))*16)

In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value 'A' by 'B' number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 6. BAUD RATE GENERATOR

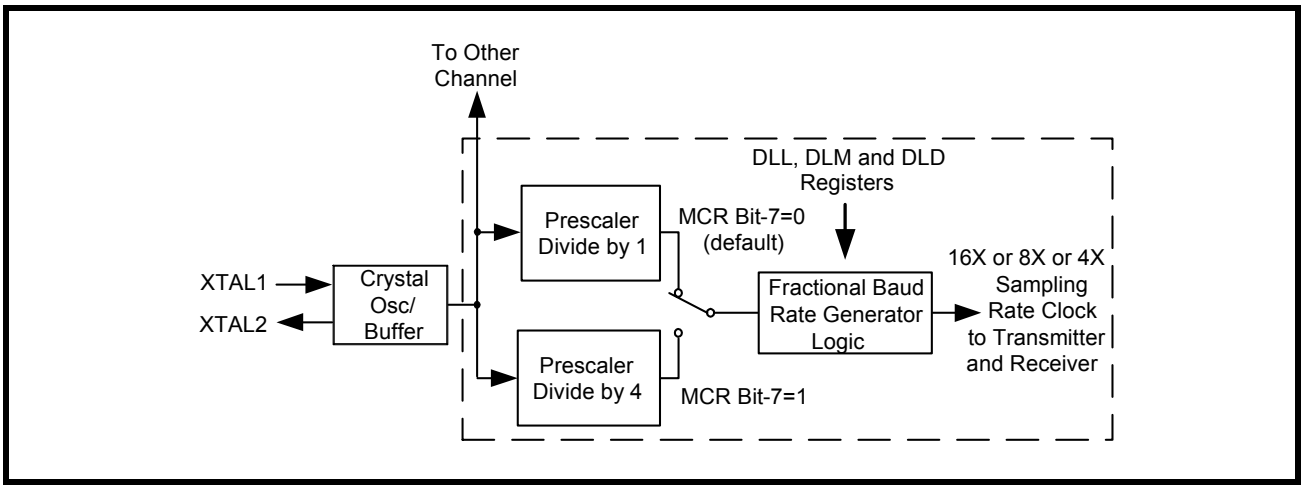


TABLE 6: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	DIVISOR FOR 16x Clock (Decimal)	DIVISOR OBTAINABLE IN M752	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DLD PROGRAM VALUE (HEX)	DATA ERROR RATE (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0
300000	5	5	0	5	0	0
400000	3.75	3 12/16	0	3	C	0
460800	3.2552	3 4/16	0	3	4	0.16
500000	3	3	0	3	0	0
750000	2	2	0	2	0	0
921600	1.6276	1 10/16	0	1	A	0.16
1000000	1.5	1 8/16	0	1	8	0

2.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X/4X internal clock. A bit time is 16 (8 if 8X or 4 if 4X) clock periods (see DLD[5:4]). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR[6:5]).

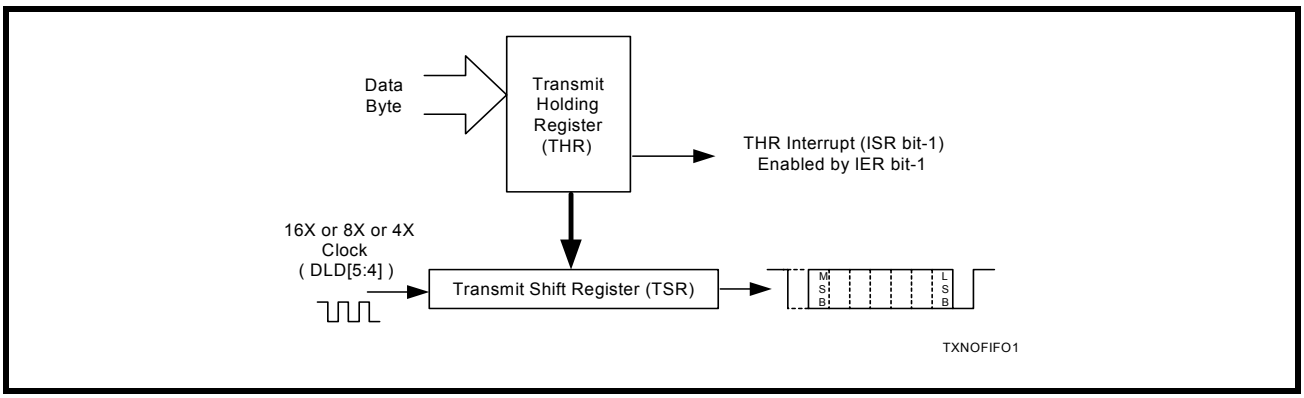
2.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

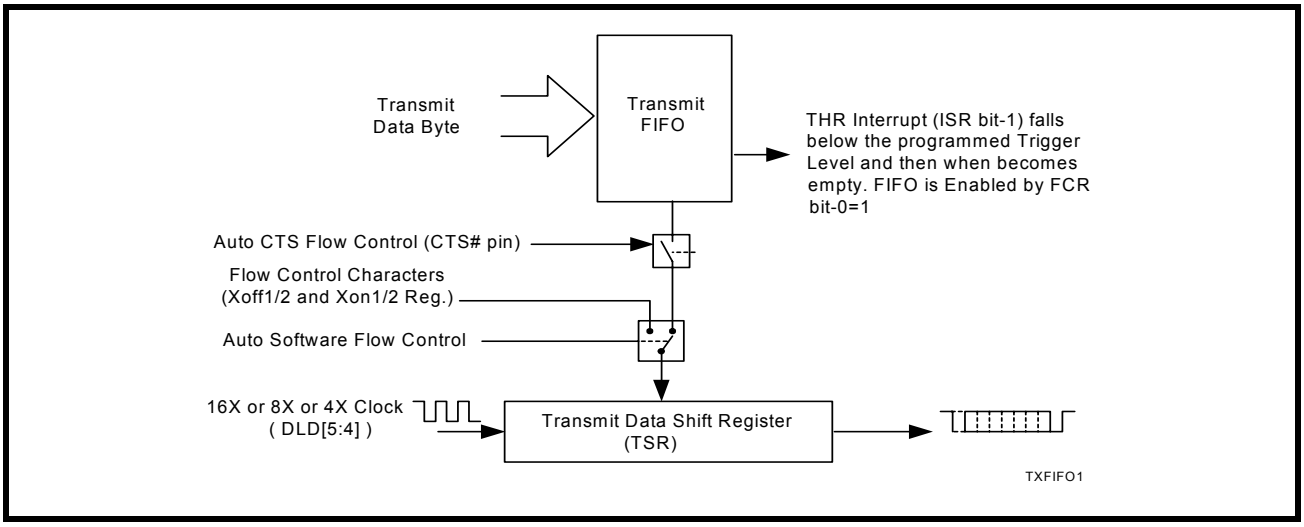
FIGURE 7. TRANSMITTER OPERATION IN NON-FIFO MODE



2.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 8. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X/4X clock (DLD [5:4]) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X/4X clock rate. After 8 clocks (or 4 if 8X or 2 if 4X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 9. RECEIVER OPERATION IN NON-FIFO MODE

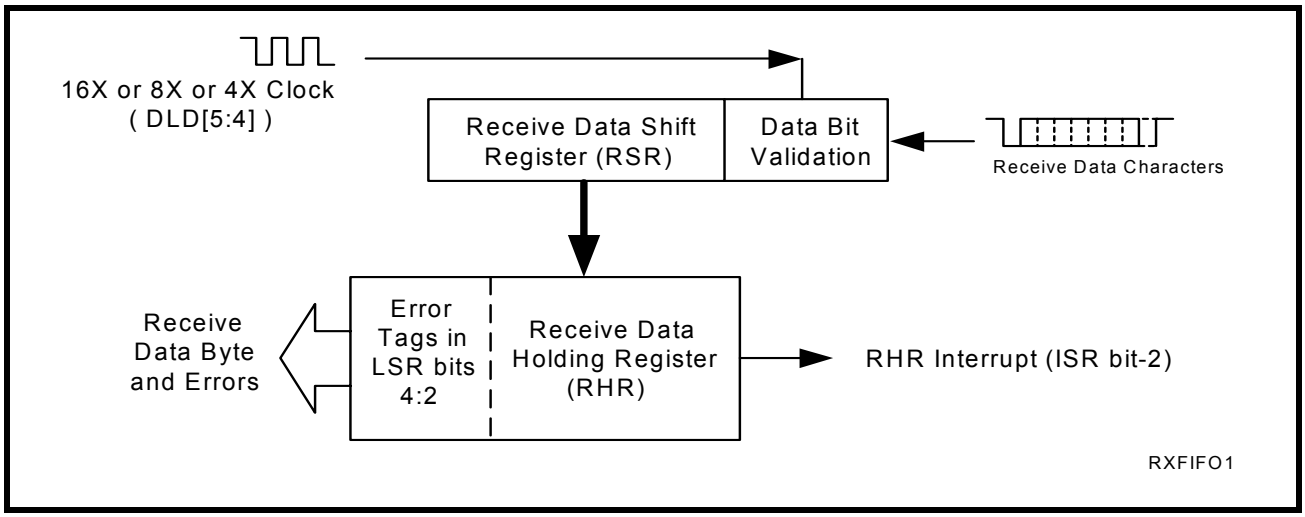
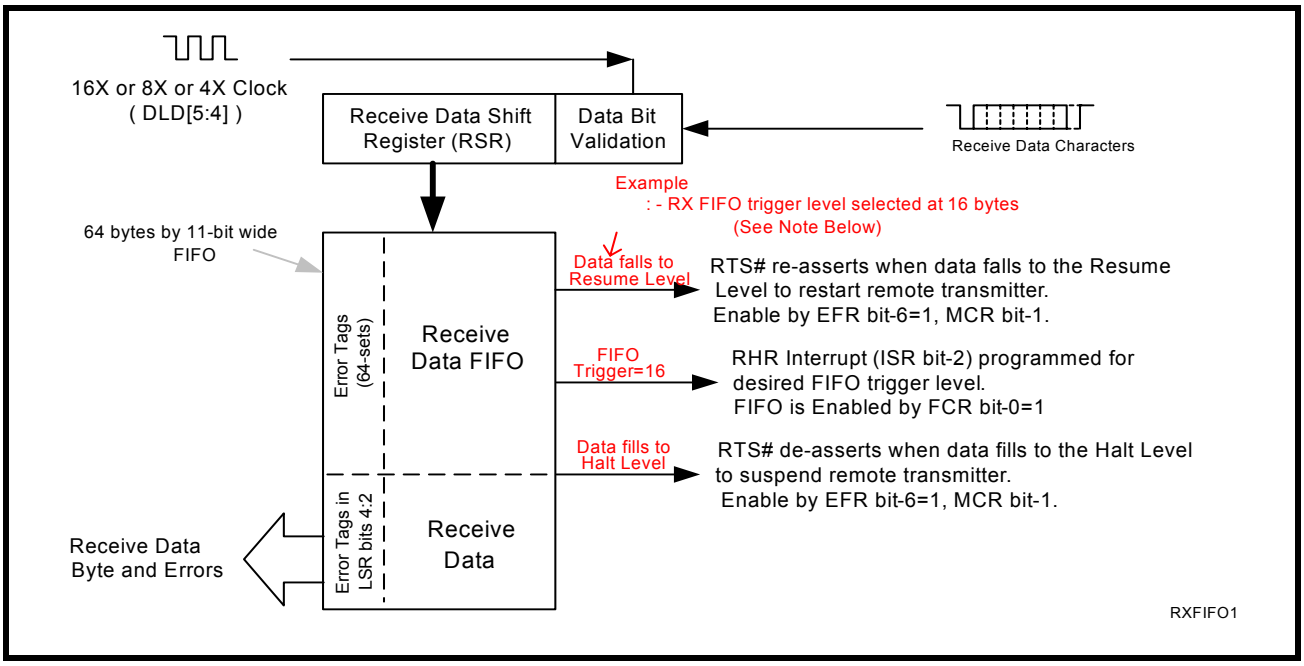


FIGURE 10. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.11 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 11):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.12 Auto RTS Halt and Resume

The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches the Halt Level (TCR[3:0]). The RTS# pin will return LOW after the RX FIFO is unloaded to the Resume Level (TCR[7:4]). Under these conditions, the M752 will continue to accept data if the remote UART continues to transmit data. It is the responsibility of the user to ensure that the Halt Level is greater than the Resume Level. If interrupts are used, it is recommended that Halt Level > RX Trigger Level > Resume Level. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On).

2.13 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by DLD bit-6. When idle, the auto RS485 half-duplex direction control signal (RTS#) is LOW for receive mode. When data is loaded into the THR for transmission, the RTS# output is automatically asserted HIGH prior to sending the data. After the last stop bit of the last character that has been transmitted, the RTS# signal is automatically de-asserted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts RTS# (HIGH) output prior to sending the data. In addition to changing the behavior of the RTS# output, this feature also changes the behavior of the transmit empty interrupt (see Table 4). In the 49-pin STBGA package, this feature can be enabled by connecting the EN485# pin to GND. If this feature is enabled by the EN485# pin, it can be disabled by DLD bit-6 after power-up.

2.14 Auto CTS Flow Control

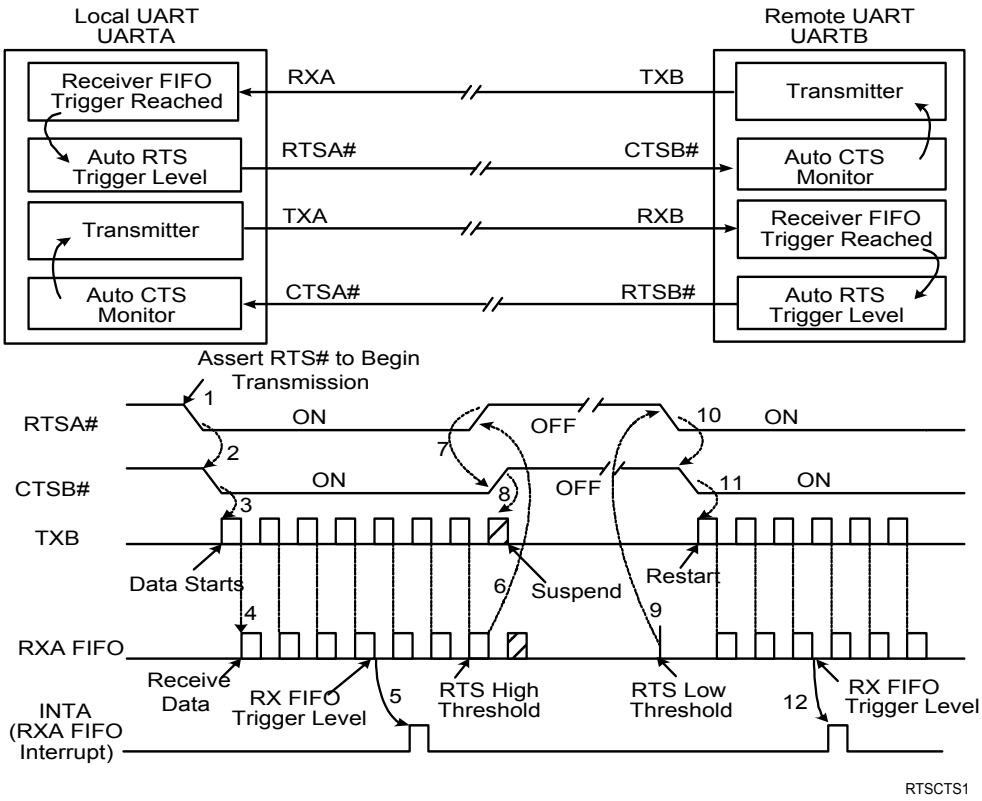
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 11**):

- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 11. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.15 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 15), the M752 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the M752 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the M752 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the M752 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to 0x00. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 15) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the M752 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the M752 automatically sends the Xoff-1,2 via the serial TX output to the remote modem when the RX FIFO reaches the Halt Level (TCR[3:0]). To clear this condition, the M752 will transmit the programmed Xon-1,2 characters as soon as RX FIFO falls down to the Resume Level.

2.16 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The M752 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison.

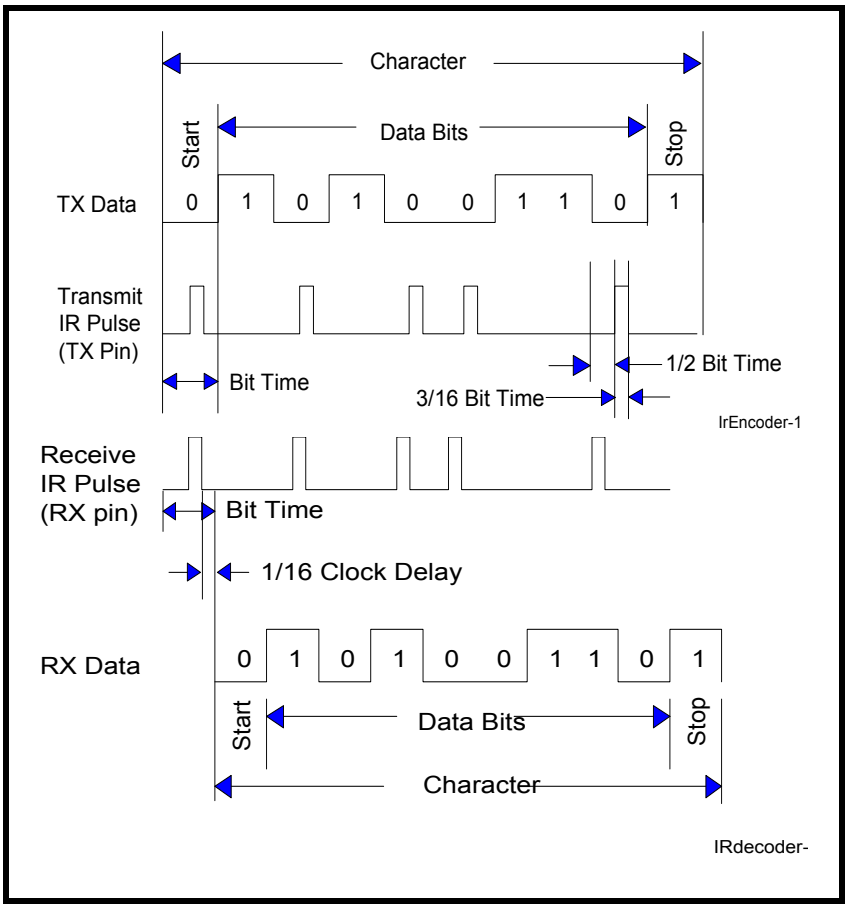
2.17 Infrared Mode

The M752 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 12 below.

The infrared encoder and decoder can be enabled by setting DLD register bit-7 to a ‘1’. When the infrared feature is enabled, the transmit data output, TX, idles LOW. Likewise, the RX input also idles LOW, see Figure 12. In the 49-pin STBGA package, this feature can be enabled upon power-up by connecting the ENIR# pin of the STBGA package to GND. If the IR mode is enabled via the ENIR# pin, it can be disabled after power-up via DLD bit-7.

The wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream.

FIGURE 12. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.18 Sleep Mode with Wake-Up Indicator and PowerSave Feature

The M2751 supports low voltage system designs, hence, a sleep mode with auto wake-up and PowerSave feature is included to reduce power consumption when the device is not actively used.

2.19 Sleep Mode with Auto Wake-Up

The M752 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used. In addition, there is a PowerSave Feature on the 49-pin STBGA package that eliminates any unnecessary external buffer.

All of these conditions must be satisfied for the M752 to enter sleep mode:

- no interrupts pending for both channels of the M752 (ISR bit-0 = 1)
- sleep mode of both channels are enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idling HIGH

The M752 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The M752 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the M752 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the M752 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from channel A or B. The M752 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, and modem input lines remain steady when the M752 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 40. If the input lines are floating or are toggling while the M752 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current.

2.19.1 PowerSave Feature (49-pin STBGA pacakge only)

The PowerSave Feature will eliminate the need for an external buffer by internally isolating the address, data and control signals from other bus activities that could cause wasteful power drain. The M752 enters PowerSave mode when pin F1 is connected to VCC and the M752 is in sleep mode (see Sleep Mode section above).

Since PowerSave mode isolates the address, data and control signals, the device will wake-up by:

- a receive data start bit transition (HIGH to LOW)
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

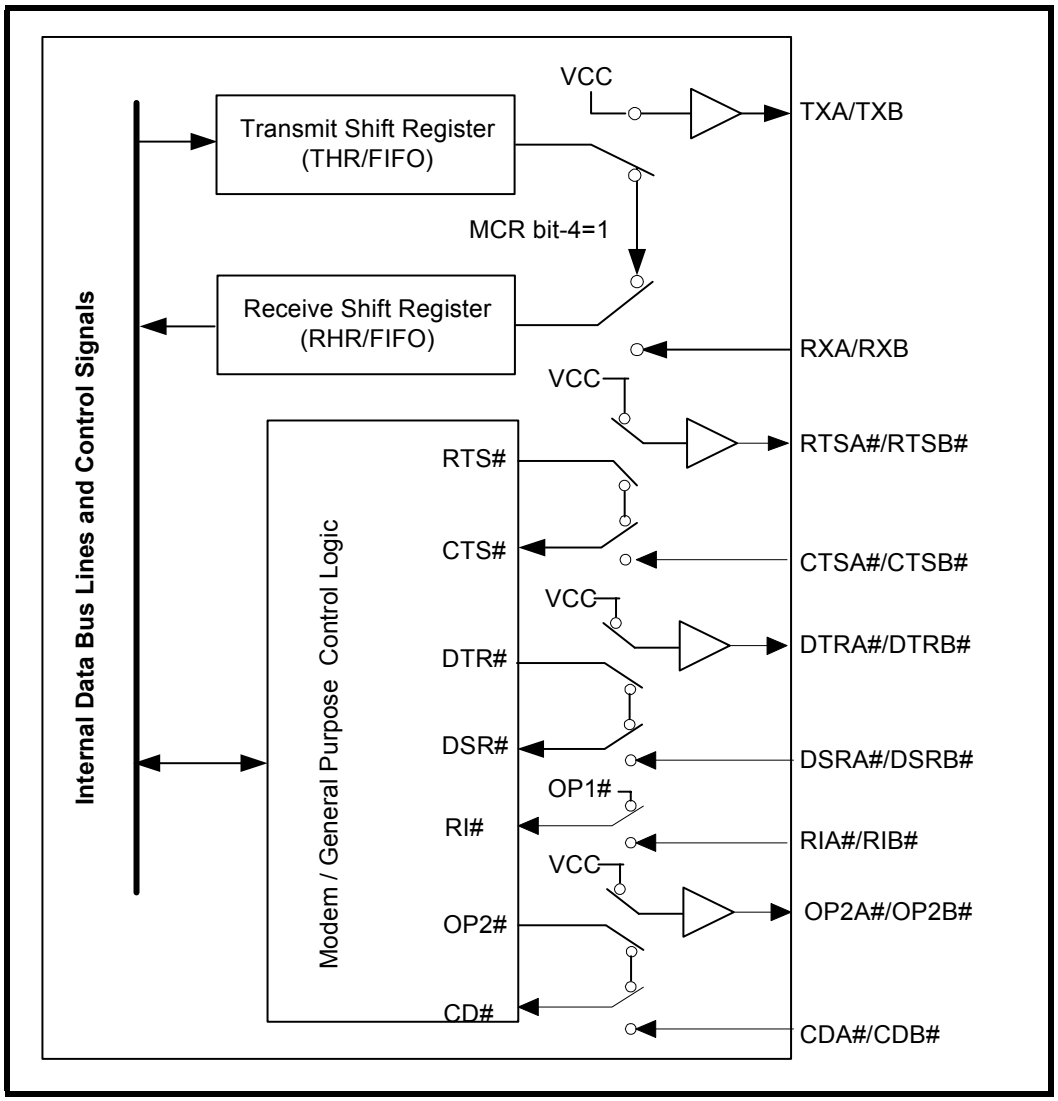
The M752 will return to the PowerSave mode automatically after a read to the MSR (to reset the modem inputs) and all interrupting conditions have been serviced and cleared. The 2751 will stay in the PowerSave mode of operation until it is disabled by setting IER bit-4 to a logic 0 and/or the PowerSave pin is connected to GND.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate. Also, it is important to keep RX A/B inputs idling HIGH or “marking” condition during sleep mode to avoid receiving a “break” condition upon the restart. This may occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the designer can use a 47k-100k ohm pull-up resistor on the RXA and RXB pins.

2.20 Internal Loopback

The M752 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 13 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held while the CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input pin must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal. Also, Auto RTS/CTS flow control is not supported during internal loopback.

FIGURE 13. INTERNAL LOOP BACK IN CHANNEL A AND B



3.0 UART INTERNAL REGISTERS

Each of the UART channel in the M752 has its own set of configuration registers selected by address lines A0, A1 and A2 with CSA# or CSB# selecting the channel. The complete register set is shown on Table 7 and Table 8.

TABLE 7: UART CHANNEL A AND B UART INTERNAL REGISTERS

ADDRESSES A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor MSB	Read/Write	
0 1 0	DLD - Divisor Fractional	Read/Write	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register	Read-only	
1 1 0	MSR - Modem Status Register	Read-only	See Table 13
1 1 1	SPR - Scratch Pad Register	Read/Write	See Table 12
1 1 0	TCR - Transmission Control Register	Read/Write	See Table 13
1 1 1	TLR - Trigger Level Register	Read/Write	See Table 12
1 1 1	FIFO Rdy - FIFO Ready Register	Read-only	See Table 12
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Register	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TXFIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ Clock Pres-caler Select	0/ TCR and TLR ENable	0/ XonAny	Internal Lopback Enable	OP2#/ INT Out-put Enable	FIFO Rdy Enable (OP1#)	RTS# Output Control	DTR# Output Control	LCR≠0xBF
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	See **Table 13**
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	See **Table 12**
1 1 0	TCR	RD/WR	Resume Bit-3	Resume Bit-2	Resume Bit-1	Resume Bit-0	Halt Bit-3	Halt Bit-2	Halt Bit-1	Halt Bit-0	See **Table 13**
1 1 1	TLR	RD/WR	RX Trig Bit-3	RX Trig Bit-2	RX Trig Bit-1	RX Trig Bit-0	TX Trig Bit-3	TX Trig Bit-2	TX Trig Bit-1	TX Trig Bit-0	See **Table 12**
1 1 1	FIFO Rdy	RD	0	0	RX FIFO B Status	RX FIFO A Status	0	0	TX FIFO B Status	TX FIFO A Status	See **Table 12**