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GENERAL DESCRIPTION

The XR16V564¹ (V564) is an enhanced quad Universal Asynchronous Receiver and Transmitter (UART) with 32 bytes of transmit and receive FIFOs, programmable transmit and receive FIFO trigger levels, automatic hardware and software flow control, and data rates of up to 16 Mbps at 4X sampling rate. Each UART has a set of registers that provide the user with operating status and control, receiver error indications, and modem serial interface controls. An internal loopback capability allows onboard diagnostics. The V564 is available in a 48-pin QFN, 64-pin LQFP, 68-pin PLCC and 80-pin LQFP packages. The 64-pin and 80-pin packages only offer the 16 mode interface, but the 48 and 68 pin packages offer an additional 68 mode interface which allows easy integration with Motorola processors. The XR16V564IV (64-pin) offers three state interrupt output while the XR16V564DIV provides continuous interrupt output. The XR16V564 is compatible with the industry standard ST16C554 and ST16C654/654D.

NOTE: 1 Covered by U.S. Patent #5,649,122.

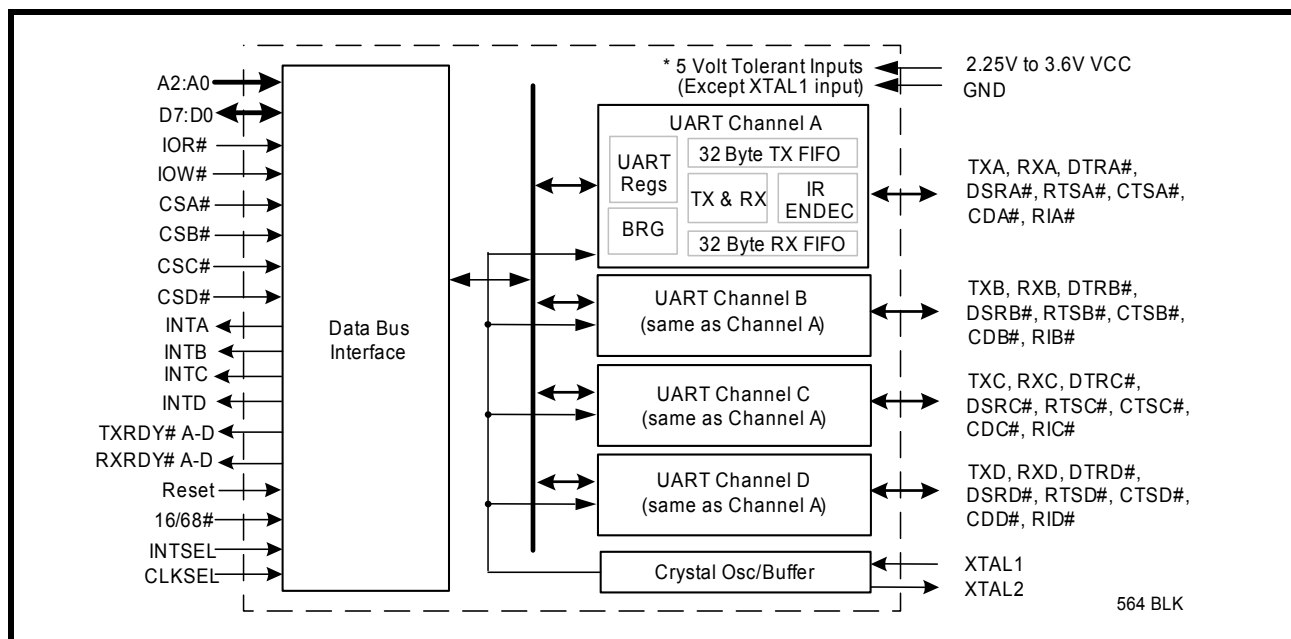
FEATURES

- Pin-to-pin compatible with ST16C454, ST16C554, TI's TL16C754B and Philip's SC16C754B
- Intel or Motorola Data Bus Interface select
- Four independent UART channels
 - Register Set Compatible to 16C550
 - Data rates of up to 16 Mbps
 - 32 byte Transmit FIFO
 - 32 byte Receive FIFO with error tags
 - 4 Selectable TX and RX FIFO Trigger Levels
 - Automatic Hardware (RTS/CTS) Flow Control
 - Automatic Software (Xon/Xoff) Flow Control
 - Programmable Xon/Xoff characters
 - Wireless Infrared (IrDA 1.0) Encoder/Decoder
 - Full modem interface
- 2.25V to 3.6V supply operation
- Sleep Mode with automatic wake-up
- Crystal oscillator or external clock input

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FIGURE 1. XR16V564 BLOCK DIAGRAM



XR16V564/564D

2.25V TO 3.6V QUAD UART WITH 32-BYTE FIFO



REV. 1.0.4

FIGURE 2. PIN OUT ASSIGNMENT FOR 68-PIN PLCC PACKAGES IN 16 AND 68 MODE AND 64-PIN LQFP PACKAGES

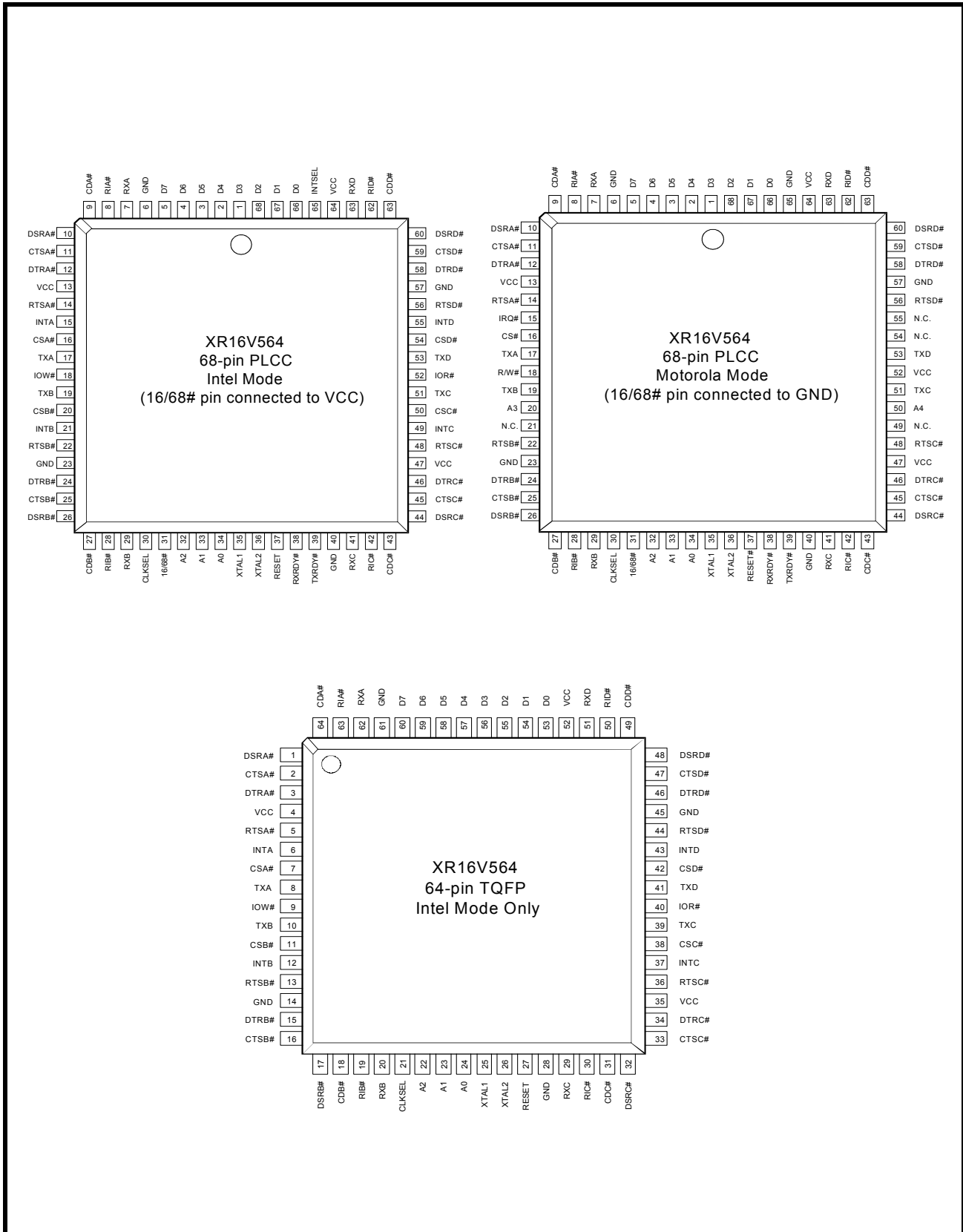
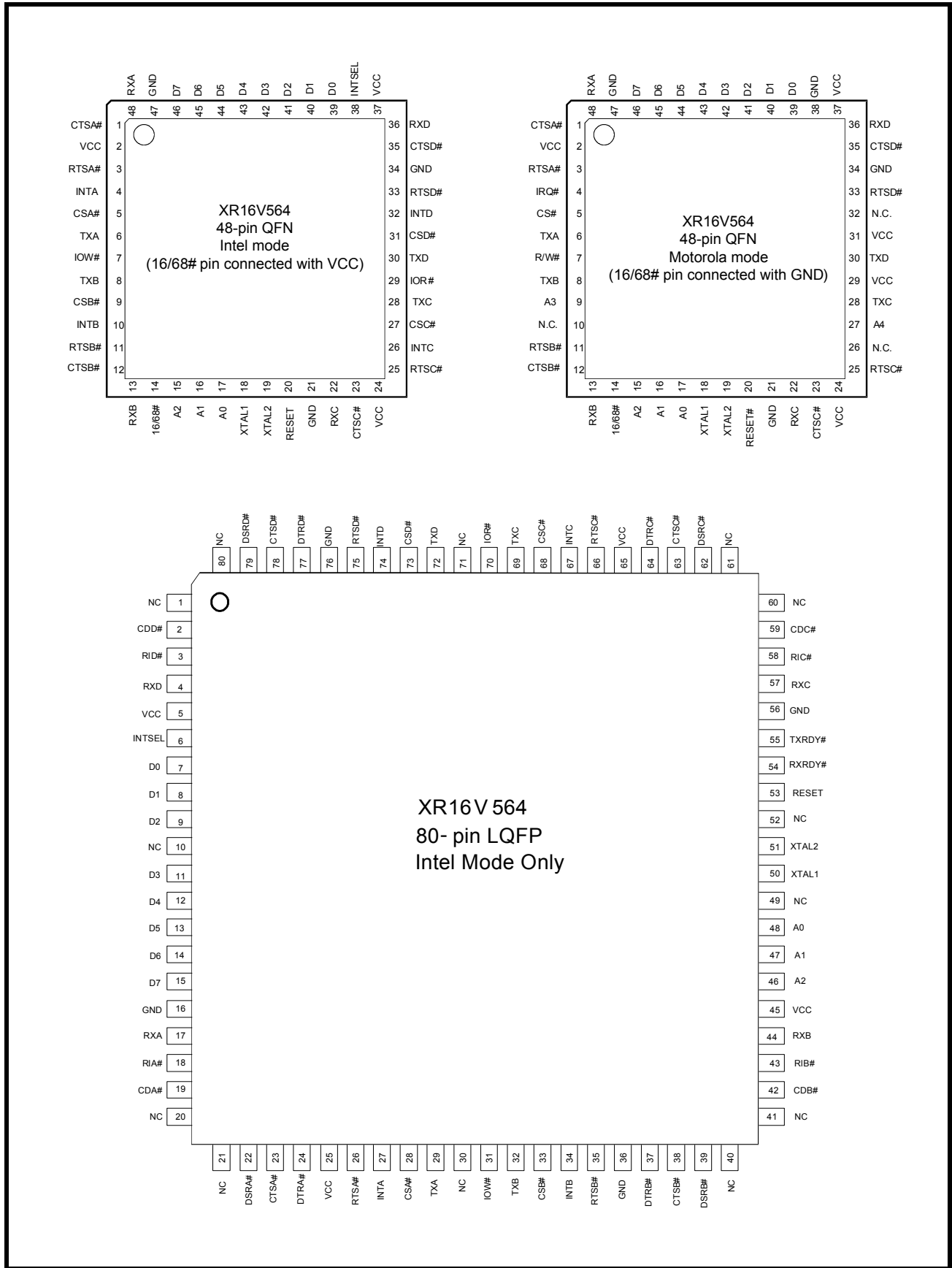


FIGURE 3. PIN OUT ASSIGNMENT FOR 48-PIN QFN PACKAGE AND 80-PIN LQFP PACKAGE



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16V564IJ	68-Lead PLCC	-40°C to +85°C	Active
XR16V564IV	64-Lead LQFP	-40°C to +85°C	Active
XR16V564DIV	64-Lead LQFP	-40°C to +85°C	Active
XR16V564IL	48-pin QFN	-40°C to +85°C	Active
XR16V564IV80	80-Lead LQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS**Pin Description**

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN #	80-LQFP PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE						
A2 A1 A0	15 16 17	22 23 24	32 33 34	46 47 48	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A-D during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	46 45 44 43 42 41 40 39	60 59 58 57 56 55 54 53	5 4 3 2 1 68 67 66	15 14 13 12 11 9 8 7	I/O	Data bus lines [7:0] (bidirectional).
IOR# (VCC)	29	40	52	70	I	When 16/68# pin is HIGH, the Intel bus interface is selected and this input becomes read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When 16/68# pin is LOW, the Motorola bus interface is selected and this input is not used and should be connected to VCC.
IOW# (R/W#)	7	9	18	31	I	When 16/68# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is LOW, the Motorola bus interface is selected and this input becomes read (logic 1) and write (LOW) signal.
CSA# (CS#)	5	7	16	28	I	When 16/68# pin is HIGH, this input is chip select A (active low) to enable channel A in the device. When 16/68# pin is LOW, this input becomes the chip select (active low) for the Motorola bus interface.

Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN #	80-LQFP PIN #	TYPE	DESCRIPTION
CSB# (A3)	9	11	20	33	I	When 16/68# pin is HIGH, this input is chip select B (active low) to enable channel B in the device. When 16/68# pin is LOW, this input becomes address line A3 which is used for channel selection in the Motorola bus interface.
CSC# (A4)	27	38	50	68	I	When 16/68# pin is HIGH, this input is chip select C (active low) to enable channel C in the device. When 16/68# pin is LOW, this input becomes address line A4 which is used for channel selection in the Motorola bus interface.
CSD# (VCC)	31	42	54	73	I	When 16/68# pin is HIGH, this input is chip select D (active low) to enable channel D in the device. When 16/68# pin is LOW, this input is not used and should be connected VCC.
INTA (IRQ#)	4	6	15	27	O (OD)	When 16/68# pin is HIGH for Intel bus interface, this output becomes channel A interrupt output. The output state is defined by the user and through the software setting of MCR[3]. INTA is set to the active mode when MCR[3] is set to a logic 1. INTA is set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3]. When 16/68# pin is LOW for Motorola bus interface, this output becomes device interrupt output (active low, open drain). An external pull-up resistor is required for proper operation.
INTB INTC INTD (N.C.)	10 26 32	12 37 43	21 49 55	34 67 74	O	When 16/68# pin is HIGH for Intel bus interface, these outputs become the interrupt outputs for channels B, C, and D. The output state is defined by the user through the software setting of MCR[3]. The interrupt outputs are set to the active mode when MCR[3] is set to a logic 1 and are set to the three state mode when MCR[3] is set to a logic 0 (default). See MCR[3]. When 16/68# pin is LOW for Motorola bus interface, these outputs are unused and will stay at logic zero level. Leave these outputs unconnected.
TXRDY#	-	-	39	55	O	Transmitter Ready (active low). This output is a logically ANDed status of TXRDY# A-D. See Table 5 . If this output is unused, leave it unconnected.
RXRDY#	-	-	38	54	O	Receiver Ready (active low). This output is a logically ANDed status of RXRDY# A-D. See Table 5 . If this output is unused, leave it unconnected.

Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN #	80-LQFP PIN #	TYPE	DESCRIPTION
INTSEL	38	-	65	6	I	Interrupt Select (active high, input with internal pull-down). When 16/68# pin is HIGH for Intel bus interface, this pin can be used in conjunction with MCR bit-3 to enable or disable the INT A-D pins or override MCR bit-3 and enable the interrupt outputs. Interrupt outputs are enabled continuously when this pin is HIGH. MCR bit-3 enables and disables the interrupt output pins. In this mode, MCR bit-3 is set to a logic 1 to enable the continuous output. See MCR bit-3 description for full detail. <u>This pin must be LOW in the Motorola bus interface mode.</u> For the 64 pin packages, this pin is bonded to VCC internally in the XR16V564D so the INT outputs operate in the continuous interrupt mode. This pin is bonded to GND internally in the XR16V564 and therefore requires setting MCR bit-3 for enabling the interrupt output pins.
MODEM OR SERIAL I/O INTERFACE						
TXA	6	8	17	29	O	UART channels A-D Transmit Data and infrared transmit data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be a HIGH during reset, or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is a logic 0.
TXB	8	10	19	32		
TXC	28	39	51	69		
TXD	30	41	53	72		
RXA	48	62	7	17	I	UART channel A-D Receive Data or infrared receive data. Normal receive data input must idle HIGH.
RXB	13	20	29	44		
RXC	22	29	41	57		
RXD	36	51	63	4		
RTSA#	3	5	14	26	O	UART channels A-D Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], and IER[6]. Also see Figure 11 . If these outputs are not used, leave them unconnected.
RTSB#	11	13	22	35		
RTSC#	25	36	48	66		
RTSD#	33	44	56	75		
CTSA#	1	2	11	23	I	UART channels A-D Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. Also see Figure 11 . These inputs should be connected to VCC when not used.
CTSB#	12	16	25	38		
CTSC#	23	33	45	63		
CTSD#	35	47	59	78		
DTRA#	-	3	12	24	O	UART channels A-D Data-Terminal-Ready (active low) or general purpose output. If these outputs are not used, leave them unconnected.
DTRB#	-	15	24	37		
DTRC#	-	34	46	64		
DTRD#	-	46	58	77		
DSRA#	-	1	10	22	I	UART channels A-D Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
DSRB#	-	17	26	39		
DSRC#	-	32	44	62		
DSRD#	-	48	60	79		

Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN #	80-LQFP PIN #	TYPE	DESCRIPTION
CDA# CDB# CDC# CDD#	- - - -	64 18 31 49	9 27 43 61	19 42 59 2	I	UART channels A-D Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIA# RIB# RIC# RID#	- - - -	63 19 30 50	8 28 42 62	18 43 58 3	I	UART channels A-D Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
ANCILLARY SIGNALS						
XTAL1	18	25	35	50	I	Crystal or external clock input. Caution: this input is not 5V tolerant.
XTAL2	19	26	36	51	O	Crystal or buffered clock output.
16/68#	14	-	31	-	I	Intel or Motorola Bus Select (input with internal pull-up). When 16/68# pin is HIGH, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When 16/68# pin is LOW, 68 or Motorola mode, the device will operate in the Motorola bus type of interface. Motorola bus interface is not available on the 64 pin package.
CLKSEL	-	21	30	-	I	Baud-Rate-Generator Input Clock Prescaler Select for channels A-D. This input is only sampled during power up or a reset. Connect to VCC for divide by 1 (default) and GND for divide by 4. MCR[7] can override the state of this pin following a reset or initialization. See MCR bit-7 and Figure 6 in the Baud Rate Generator section.
RESET (RESET#)	20	27	37	53	I	When 16/68# pin is HIGH for Intel bus interface, this input becomes the Reset pin (active high). In this case, a 40 ns minimum HIGH pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (Table 17). When 16/68# pin is at LOW for Motorola bus interface, this input becomes Reset# pin (active low). This pin functions similarly, but instead of a HIGH pulse, a 40 ns minimum LOW pulse will reset the internal registers and outputs. Motorola bus interface is not available on the 64 pin package.
VCC	2, 24, 37	4, 35, 52	13, 47, 64	5, 25, 45, 65	Pwr	2.25V to 3.6V power supply. All inputs, except XTAL1, are 5V tolerant.
GND	21, 47	14, 28, 45, 61	6, 23, 40, 57	16, 36, 56, 76	Pwr	Power supply common, ground.

Pin Description

NAME	48-QFN PIN #	64-LQFP PIN #	68-PLCC PIN #	80-LQFP PIN #	TYPE	DESCRIPTION
GND	Center Pad	N/A	N/A	N/A	Pwr	The center pad on the backside of the QFN package is metallic and should be connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.
N.C.	-	-	-	1, 10, 20, 21, 30, 40, 41, 49, 52, 60, 61, 71, 80		No Connection. These pins are not used in either the Intel or Motorola bus modes.

Pin type: I=Input, O=Output, I/O= Input/Output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The XR16V564 (V564) integrates the functions of 4 enhanced 16C550 Universal Asynchronous Receiver and Transmitter (UART). Each UART is independently controlled and has its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 32 bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, infrared encoder and decoder (IrDA ver 1.0), programmable fractional baud rate generator with a prescaler of dividing by 1 or 4, and data rate up to 16 Mbps. The XR16V564 can operate from 2.25 to 3.6 volts. The V564 is fabricated with an advanced CMOS process.

Enhanced FIFO

The V564 QUART provides a solution that supports 32 bytes of transmit and receive FIFO memory, instead of 16 bytes in the ST16C554, or one byte in the ST16C454. The V564 is designed to work with high performance data communication systems, that require fast data processing time. Increased performance is realized in the V564 by the larger transmit and receive FIFOs, FIFO trigger level control and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C554 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 32 byte FIFO in the V564, the data buffer will not require unloading/loading for 3.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

Data Rate

The V564 is capable of operation up to 16 Mbps at 3.3V with 4Xinternal sampling clock rate. The device can operate at 3.3V with a crystal oscillator of up to 24 MHz crystal on pins XTAL1 and XTAL2, or external clock source of 64 MHz on XTAL1 pin. With a typical crystal of 14.7456 MHz and through a software option, the user can set the prescaler bit and sampling rate for data rates of up to 3.68 Mbps.

Enhanced Features

The rich feature set of the V564 is available through the internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. MCR bit-5 provides a facility for turning off (Xon) software flow control with any incoming (RX) character. In the 16 mode INTSEL and MCR bit-3 can be configured to provide a software controlled or continuous interrupt capability. For backward compatibility to the ST16C654, the 64-pin LQFP does not have the INTSEL pin. Instead, two different LQFP packages are offered. The XR16V564DIV operates in the continuous interrupt enable mode by internally bonding INTSEL to VCC. The XR16V564IV operates in conjunction with MCR bit-3 by internally bonding INTSEL to GND.

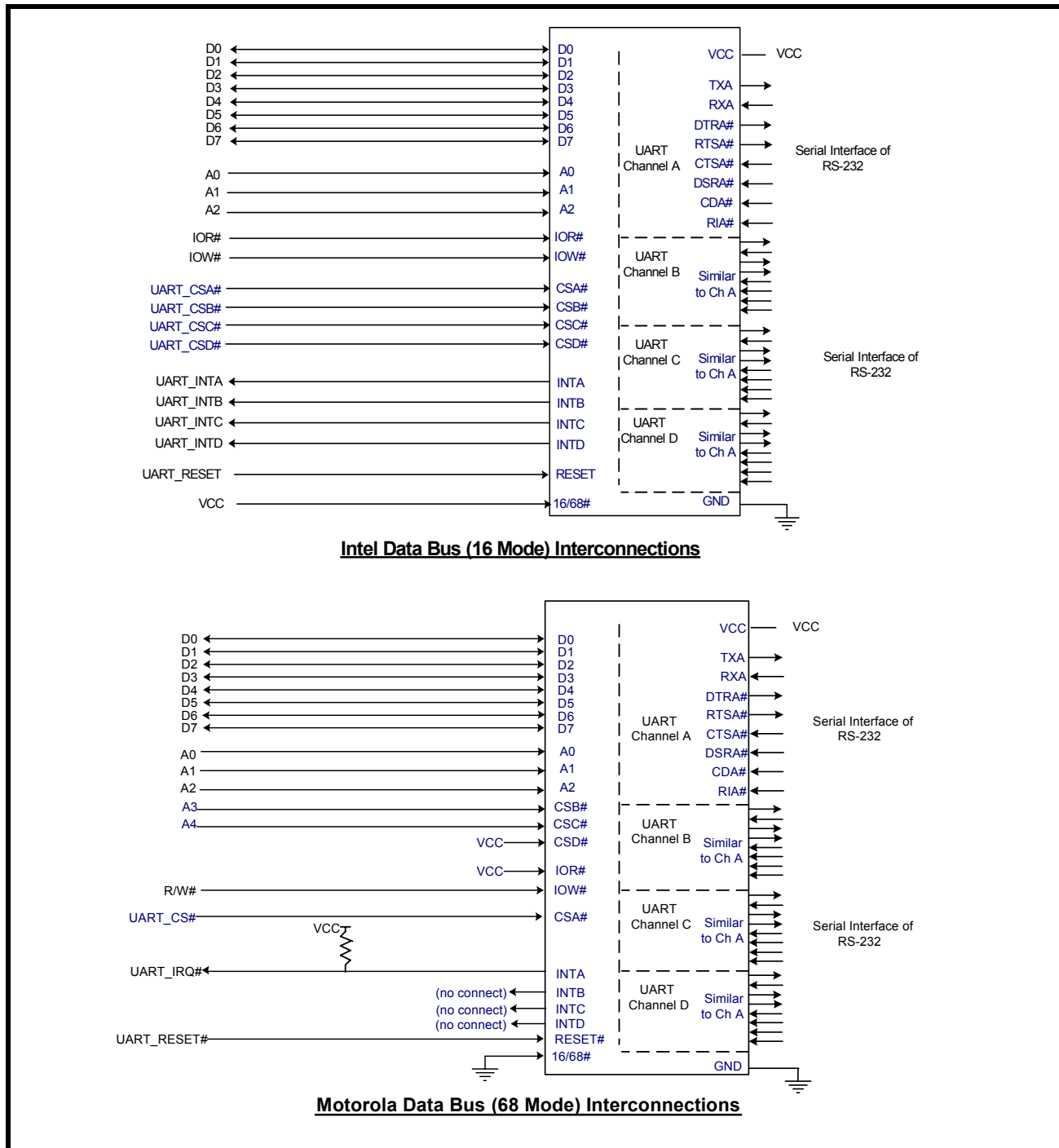
The XR16V564 offers a clock prescaler select pin to allow system/board designers to preset the default baud rate table on power up. The CLKSEL pin selects the div-by-1 or div-by-4 prescaler for the baud rate generator. It can then be overridden following initialization by MCR bit-7.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The V564 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required for a data bus transaction. Each bus cycle is asynchronous using CS# A-D, IOR# and IOW# or CS#, R/W#, A4 and A3 inputs. All four UART channels share the same data bus for host operations. A typical data bus interconnection for Intel and Motorola mode is shown in **Figure 4**.

FIGURE 4. XR16V564 TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS



2.2 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see [Table 17](#)). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device. Following a power-on reset or an external reset, the V564 is software compatible with previous generation of UARTs, 16C454 and 16C554.

2.3 Channel Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. During Intel Bus Mode (16/68# pin is connected to VCC), a LOW on chip select pins, CSA#, CSB#, CSC# or CSD# allows the user to select UART channel A, B, C or D to configure, send transmit data and/or unload receive data to/from the UART. Selecting all four UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from all four uarts simultaneously. Individual channel select functions are shown in [Table 1](#).

TABLE 1: CHANNEL A-D SELECT IN 16 MODE

CSA#	CSB#	CSC#	CSD#	FUNCTION
1	1	1	1	UART de-selected
0	1	1	1	Channel A selected
1	0	1	1	Channel B selected
1	1	0	1	Channel C selected
1	1	1	0	Channel D selected
0	0	0	0	Channels A-D selected

During Motorola Bus Mode (16/68# pin is connected to GND), the package interface pins are configured for connection with Motorola, and other popular microprocessor bus types. In this mode the V564 decodes two additional addresses, A3 and A4, to select one of the four UART ports. The A3 and A4 address decode function is used only when in the Motorola Bus Mode. [See Table 2](#).

TABLE 2: CHANNEL A-D SELECT IN 68 MODE

CS#	A4	A3	FUNCTION
1	X	X	UART de-selected
0	0	0	Channel A selected
0	0	1	Channel B selected
0	1	0	Channel C selected
0	1	1	Channel D selected

2.4 Channels A-D Internal Registers

Each UART channel in the V564 has a set of enhanced registers for controlling, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM/DLD), and a user accessible scratchpad register (SPR).

Beyond the general 16C550 features and capabilities, the V564 offers enhanced feature registers (EFR, Xon/Xoff 1, Xon/Xoff 2) that provide automatic RTS and CTS hardware flow control and automatic Xon/Xoff software flow control. All the register functions are discussed in full detail later in **“Section 3.0, UART Internal Registers” on page 25.**

2.5 INT Outputs for Channels A-D

The interrupt outputs change according to the operating mode and enhanced features setup. **Table 3 and 4** summarize the operating behavior for the transmitter and receiver. Also see **Figure 20** through **25.**

TABLE 3: INT PIN OPERATION FOR TRANSMITTER FOR CHANNELS A-D

	FCR Bit-0 = 0 (FIFO DISABLED)	FCR Bit-0 = 1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
INT Pin	LOW = a byte in THR HIGH = THR empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty

TABLE 4: INT PIN OPERATION FOR RECEIVER FOR CHANNELS A-D

	FCR Bit-0 = 0 (FIFO DISABLED)	FCR Bit-0 = 1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
INT Pin	LOW = no data HIGH = 1 byte	LOW = FIFO below trigger level HIGH = FIFO above trigger level	LOW = FIFO below trigger level HIGH = FIFO above trigger level

2.6 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document does not mean “direct memory access” but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A-D and TXRDY# A-D output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3 = 1). When the transmit and receive FIFOs are enabled and the DMA mode is disabled (FCR bit-3 = 0), the V564 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by

loading or unloading the FIFO in a block sequence determined by the programmed trigger level. The following table show their behavior. Also see [Figure 20](#) through [25](#).

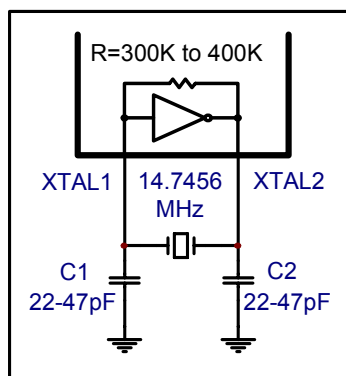
TABLE 5: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE FOR CHANNELS A-D

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR BIT-3 = 0 (DMA MODE DISABLED)	FCR BIT-3 = 1 (DMA MODE ENABLED)
RXRDY#	LOW = 1 byte HIGH = no data	LOW = at least 1 byte in FIFO HIGH = FIFO empty	HIGH to LOW transition when FIFO reaches the trigger level, or timeout occurs LOW to HIGH transition when FIFO empties
TXRDY#	LOW = THR empty HIGH = byte in THR	LOW = FIFO empty HIGH = at least 1 byte in FIFO	LOW = FIFO has at least 1 empty location HIGH = FIFO is full

2.7 Crystal Oscillator or External Clock Input

The V564 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Caution: the XTAL1 input is not 5V tolerant. For programming details, see [“Section 2.8, Programmable Baud Rate Generator with Fractional Divisor” on page 13.](#)

FIGURE 5. TYPICAL CRYSTAL CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins. Typical oscillator connections are shown in [Figure 5](#). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

2.8 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (216 - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X or 8X or 4X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to

the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon reset. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the divisor. Only the four lower bits of the DLD are implemented and they are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. **Table 6** shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in **Table 6**. At 8X sampling rate, these data rates would double. And at 4X sampling rate, they would quadruple. Also, when using 8X sampling mode, please note that the bit-time will have a jitter (+/- 1/16) whenever the DLD is non-zero and is an odd number. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal)=(XTAL1 clock frequency / prescaler) / (serial data rate x 16), with 16X mode, DLD[5:4]='00'
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 8), with 8X mode, DLD[5:4] = '01'
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 4), with 4X mode, DLD[5:4] = '10'

The closest divisor that is obtainable in the V564 can be calculated using the following formula:

$$\text{ROUND}((\text{Required Divisor} - \text{TRUNC}(\text{Required Divisor})) * 16) / 16 + \text{TRUNC}(\text{Required Divisor}), \text{ where}$$

$$\text{DLM} = \text{TRUNC}(\text{Required Divisor}) \gg 8$$

$$\text{DLL} = \text{TRUNC}(\text{Required Divisor}) \& 0xFF$$

$$\text{DLD} = \text{ROUND}((\text{Required Divisor} - \text{TRUNC}(\text{Required Divisor})) * 16)$$

In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value 'A' by 'B' number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 6. BAUD RATE GENERATOR

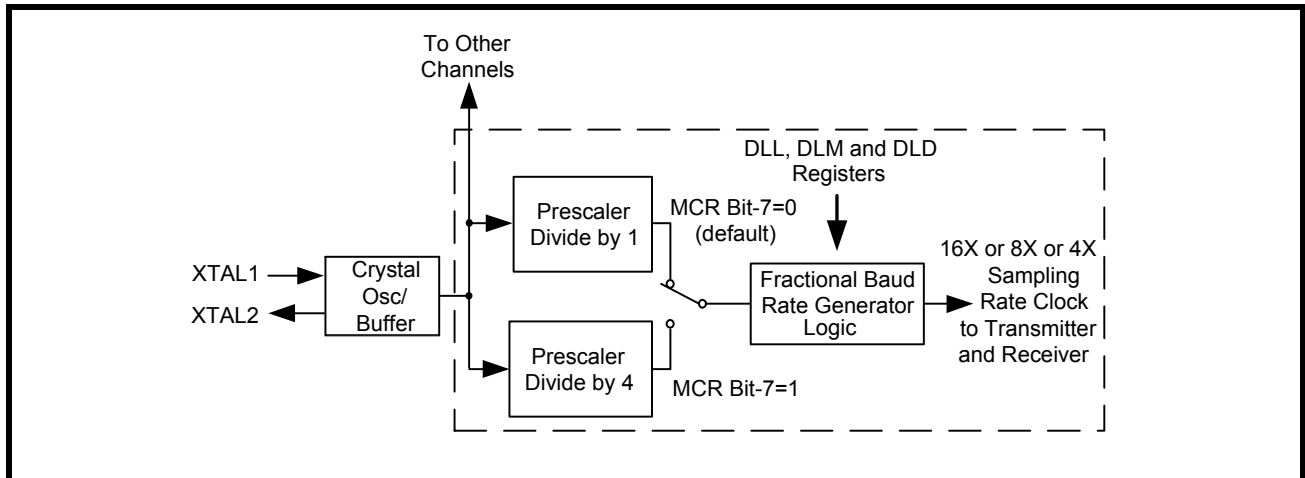


TABLE 6: TYPICAL DATA RATES WITH A 24 MHz CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	DIVISOR FOR 16x Clock (Decimal)	DIVISOR OBTAINABLE IN V2550	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DLD PROGRAM VALUE (HEX)	DATA ERROR RATE (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0
300000	5	5	0	5	0	0
400000	3.75	3 12/16	0	3	C	0
460800	3.2552	3 4/16	0	3	4	0.16
500000	3	3	0	3	0	0
750000	2	2	0	2	0	0
921600	1.6276	1 10/16	0	1	A	0.16
1000000	1.5	1 8/16	0	1	8	0

2.9 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 32 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X/4X internal clock. A bit time is 16/8/4 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

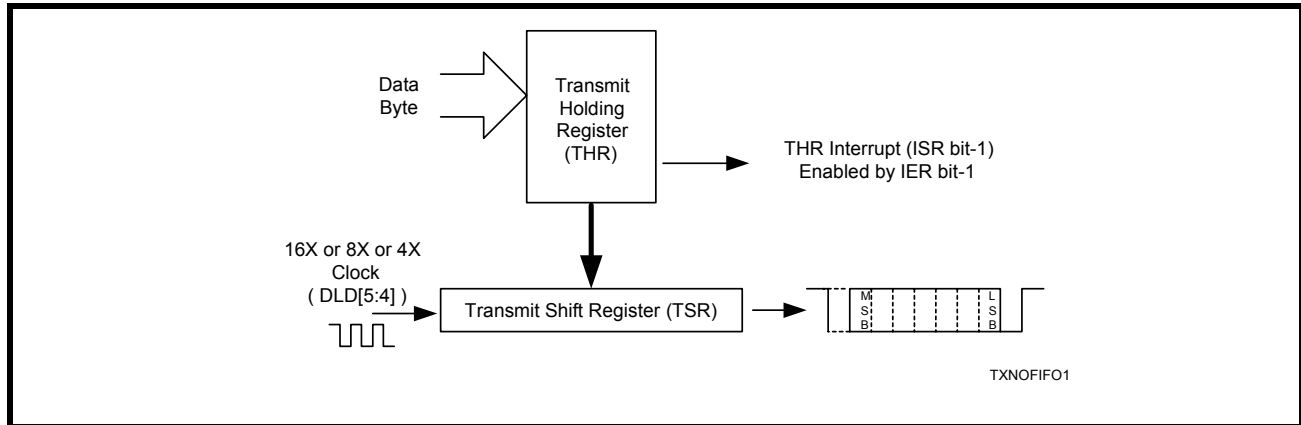
2.9.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 32 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.9.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

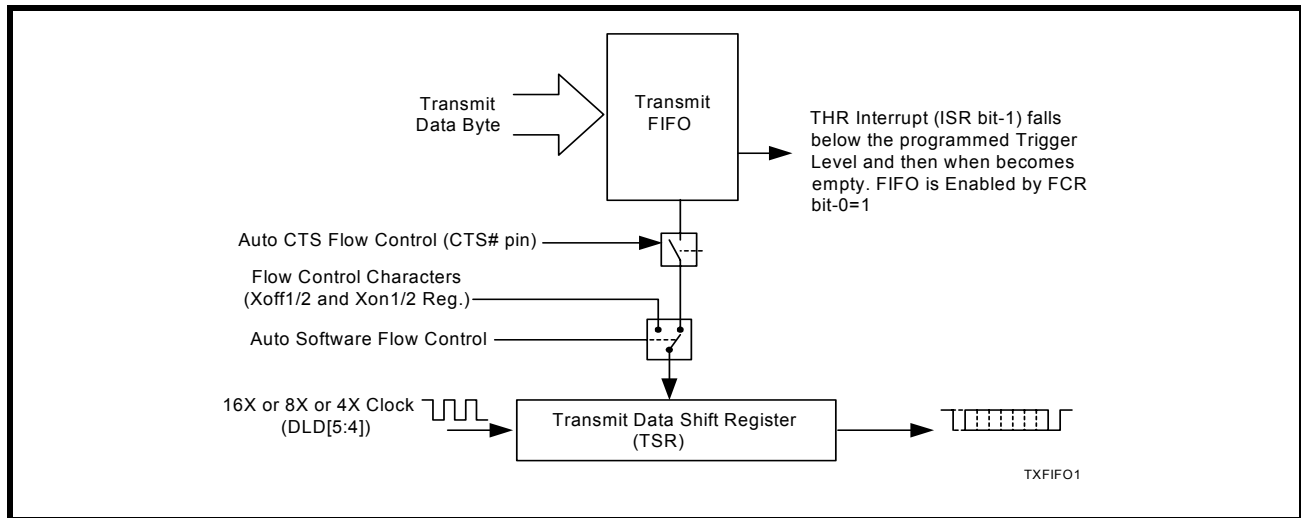
FIGURE 7. TRANSMITTER OPERATION IN NON-FIFO MODE



2.9.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 32 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the FIFO becomes empty. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 8. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.10 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 32 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X/4X clock (DLD[5:4]) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X/4X clock rate. After 8 clocks (or 4 if 8X or 2 if 4X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still LOW it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0. See **Figure 9** and **Figure 10** below.

2.10.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 32 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 9. RECEIVER OPERATION IN NON-FIFO MODE

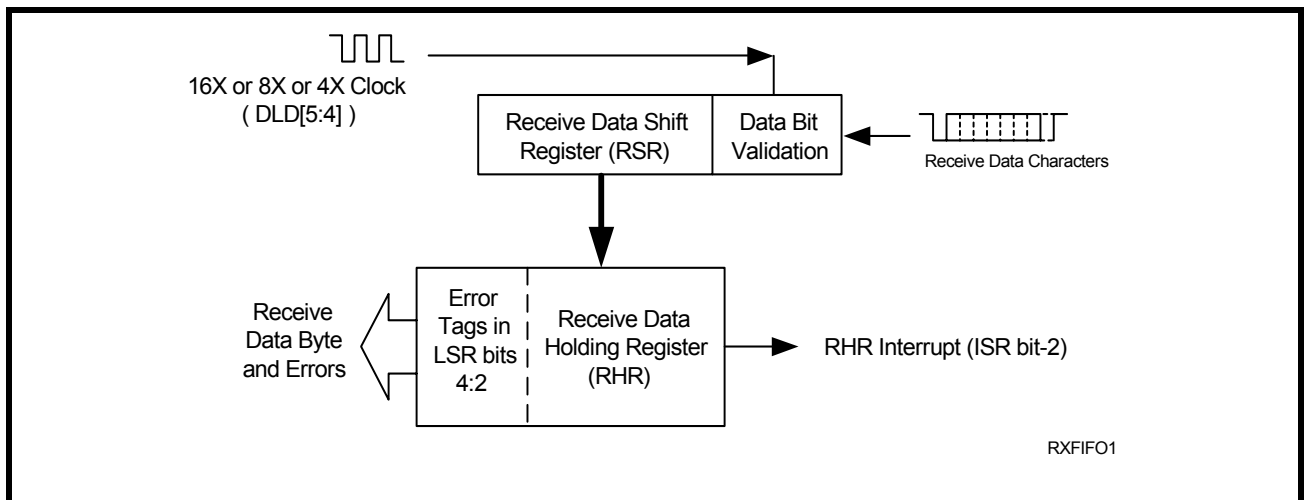
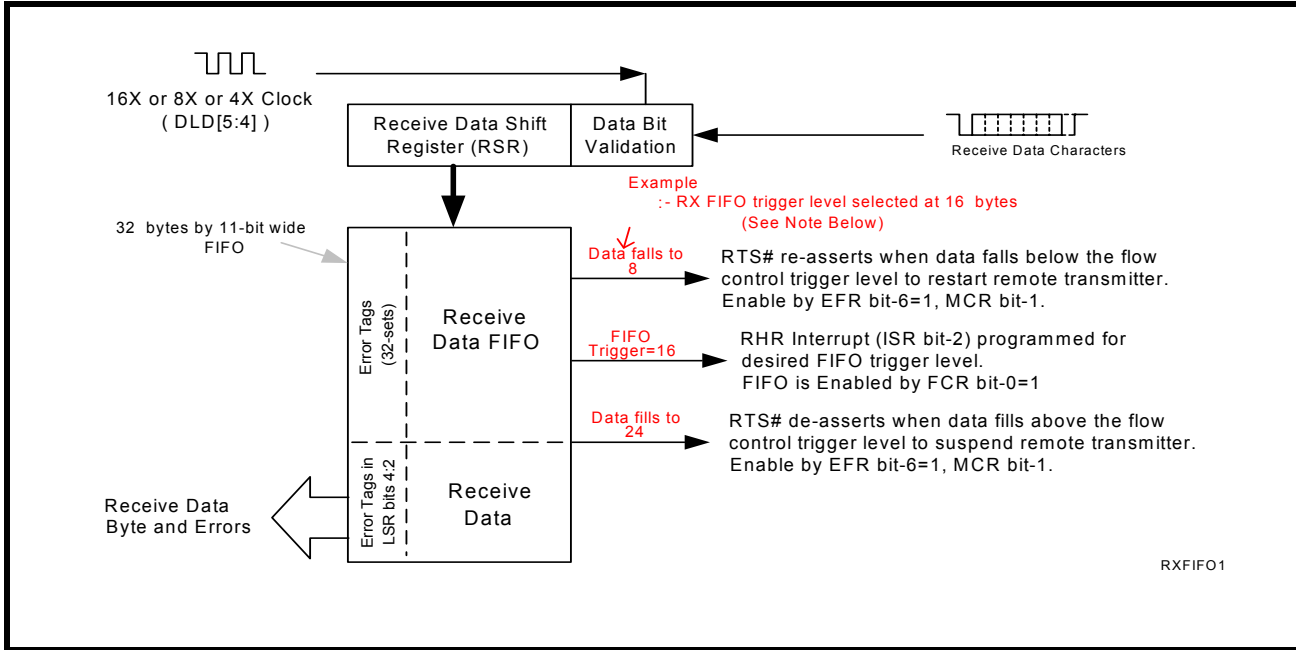


FIGURE 10. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.11 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 11**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.12 Auto RTS Hysteresis

The V564 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the XR16C850, ST16C650A and ST16C550 family of UARTs. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the selected RX trigger level. The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches one trigger level above the selected trigger level in the trigger table (**Table 12**). The RTS# pin will return LOW after the RX FIFO is unloaded to one level below the selected trigger level. Under the above described conditions, the V564 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On).

TABLE 7: AUTO RTS (HARDWARE) FLOW CONTROL

Rx TRIGGER LEVEL	INT PIN ACTIVATION	RTS# DE-ASSERTED (HIGH) (CHARACTERS IN Rx FIFO)	RTS# ASSERTED (LOW) (CHARACTERS IN Rx FIFO)
8	8	16	0
16	16	24	8
24	24	30	16
30	30	30	24

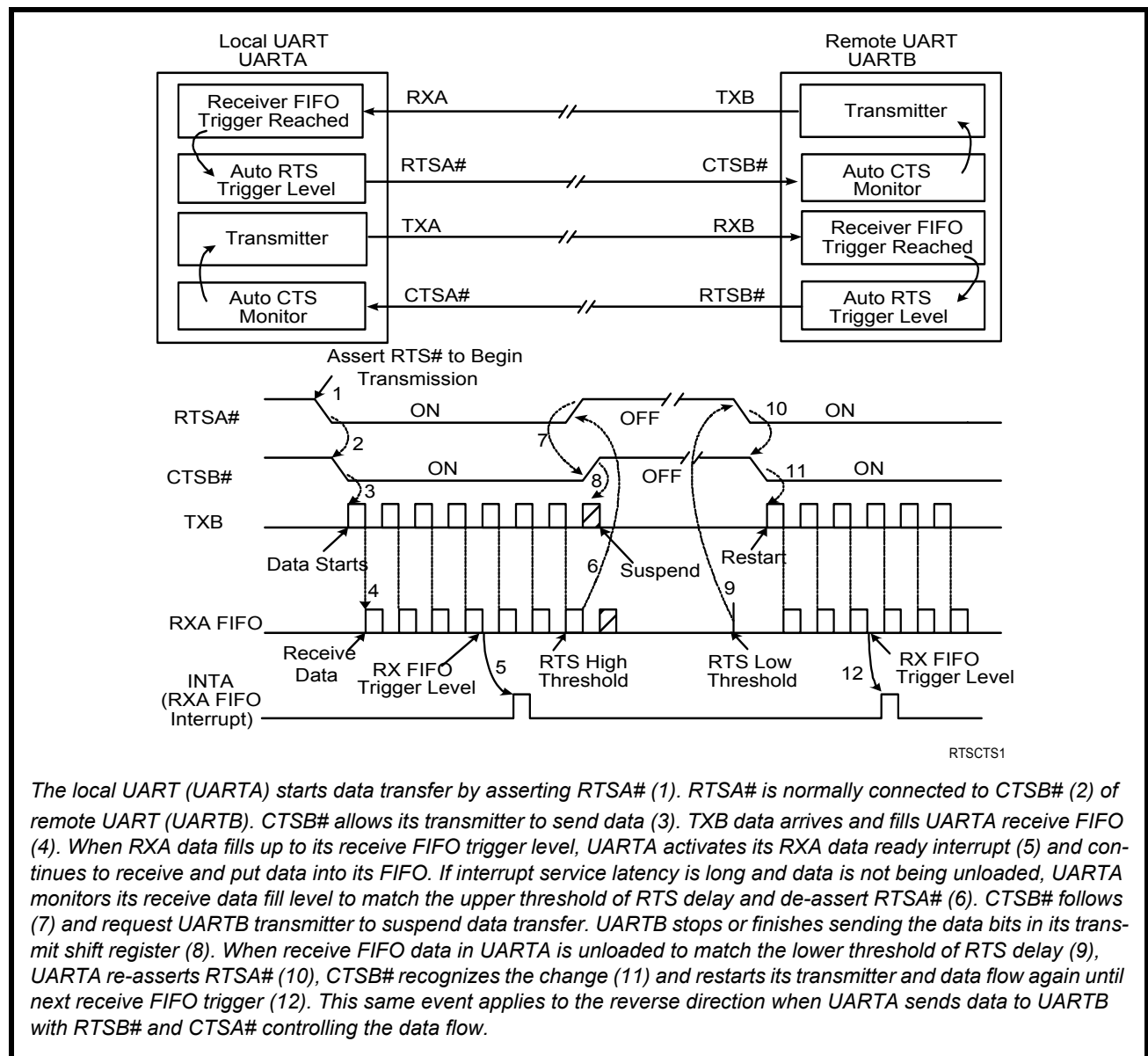
2.13 Auto CTS Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 11**):

- Enable auto CTS flow control using EFR bit-7.

If needed, the CTS interrupt can be enabled through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 11. AUTO RTS AND CTS FLOW CONTROL OPERATION



2.14 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 16), the V564 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the V564 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the V564 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the V564 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to LOW. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 16) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the V564 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overflowing and flow control needs to be executed, the V564 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The V564 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the V564 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level. Table 8 below explains this.

TABLE 8: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
30	30	30*	24

* After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.

2.15 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The V564 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

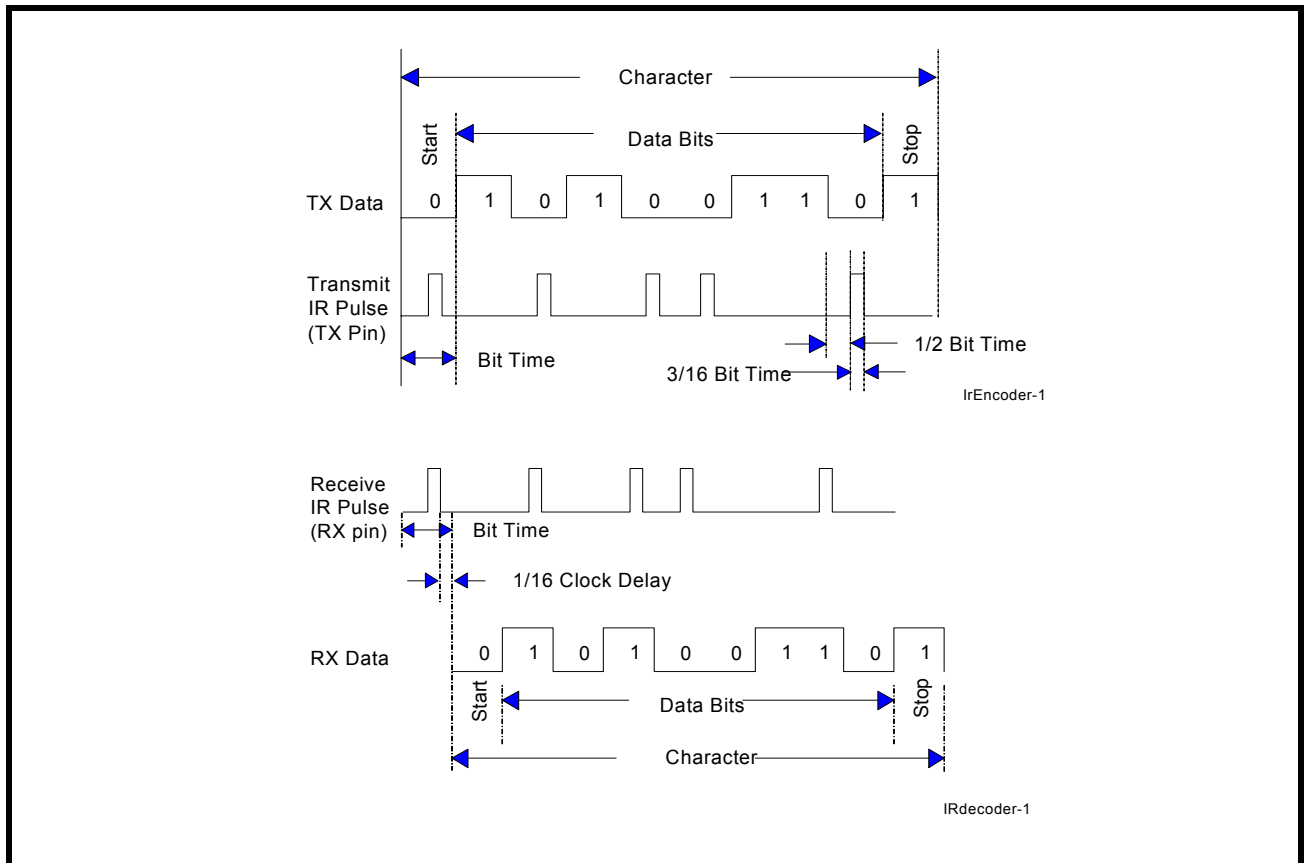
2.16 Infrared Mode

The V564 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 12** below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see **Figure 12**.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns HIGH to the data bit stream.

FIGURE 12. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.17 Sleep Mode with Auto Wake-Up

The V564 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the V564 to enter sleep mode:

- no interrupts pending for all four channels of the V564 (ISR bit-0 = 1)
- sleep mode of all channels are enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idling HIGH

The V564 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The V564 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the V564 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the V564 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The V564 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

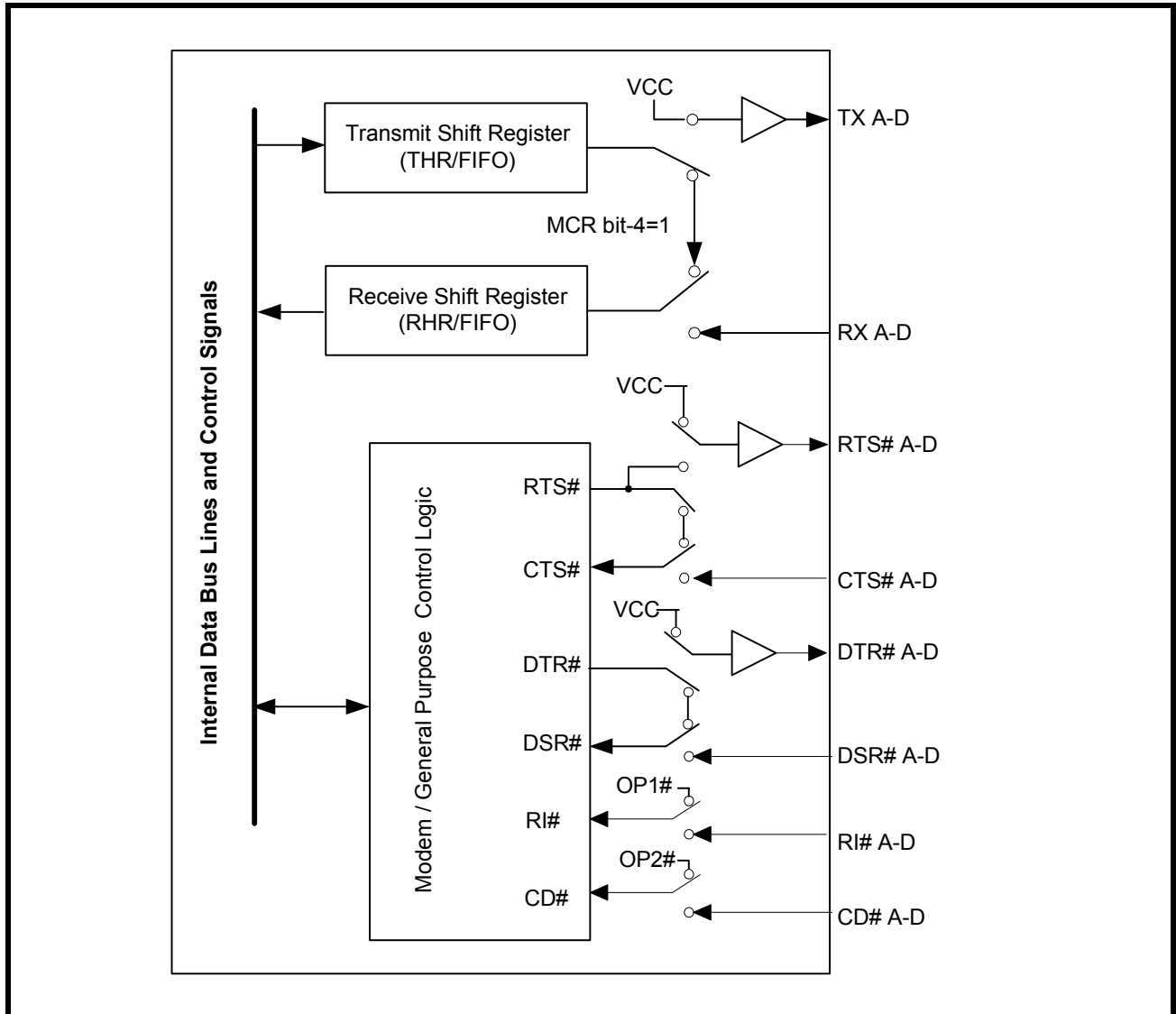
If the address lines, data bus lines, IOW#, IOR#, CSA#, CSB#, CSC#, CSD# and modem input lines remain steady when the V564 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on [page 41](#). If the input lines are floating or are toggling while the V564 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX A-D pins are idling HIGH or “marking” condition during sleep mode. This may not occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on each of the RX A-D inputs.

2.18 Internal Loopback

The V564 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. [Figure 13](#) shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held HIGH or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 13. INTERNAL LOOP BACK



3.0 UART INTERNAL REGISTERS

Each UART channel in the V564 has its own set of configuration registers selected by address lines A0, A1 and A2 with a specific channel selected (See [Table 1](#) and [Table 2](#)). The complete register set is shown on [Table 9](#) and [Table 10](#).

TABLE 9: UART INTERNAL REGISTERS

A2,A1,A0 ADDRESSES	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor MSB	Read/Write	
0 1 0	DLD - Divisor Fractional	Read/Write	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR[7] = 0
1 0 1	LSR - Line Status Register	Read/Write	
1 1 0	MSR - Modem Status Register	Read/Write	
1 1 1	SPR - Scratch Pad Register	Read/Write	
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Reg	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	

TABLE 10: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS# Int. Enable	0/ RTS# Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RXLine Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ RTS CTS Int	0/ Xoff Int	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres- caler	0/ IR Mode ENable	0/ Xon Any	Internal Lopback Enable	INT Out- put Enable (OP2#)	Rsvd (OP1#)	RTS# Output Control	DTR# Output Control	LCR[7] = 0
1 0 1	LSR	RD/WR	RXFIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Over- run Error	RX Data Ready	
1 1 0	MSR	RD/WR	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR≠0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 1 0	DLD	RD/WR	Rsvd	Rsvd	4X Mode	8X Mode	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7] = 1 LCR≠0xBF EFR[4] = 1