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GENERAL DESCRIPTION

The XR17C152[1] (152) is a monolithic dual PCI Bus Universal Asynchronous Receiver and Transmitter (UART) in Exar's PCI Bus UART family. The device is designed to meet today's 32-bit PCI Bus and high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for both channels to speed up interrupt parsing. Each UART is independently controlled and has its own 16C550 compatible 5G (Fifth Generation) register set, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO trigger levels, transmit and receive FIFO level counters, automatic hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, automatic half-duplex control output, wireless IrDA (Infrared Data Association) infrared encoder/decoder, 8 multi-purpose definable inputs/outputs, and a 16-bit general purpose timer/counter.

NOTE: *1 Covered by U.S. Patents #5,649,122, #5,949,787*

APPLICATIONS

- Network Management
- Factory Automation and Process Control
- Ethernet Network to Serial Ports
- Point-of-Sale Systems
- Remote Access Servers
- Multi serial ports RS-232/RS-422/RS-485 Cards

FEATURES

- High Performance Dual PCI UART
- PCI Bus 2.2 Target Interface Compliance
- 5V PCI Bus Compliant up to 33MHz Clock
- 32-bit PCI Bus Interface with EEPROM Interface
- A Global Interrupt Source Register for both UARTs
- Data Transfer in Byte, Word and Double-word
- Data Read/Write Burst Operation
- Each UART is independently controlled with:
  - •16C550 Compatible 5G Register Set
  - •64-byte Transmit and Receive FIFOs
  - •Transmit and Receive FIFO Level Counters
  - •Automatic RTS/CTS or DTR/DSR Flow Control
  - •Automatic Xon/Xoff Software Flow Control
  - •Automatic RS485 Half-duplex Control Output with 16 Selectable Turn-around Delay
  - •Infrared (IrDA 1.0) Data Encoder/Decoder
  - •Programmable Data Rate with Prescaler
  - •Up to 6.25 Mbps Serial Data Rate at 5V and 8X Sampling
- Eight Multi-Purpose Inputs/outputs
- A General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up Indicator
- Same package and pinout as the XR17D152 (14x14x1.0mm TQFP package)

FIGURE 1. BLOCK DIAGRAM

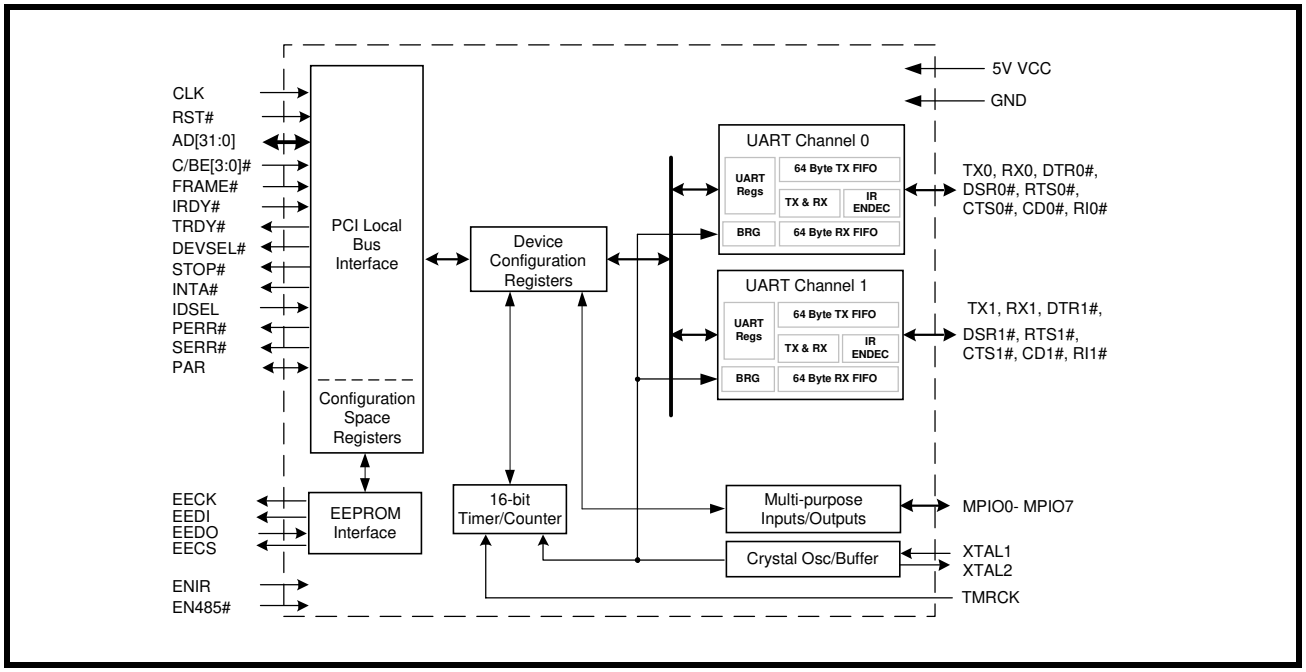
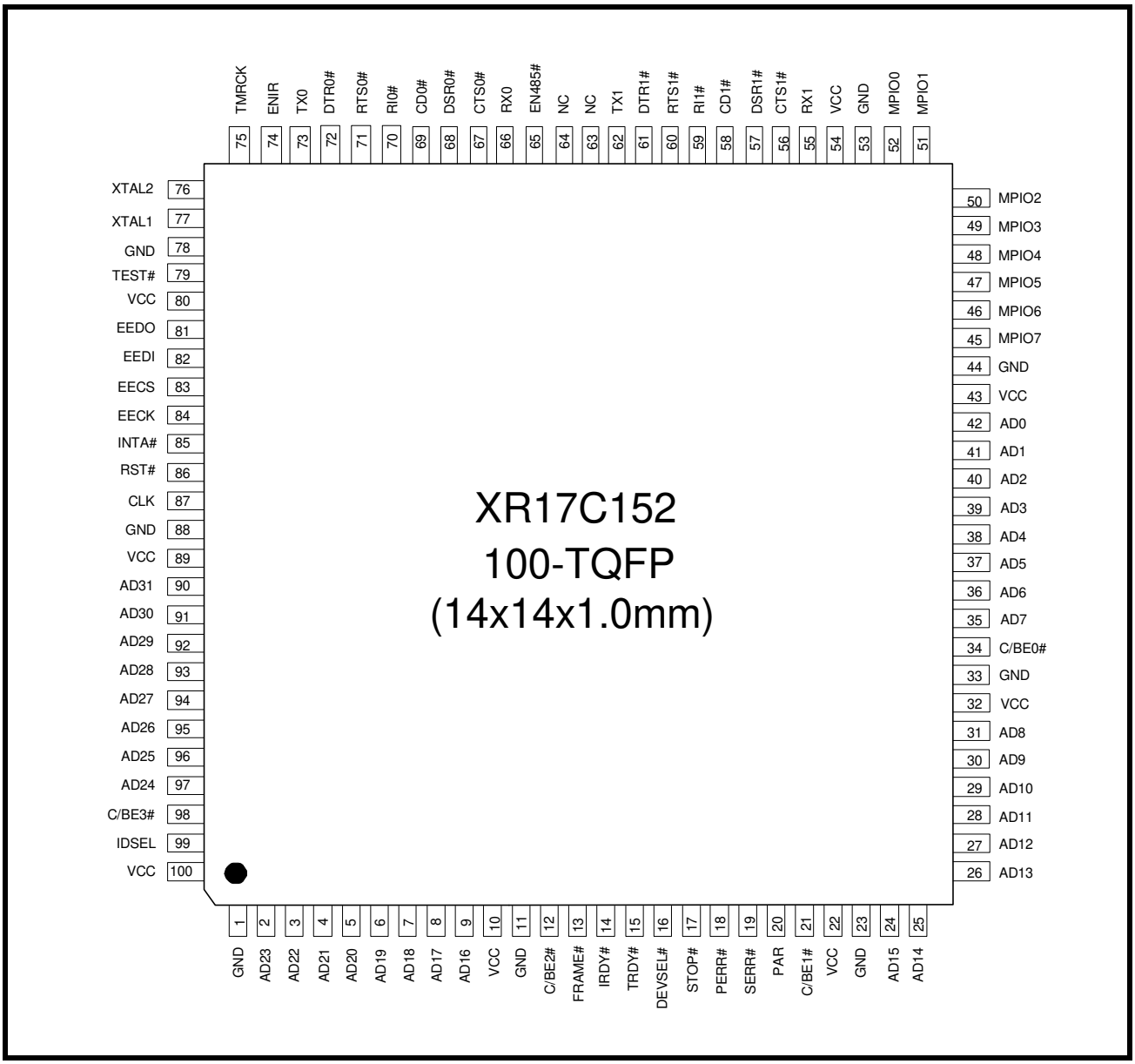


FIGURE 2. PIN OUT OF THE DEVICE



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR17C152CM	100-Lead TQFP	0°C to +70°C	Active
XR17C152IM	100-Lead TQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	PIN #	TYPE	DESCRIPTION
PCI LOCAL BUS INTERFACE			
RST#	86	I	Bus reset input (active low). It resets the PCI local bus configuration space registers, device configuration registers and UART channel registers to the default condition, see Table 19 on page 48.
CLK	87	I	Bus clock input of up to 33MHz at 5V.
AD31-AD24, AD23-AD16, AD15-AD8, AD7-AD0	90-97, 2-9, 24-31, 35-42	I/O	Address data lines [31:0] (bidirectional).
FRAME#	13	I	Bus transaction cycle frame (active low). It indicates the beginning and duration of an access.
C/BE3#-C/BE0#	98, 12, 21, 34	I	Bus Command/Byte Enable [3:0] (active low). This line is multiplexed for bus Command during the address phase and Byte Enables during the data phase.
IRDY#	14	I	Initiator Ready (active low). During a write, it indicates that valid data is present on data bus. During a read, it indicates the master is ready to accept data.
TRDY#	15	O	Target Ready (active low).
STOP#	17	O	Target request to stop current transaction (active low).
IDSEL	99	I	Initialization device select (active high).
DEVSEL#	16	O	Device select to the XR17C152 (active low).
INTA#	85	OD	Device interrupt from XR17C152 (open drain, active low).
PAR	20	I/O	Parity is even across AD[31:0] and C/BE[3:0]# (bidirectional, active high).
PERR#	18	O	Data Parity error indicator, except for Special Cycle transactions (active low). Optional in bus target application.
SERR#	19	OD	System error indicator, Address parity or Data parity during Special Cycle transactions (open drain, active low). Optional in bus target application.
MODEM OR SERIAL I/O INTERFACE			
TX0	73	O	UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX0	66	I	UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS0#	71	O	UART channel 0 Request to Send or general purpose output (active low). If this output is not used, leave it unconnected.
CTS0#	67	I	UART channel 0 Clear to Send or general purpose input (active low). This input should be connected to VCC when not used.
DTR0#	72	O	UART channel 0 Data Terminal Ready or general purpose output (active low). If this output is not used, leave it unconnected.
DSR0#	68	I	UART channel 0 Data Set Ready or general purpose input (active low). This input should be connected to VCC when not used.
CD0#	69	I	UART channel 0 Carrier Detect or general purpose input (active low). This input should be connected to VCC when not used.

Pin Description

NAME	PIN #	TYPE	DESCRIPTION
RI0#	70	I	UART channel 0 Ring Indicator or general purpose input (active low). This input should be connected to VCC when not used.
TX1	62	O	UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX1	55	I	UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS1#	60	O	UART channel 1 Request to Send or general purpose output (active low). If this output is not used, leave it unconnected.
CTS1#	56	I	UART channel 1 Clear to Send or general purpose input (active low). This input should be connected to VCC when not used.
DTR1#	61	O	UART channel 1 Data Terminal Ready or general purpose output (active low). If this output is not used, leave it unconnected.
DSR1#	57	I	UART channel 1 Data Set Ready or general purpose input (active low). This input should be connected to VCC when not used.
CD1#	58	I	UART channel 1 Carrier Detect or general purpose input (active low). This input should be connected to VCC when not used.
RI1#	59	I	UART channel 1 Ring Indicator or general purpose input (active low). This input should be connected to VCC when not used.
ANCILLARY SIGNALS			
MPIO0-MPIO7	52-45	I/O	Multi-purpose inputs/outputs 0-7. The function of these pin are defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT
EECK	84	O	Serial clock to EEPROM. An internal clock of CLK divide by 256 is used for reading the vendor and sub-vendor ID during power up or reset. However, it can be manually clocked thru the Configuration Register REGB.
EECS	83	O	Chip select to a EEPROM device like 93C46. It is manually selectable thru the Configuration Register REGB. Requires a pull-up 4.7K ohm resister for external sensing of EEPROM during power up. See DAN112 for further details.
EEDI	82	O	Write data to EEPROM device. It is manually accessible thru the Configuration Register REGB. The 152 auto-configuration register interface logic uses the 16-bit format.
EEDO	81	I	Read data from EEPROM device. It is manually accessible thru the Configuration Register REGB.
XTAL1	77	I	Crystal or external clock input of up to 50MHz for data rate of 3.125Mbps at 5V. See AC Characterization table.
XTAL2	76	O	Crystal or buffered clock output.
TMRCK	75	I	16-bit timer/counter external clock input.
ENIR	74	I	Global Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up both UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART. Software can override this pin thereafter and enable or disable it.
EN485#	65	I	Global AutoRS485 half-duplex direction control enable (active low). During power up or reset, this pin is sampled and if it is a logic high, both UARTs are set for Auto RS485 Mode. Also, the Auto RS485 bit, FCTR[5], is set in both channels. Software can override this pin thereafter and enable or disable it.

Pin Description

NAME	PIN #	TYPE	DESCRIPTION
TEST#	79	I	Factory Test. Connect to VCC for normal operation.
VCC	10, 22, 32, 43, 54, 80, 89, 100	PWR	+5V (PCI Compliance). See the electrical characteristics for details.
GND	1, 11, 23, 33, 44, 53, 78, 88	PWR	Power supply common, ground.
NC	63, 64		No Connection.

NOTE: *Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.*

FUNCTIONAL DESCRIPTION

The XR17C152 (152) integrates the functions of 2 enhanced 16550 UARTs with the PCI Local Bus interface and a non-volatile memory interface for PCI bus's plug-and-play auto-configuration, a 16-bit timer/counter, 8 multi-purpose inputs/outputs, and an on-chip oscillator. The PCI local bus is a synchronous timing bus where all bus transactions are associated to the bus clock of up to 33 MHz. The 152 supports 32-bit wide read and write data transfer operations including data burst mode through the PCI Local Bus interface. Read and write data operations may be in byte, word or double-word (DWORD) format. The data transfer rate in a DWORD operation is 4 times faster than the single byte operation with 8-bit ISA bus. A single 32-bit interrupt status register provides interrupts status for both UARTs, timer/counter, multipurpose inputs/outputs, and a special sleep wake up indicator. There are three sets of registers in the device. First, the PCI local bus configuration registers for PCI auto configuration. A set of device configuration registers for overall control, 32-bit wide transmit and receive data transfer, and monitoring of the 2 UART channels. Lastly, each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status, and byte wide data transfer. See electrical characteristics table for more details.

Each UART has the fifth generation (5G) register set, 64-byte FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger level, FIFO level counters, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of 1X or 4X, and data rate up to 3 Mbps. The XR17C152 bus timing and drive capability meets the PCI local bus specification revision 2.2 for 5 volt 33 MHz operation over the temperature range. For a pin-to-pin compatible part that can operate at 3.3V, see the XR17D152.

PCI LOCAL BUS INTERFACE

This is the host interface and it meets the PCI Local Bus Specification revision 2.2. The PCI local bus operations are synchronous meaning each transaction is associated to the bus clock. The XR17C152 can operate with the bus clock of up to a 33.34 MHz. Data transfers operation can be formatted in 8-bit, 16-bit, 24-bit or 32-bit wide. With 32-bit data operations, it pushes the data transfer rate on the bus up to 132 MByte/sec. This increases the overall system's communication performance up to 16 times better than the 8-bit ISA bus. See PCI local bus specification revision 2.2 for bus operation details.

PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

A set of PCI local bus configuration space register is provided. These registers provide the PCI local bus operating system with the card's vendor ID, device ID, sub-vendor ID, product model number, and resources and capabilities. The PCI local bus operating system collects this data from all the cards on the bus during the auto configuration phase that follows immediately after a power up or system reset/reboot. After it has sorted out all devices on the bus, it defines and download the operating conditions to the cards. One of the definitions is the base address loaded into the Base Address Register (BAR) where the card will be operating in the PCI local bus memory space.

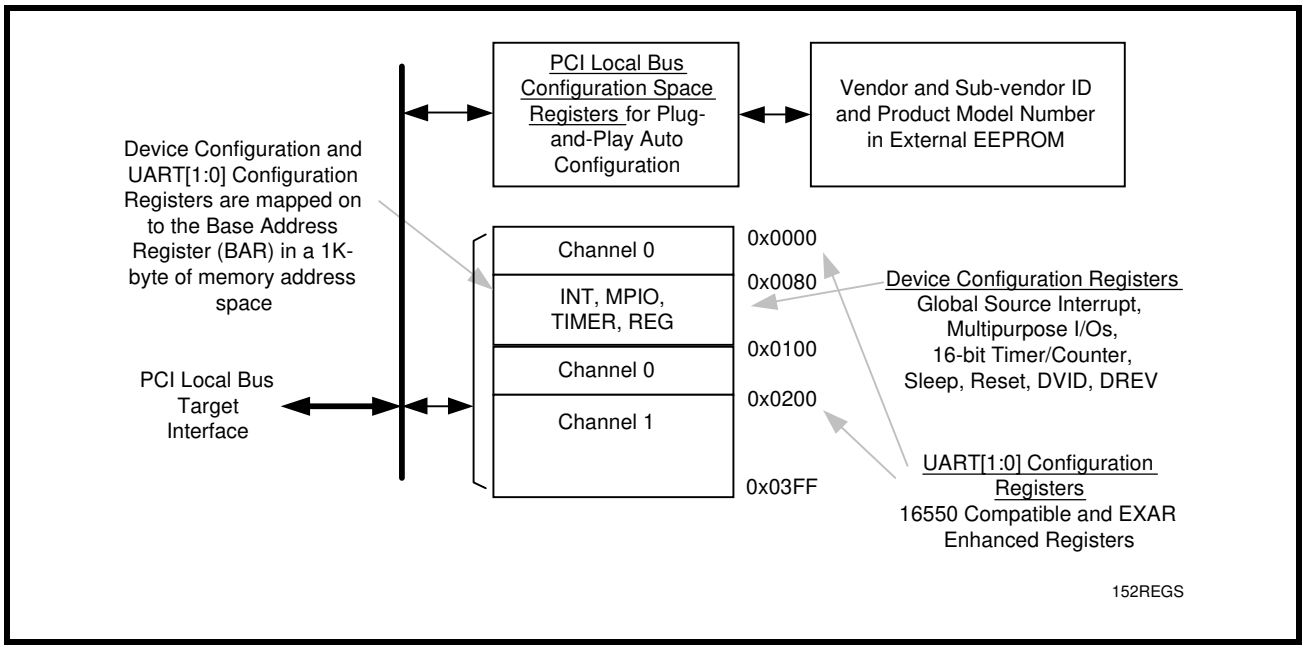
EEPROM INTERFACE

An external 93C46 EEPROM is only used to store the vendor's ID and model number, and the sub-vendor's ID and product model number. This information is only used with the plug-and-play auto configuration of the PCI local bus. These data provide automatic hardware installation onto the PCI bus. The EEPROM interface consists of 4 signals, EEDI, EEDO, EECS, and EECK. The EEPROM is not needed when auto configuration is not required in the application. However, if your design requires non-volatile memory for other purpose. It is possible to store and retrieve data on the EEPROM through a special PCI device configuration register. See application note DAN112 for its programming details.

1.0 XR17C152 REGISTERS

The XR17C152 UART has three different sets of registers as shown in Figure 3. The PCI local bus configuration space registers are for plug-and-play auto-configuration when connecting the device to the PCI bus. This auto-configuration feature makes installation very easy into a PCI system and it is part of the PCI local bus specification. The second register set is the device configuration registers that are accessible directly from the PCI bus for programming general operating conditions of the device and monitoring the status of various functions. These registers are mapped into 1K of the PCI bus memory address space. These functions include both channel UART's interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode, soft-reset, and device identification and revision. And lastly, each UART channel has its own set of 5G internal UART configuration registers for its own operation control and status reporting. Both sets of channel registers are embedded inside the device configuration registers space, which provides faster access. The following paragraphs describe all 3 sets of registers in detail.

FIGURE 3. THE XR17C152 REGISTER SETS



1.1 PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

The PCI local bus configuration space registers are responsible for setting up the device's operating environment in the PCI local bus. The pre-defined operating parameters of the device are read by the PCI bus plug-and-play auto-configuration manager in the operating system. After the PCI bus has collected all data from every device/card on the bus, it defines and downloads the memory mapping information to each device/card about their individual operation memory address location and conditions. The operating memory mapped address location is downloaded into the Base Address Register (BAR) register, 0x10. The plug-and-play auto configuration feature is only available when an external 93C46 EEPROM is used. The EEPROM contains the device vendor and sub-vendor data required by the auto-configuration setup.

TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX)
0x00	31:16	RWR[1]	Device ID (Exar device ID number or from EEPROM)	0x0152
	15:0	RWR[1]	Vendor ID (Exar ID or from EEPROM) assigned by PCISIG	0x13A8
0x04	31 30 29:28	RWC RWC RO	Parity error detected. Cleared by writing a logic 1. System error detected. Cleared by writing a logic 1. Unused	0000
	27	R-Reset	Target Abort. Set whenever 152 terminates with a target abort.	0
	26:25	RO	DEVSEL# timing.	00
	24	RO	Unimplemented bus master error reporting bit	0
	23	RO	Fast back to back transactions are supported	1
	22:16	RO	Reserved Status bits	000 0000
	15:9,7, 5,4,3,2	RO	Command bits (reserved)	0x0000
	8	RWR	SERR# driver enable. Logic 1=enable driver and 0=disable driver	0
	6	RWR	Parity error enable. Logic 1=respond to parity error and 0=ignore	0
	1	RWR	Command controls a device's response to mem space accesses: 0=disable mem space accesses, 1=enable mem space accesses	0
	0	RO	Command controls a device's response to I/O space accesses: 0 = disable I/O space accesses 1 = enable I/O space accesses	0
0x08	31:8	RO	Class Code (Simple 550 Communication Controller).	0x070002
	7:0	RO	Revision ID (Exar device revision number)	Current Rev. value
0x0C	31:24	RO	BIST (Built-in Self Test)	0x00
	23:16	RO	Header Type (a single function device with one BAR)	0x00
	15:8	RO	Unimplemented Latency Timer (needed only for bus master)	0x00
	7:0	RO	Unimplemented Cache Line Size	0x00
0x10	31:10	RWR	Memory Base Address Register (BAR)	0x00 00 00
	9:0	RO	Claims a 1K address space for the memory mapped UARTs	00 0000 0000
0x14	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000

TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX)
0x18h	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x1C	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x20	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x24	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x28	31:0	RO	Reserved	0x00000000
0x2C	31:16	RWR[1]	Subsystem ID (write from external EEPROM by customer)	0x0000
	15:0	RWR[1]	Subsystem Vendor ID (write from external EEPROM by customer)	0x0000
0x30	31:0	RO	Expansion ROM Base Address (Unimplemented)	0x00000000
0x34	31:0	RO	Reserved (returns zeros)	0x00000000
0x38	31:0	RO	Reserved (returns zeros)	0x00000000
0x3C	31:24	RO	Unimplemented MAXLAT	0x00
	23:16	RO	Unimplemented MINGNT	0x00
	15:8	RO	Interrupt Pin, use INTA#.	0x01
	7:0	RWR	Interrupt Line.	0xXX

NOTE: RWR[1]=Read/Write from external EEPROM. RWR=Read/Write from AD[31:0]. RO= Read Only. WO=Write Only.

1.2 Device configuration Register Set

The device configuration registers and a special way to access each of the UART's transmit and receive data FIFOs are accessible directly from the PCI data bus. This provides easy programming of general operating parameters to the 152 UART and for monitoring the status of various functions. The registers occupy 1K of PCI bus memory address space. These addresses are offset onto the basic memory address, a value loaded into the Memory Base Address Register (BAR) in the PCI local bus configuration register set. These registers control or report on both channel UARTs functions that include interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode control, soft-reset control, and device identification and revision, and others.

The registers set is mapped into 2 address blocks where each UART channel occupies 512 bytes memory space for its own 16550 compatible configuration registers. The device configuration and control registers are embedded inside the UART channel zero's address space between 0x0080 to 0x0093. All these registers can be accessed in 8, 16, 24 or 32 bit width depending on the starting address given by the host at beginning of the bus cycle. Transmit and receive data may be loaded or unloaded in 8, 16, 24 or 32 bit format to the register's address. Every time a read or write operation is made to the transmit or receive register, its FIFO data pointer is automatically bumped to the next sequential data location either in byte, word or dword. One special case applies to the receive data unloading when reading the receive data together with its LSR register content. The host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error tags.

TABLE 2: XR17C152 DEVICE CONFIGURATION REGISTERS

OFFSET ADDRESS	MEMORY SPACE	READ/WRITE	DATA WIDTH	COMMENT
0x000 - 0x00F	UART channel 0 Regs	(Table 10 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0x010 - 0x07F	Reserved			
0x080 - 0x093	DEVICE CONFIG. REGISTERS	(Table 3)	8/16/24/32	
0x094 - 0x0FF	Reserved	Read/Write		
0x100 - 0x13F	UART 0 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0x100 - 0x13F	UART 0 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0x140 - 0x17F	Reserved			
0x180 - 0x1FF	UART 0 – Read FIFO with status	Read-Only	16/32	64 bytes of RX FIFO data + 64 bytes of LSR status information
0x200 - 0x20F	UART channel 1 Regs	(Table 10 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0x210 - 0x2FF	Reserved	Read/Write		
0x300 - 0x33F	UART 1 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0x300 - 0x33F	UART 1 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0x340 - 0x37F	Reserved			
0x380 - 0x3FF	UART 1 – Read FIFO with status	Read-Only	16/32	64 bytes of RX FIFO data + 64 bytes of LSR status information

TABLE 3: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT

ADDRESS [A7:A0]	REGISTER	READ/WRITE COMMENT	RESET STATE
Ox080	INT0 [7:0]	Read-only Interrupt [1:0], Reserved [7:2]	Bits 7-0 = 0x00
Ox081	INT1 [15:8]	Read-only [5:0], Reserved [7:6]	Bits 7-0 = 0x00
Ox082	INT2 [23:16]	Reserved	Bits 7-0 = 0x00
Ox083	INT3 [31:24]	Reserved	Bits 7-0 = 0x00
Ox084	TIMERCNTL	Read/Write Timer Control	Bits 7-0 = 0x00
Ox085	TIMER	Reserved	Bits 7-0 = 0x00
Ox086	TIMERLSB	Read/Write Timer LSB	Bits 7-0 = 0x00
Ox087	TIMERMSB	Read/Write Timer MSB	Bits 7-0 = 0x00
Ox088	8XMODE	Read/Write	Bits 7-0 = 0x00
Ox089	REGA	Reserved	Bits 7-0 = 0x00

TABLE 3: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT

ADDRESS [A7:A0]	REGISTER	READ/WRITE COMMENT	RESET STATE
Ox08A	RESET	Write-only Self clear bits after executing Reset [1:0]	Bits 7-0 = 0x00
Ox08B	SLEEP	Read/Write Sleep mode [1:0]	Bits 7-0 = 0x00
Ox08C	DREV	Read-only Device revision	Bits 7-0 = 0x02
Ox08D	DVID	Read-only Device identification	Bits 7-0 = 0x22
Ox08E	REGB	Read/Write	Bits 7-0 = 0x00
Ox08F	MPIOINT	Read/Write MPIO interrupt mask	Bits 7-0 = 0x00
Ox090	MPIOLVL	Read/Write MPIO level control	Bits 7-0 = 0x00
Ox091	MPIO3T	Read/Write MPIO output control	Bits 7-0 = 0x00
Ox092	MPIOINV	Read/Write MPIO input polarity select	Bits 7-0 = 0x00
Ox093	MPIOSEL	Read/Write MPIO select	Bits 7-0 = 0xFF

TABLE 4: DEVICE CONFIGURATION REGISTERS SHOWN IN DWORD ALIGNMENT

ADDRESS	REGISTER	BYTE 3 [31:24]	BYTE 2 [23:16]	BYTE 1 [15:8]	BYTE 0 [7:0]
0x080-083	INTERRUPT (read-only)	INT3	INT2	INT1	INT0
0x084-087	TIMER (read/write)	TIMERMSB	TIMERLSB	TIMER (reserved)	TIMERCNTL
0x088-08B	ANCILLARY1 (read/write)	SLEEP	RESET	REGA (reserved)	8XMODE
0x08C-08F	ANCILLARY2 (read-only)	MPIOINT	REGB	DVID	DREV
0x090-093	MPIO (read/write)	MPIOSEL	MPIOINV	MPIO3T	MPIOLVL

1.2.1 The Interrupt Status Register

The XR17C152 has a 32-bit wide register [INT0, INT1, INT2 and INT3] to provide interrupt information and supports two interrupt schemes. The first scheme uses bits 0 to 1 of an 8-bit indicator (INT0) representing channels 0 to 1 of the XR17C152, respectively. This permits the interrupt routine to quickly vector and serve that UART channel and determine the source(s) in each individual routines. INT0 bit-0 represents the interrupt status for UART channel 0 when its transmitter, receiver, line status, or modem port status requires service. INT0 bit-1 provides interrupt status for channel 1 and bits 2 to 7 are reserved and remain at a logic 0.

The second scheme provides detail about the source of the interrupts for each UART channel. All the interrupts are encoded into a 3-bit code per channel. This 3-bit code represents 7 interrupts corresponding to individual UART's transmitter, receiver, line status, modem port status. INT1 register provides the 6-bit interrupt status for both channels. Bits 8, 9 and 10 represents channel 0 and bits 11,12 and 13 represents channel 1. Bits 14 to 31 are reserved and remain at logic zero. Both channels interrupt status are available with a single DWORD read operation. This feature allows the host to quickly vector and serve the interrupts, reducing service interval, hence, reducing host bandwidth requirements. Figure 4 shows the 4-byte interrupt register and its make up.

GLOBAL INTERRUPT REGISTER (DWORD) [default 0x00-00-00-00]

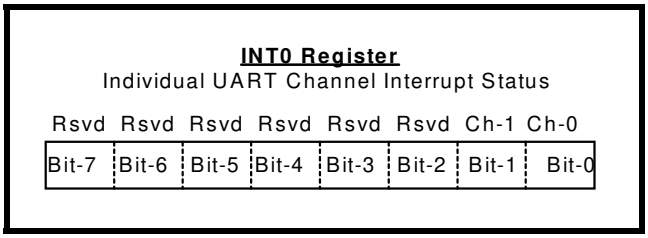
INT3 [31:24]	INT2 [23:16]	INT1 [15:8]	INT0 [7:0]

A special interrupt condition is generated by the 152 when it wakes up from sleep mode. This special interrupt is cleared by reading the INT0 register. If there are not any other interrupts pending, the value read from INT0 would be 0x00.

INT0 [7:0] Channel Interrupt Indicator

Each bit gives an indication of the channel that has requested for service. Bit-0 represents channel 0 and bit-1 indicates channel 1. Logic 1 indicates that a channel has requested for service. Bits 2 to 7 are reserved and remain at logic 0 The interrupt bit clears after reading the appropriate register of the interrupting channel register, see Interrupt Clearing section.

The INT0 register provides status for each channel



Registers INT3, INT2 and INT1 [32:8]

Twenty four bit encoded interrupt indicator. Each channel's interrupt is encoded into 3 bits for receive, transmit, and status. Bit [10:8] represent channel 0 and channel 1 with bits [13:11]. The 3 bit encoding and their priority order are shown below in Table 5 on page 13. The Timer and MPIO interrupts are for the device and therefore they exist within channel 0 (bits [10:8]) only.

FIGURE 4. THE GLOBAL INTERRUPT REGISTER, INT0, INT1, INT2 AND INT3

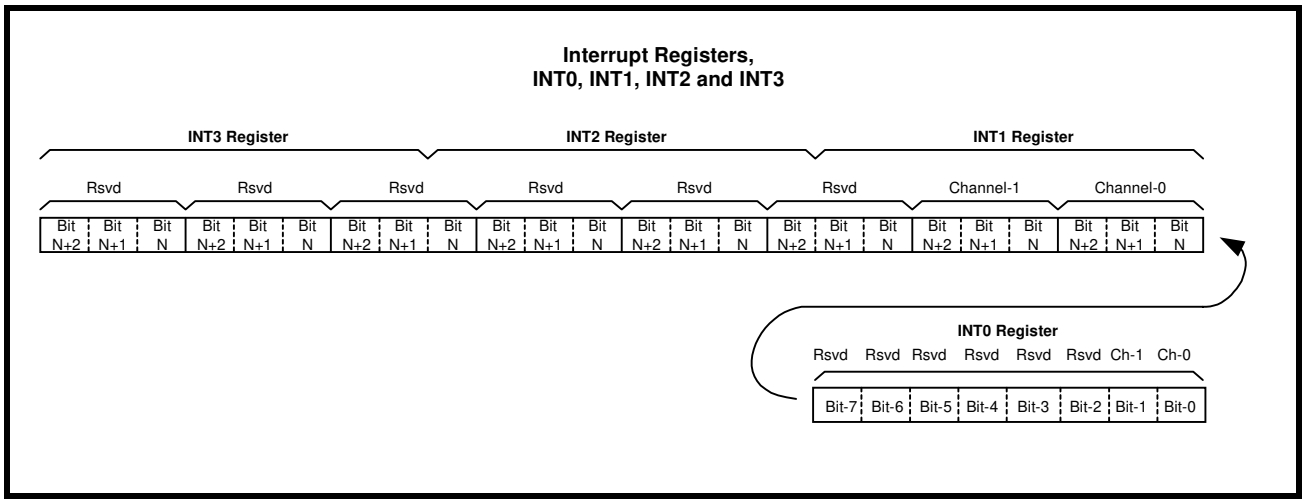


TABLE 5: UART CHANNEL [1:0] INTERRUPT SOURCE ENCODING

PRIORITY	BIT[N+2]	BIT[N+1]	BIT[N]	INTERRUPT SOURCE(S)
x	0	0	0	None
1	0	0	1	RXRDY and RX Line Status (logic OR of LSR[4:1])
2	0	1	0	RXRDY Time-out
3	0	1	1	TXRDY, THR or TSR (auto RS485 mode) empty
4	1	0	0	MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon det. or special char. detected
5	1	0	1	Reserved.
6	1	1	0	MPIO pin(s). Available only in channel 0, reserved in channel 1.
7	1	1	1	TIMER Time-out. Available only in channel 0, reserved channel 1.

TABLE 6: UART CHANNEL [1:0] INTERRUPT CLEARING:

RXRDY is cleared by reading data in the RX FIFO until it falls below the trigger level.
RXRDY Time-out is cleared by reading data until the RX FIFO is empty.
RX Line Status interrupt clears after reading the LSR register.
TXRDY interrupt clears after reading ISR register that is in the UART channel register set.
Modem Status Register interrupt clears after reading MSR register that is in the UART channel register set.
RTS/CTS or DTR/DSR delta interrupt clears after reading MSR register that is in the UART channel register set.
Xoff/Xon interrupt clears after reading the ISR register that is in the UART channel register set.
Special character detect interrupt is cleared by a read to ISR or after the next character is received.
TIMER Time-out interrupt clears after reading the TIMERCNTL register that is in the Device Configuration register set.
MPIO interrupt clears after reading the MPIOLVL register that is in the Device Configuration register set.

1.2.2 General Purpose 16-bit Timer/Counter [TIMERMSB, TIMELSB, TIMER, TIMECNTL] (DEFAULT 0xXX-XX-00-00)

A 16-bit down-count timer for general purpose timer or counter. Its clock source may be selected from internal crystal oscillator or externally on pin TMRCK. The timer can be set to be a single-shot for a one-time event or re-triggerable for a continuous interval. An interrupt may be generated in the INT Register when the timer times out. It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. These registers provide start/stop and re-triggerable or one-shot operation. The time-out output of the Timer can be set to generate an interrupt for system or event alarm.

FIGURE 5. TIMER/COUNTER CIRCUIT.

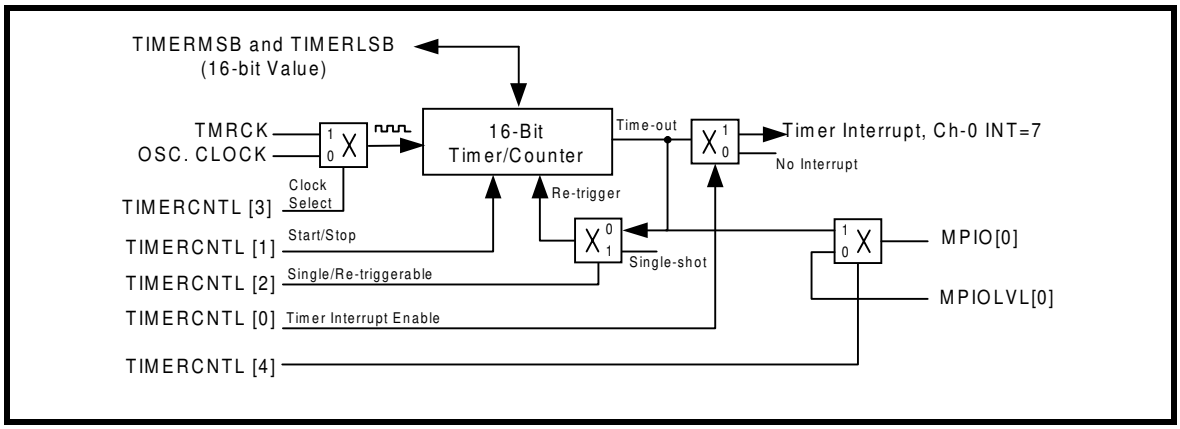


TABLE 7: TIMER CONTROL REGISTERS

TIMERCNTL [0]	Logic 0 (default) disables Timer-Counter interrupt and logic one enables the interrupt, reading the TIMERCNTL clears the interrupt.
TIMERCNLT [1]	Logic 0 (default) stops/pauses the timer and logic one starts/re-starts the timer/counter.
TIMERCNTL [2]	Logic 0 (default) selects re-trigger timer function and logic one selects one-shot (timer function.
TIMERCNTL [3]	Logic 0 (default) selects internal and logic one selects external clock to the timer/counter.
TIMERCNTL [4]	Routes the Timer-Counter interrupt to MPIO[0] if MPIOSEL[0]=0 for external event control.
TIMERCNTL [7:5]	Reserved (defaults to zero).

TIMERCNTL Register

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Rsvd	Rsvd	Rsvd	MPIO[0] Control	Clock Select	Single/ Re-trigger	Start/ Stop	INT Enable

TIMER [15:8] Reserved

TIMERMSB [31:24] and TIMERLSB [23:16]

TIMERMSB and TIMERLSB form a 16-bit value. The least-significant bit of the timer is being bit [0] of the TIMERLSB with most-significant-bit being bit-7 in TIMERMSB. Notice that these registers do not hold the current counter value when read. Reading the TIMERCNTL register will clear its interrupt. Default value is zero (timer disabled) upon powerup and reset.

16-Bit Timer/Counter Programmable Registers

TIMERMSB Register								TIMERLSB Register							
Bit-15	Bit-14	Bit-13	Bit-12	Bit-11	Bit-10	Bit-9	Bit-8	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

1.2.3 8XMODE [7:0] (default 0x00)

Each bit selects 8X or 16X sampling rate for that UART channel, bit-0 is channel 0. Logic 0 (default) selects normal 16X sampling with logic one selects 8X sampling rate. Transmit and receive data rates will double by selecting 8X.

8XMODE Register
Individual UART Channel 8X Clock Mode Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Ch-1	Ch-0

1.2.4 REGA [15:8] Reserved

1.2.5 RESET [23:16] - (default 0x00)

Bits 0 to 1 of the Reset register [RESET] provides the software with the ability to reset the UART(s) when there is a need. Each bit is self-resetting after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition, see Table 19 on page 48 for details. Bit-0 =1 resets UART channel 0 while bit-1=1 resets channel 1.

RESET Register
Individual UART Channel Reset Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Ch-1	Ch-0

1.2.6 SLEEP [31:24] - (default 0x00)

The 8-bit Sleep register enables each UART separately to enter Sleep mode. Sleep mode reduces power consumption when the system needs to put the UART(s) to idle. All of these conditions must be satisfied for the 152 to enter sleep mode:

- no interrupts pending (INT0 = 0x00)
- divisor is a non-zero value for both channels (ie. DLL = 0x1)
- sleep mode is enabled (SLEEP = 0x03)
- modem inputs for both channels are not toggling (MSR bits 0-3 = 0)
- RX input pins for both channels are idling HIGH

The 152 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 152 resumes normal operation by any of the following:

- a receive data start bit transition (logic HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the 152 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 152 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The 152 will stay in the sleep mode of operation until it is disabled by setting Sleep = 0x00. In this case, the dual UART is awaken by any of the UART channel on from a receive data byte or a change on the serial port. The UART is ready after 32 crystal clocks to ensure full functionality. Also, a special interrupt is generated with an indication of no pending interrupt. Reading INT0 will clear this special interrupt. Logic 0 (default) is disable and logic 1 is enable to sleep mode.

SLEEP Register
Individual UART Channel Sleep Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Ch-1	Ch-0

1.2.7 Device Identification and Revision

There are two internal registers that provide device identification and revision, DVID and DREV registers. The 8-bit content in the DVID register provides device identification. A return value of 0x22 from this register indicates the device is an XR17C152 or an XR17D152. The DREV register returns an 8-bit value of 0x01 for revision A with 0x02 equals to revision B and so forth. This information is very useful to the software driver for identifying which device it is communicating with and to keep up with revision changes.

DVID [15:8]

Device identification for the type of UART. The upper nibble indicates it is an XR17Cxxx or XR17Dxxx series device with lower nibble indicating the number of channels.

Examples:

XR17C158 or XR17D158 = 0x28

XR17C154 or XR17D154 = 0x24

XR17C152 or XR17D152 = 0x22

DREV [7:0]

Revision number of the XR17C152. A 0x01 represents "revision-A" with 0x02 for rev-B and so forth.

REGB [23:16] (default 0x00)

REGB register provides a control for simultaneous write to both UARTs configuration register or individually. This is very useful for device initialization in the power up and reset routines. Also, the register provides a facility to interface to the non-volatile memory device such as a 93C46 EEPROM. In embedded applications, the user can use this facility to store proprietary data.

1.2.8 REGB Register

REGB[16] (Read/Write)	Logic 0 (default) write to each UART configuration registers individually.
	Logic 1 enables simultaneous write to both UARTs configuration register.
REGB[19:17]	Reserved.
REGB[20] (Write-Only)	Control the EECK, clock, output (pin 84) on the EEPROM interface.
REGB[21] (Write-Only)	Control the EECS, chips select, output (pin 83) to the EEPROM device.
REGB[22] (Write-Only)	EEDI (pin 82) data input. Write data to the EEPROM device.
REGB[23] (Read-Only)	EEDO (pin 81) data output. Read data from the EEPROM device.

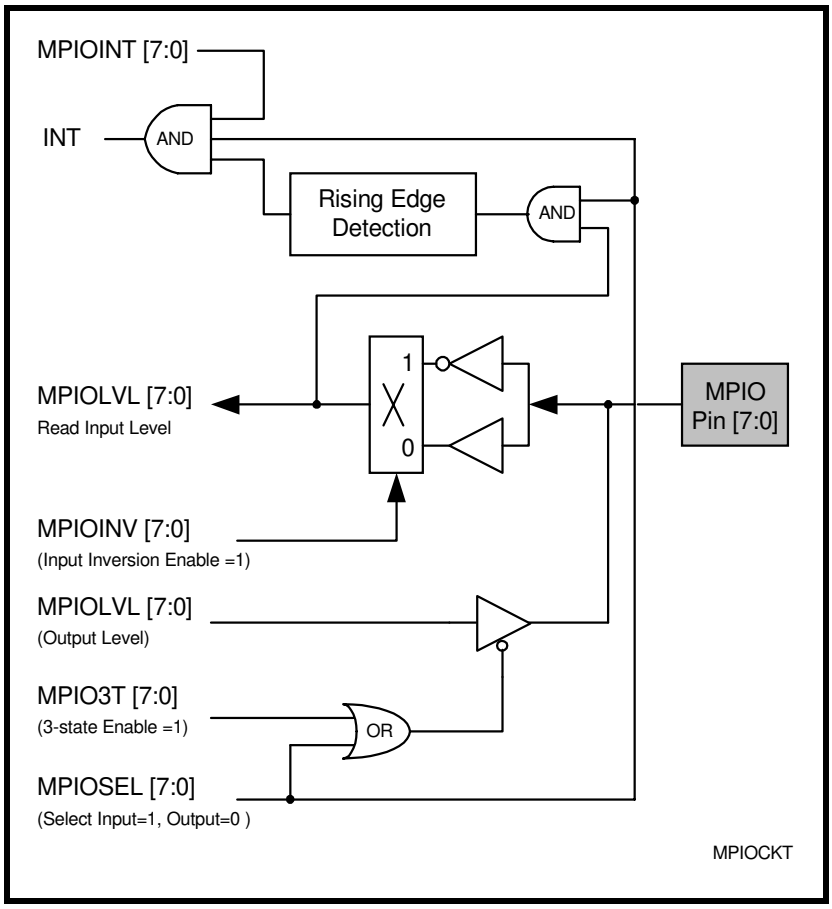
1.2.9 Multi-Purpose Inputs and Outputs

The 152 provides 8 multi-purpose inputs/outputs [MPIO7:0] for general use. Each pin can be programmed to be an input or output function. The input logic state can be set for normal or inverted level, and optionally set to generate an interrupt. The outputs can be set to be normal HIGH or LOW state, or three-state. Their functions and definitions are programmed through 5 registers: MPIOINT, MPIOLVL, MPIO3T, MPIOINV and MPIOSEL. If all 8 pins are set for inputs, all 8 interrupts would be or'ed together. The Or'ed interrupt is reported in the channel 0 UART interrupt status, see Interrupt Status Register. The pins may also be programmed to be outputs and to the three-state condition for signal sharing.

1.2.10 MPIO REGISTER

Bit 7 represents MPIO7 pin and bit 0 represents MPIO0 pin. There are 5 registers that select, control and monitor the 8 multipurpose inputs and output pins. Figure 6 shows the internal circuitry.

FIGURE 6. MULTIPURPOSE INPUT/OUTPUT INTERNAL CIRCUIT



MPIOINT [7:0] (default 0x00)

Enable multipurpose input pin interrupt. If the pin is selected by MPIOSEL as input then bit-0 enables input pin 0 for interrupt, and bit-7 enables input pin 7. No interrupt is enabled if the pin is selected to be an output. The interrupt is edge sensing and determined by MPIOINV and MPIOLVL registers. The MPIO interrupt clears after a read to register MPIOLVL. The combination of MPIOLVL and MPIOINV determines the interrupt being active low or active high, it's level trigger. Logic 0 (default) disables the pin's interrupt and logic 1 enables it.

MPIOINT Register
Multipurpose Input/Output Interrupt Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
MPIO7	MPIO6	MPIO5	MPIO4	MPIO3	MPIO2	MPIO1	MPIO0

MPIOLVL [7:0] (default 0x00)

Output pin level control and input level status. The status of the input pin(s) is read on this register and output pins are controlled on this register. A logic 0 (default) sets the output to low and a logic 1 sets the output pin to high. The MPIO interrupt will clear upon reading this register.

MPIOLVL Register
Multipurpose Output Level Control

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
MPIO7	MPIO6	MPIO5	MPIO4	MPIO3	MPIO2	MPIO1	MPIO0

MPIO3T [7:0] (default 0x00)

Output pin three-state control. A logic 0 (default) sets the output to active level per register MPIOBIT settling, a logic 1 sets the output pin to tri-state.

MPIO3T Register
Multipurpose Output 3-state Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
MPIO7	MPIO6	MPIO5	MPIO4	MPIO3	MPIO2	MPIO1	MPIO0

MPIOINV [7:0] (default 0x00)

Input inversion control. A logic 0 (default) does not invert the input pin logic. A logic 1 inverts the input logic level.

MPIOINV Register
Multipurpose Input Signal Inversion Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
MPIO7	MPIO6	MPIO5	MPIO4	MPIO3	MPIO2	MPIO1	MPIO0

MPIOSEL [7:0] (default 0xFF)

Multipurpose input/output pin select. This register defines the functions of the pins. A logic 1 (default) defines the pin for input and a logic 0 for output.

MPIOSEL Register
Multipurpose Input/Output Selection

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
MPIO7	MPIO6	MPIO5	MPIO4	MPIO3	MPIO2	MPIO1	MPIO0

2.0 CRYSTAL OSCILLATOR / BUFFER

The 152 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in each of the 2 UARTs, the 16-bit general purpose timer/counter and internal logics. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. See Programmable Baud Rate Generator in the UART section for programming details.

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant with 10-22 pF capacitance load, 100ppm) connected externally between the XTAL1 and XTAL2 pins (see Figure 7). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal 2 baud rate generators for standard or custom rates. However, for external clock frequencies greater than 24MHz, a 2K pull-up may be necessary on the XTAL2 output (see Figure 8). Typical oscillator connections are shown in Figure 7. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

FIGURE 7. TYPICAL OSCILLATOR CONNECTIONS

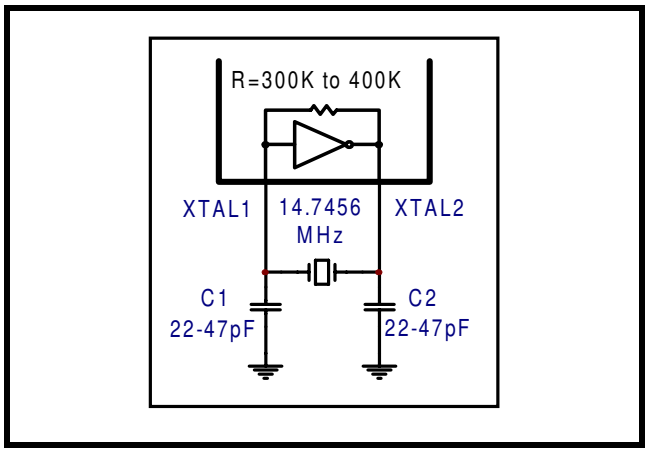
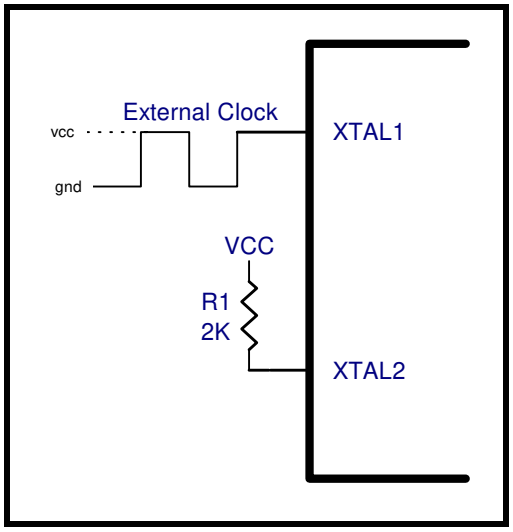


FIGURE 8. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE



3.0 TRANSMIT AND RECEIVE DATA

There are two methods to load transmit data and unload receive data from each UART channel. First, there is a transmit data register and receive data register for each UART channel in the device configuration register set to ease programming. These registers support 8, 16, 24 and 32 bits wide format. In the 32-bit format, it increases the data transfer rate on the PCI bus. Additionally, a special register location provides receive data byte with its associated error tags. This is a 16-bit or 32-bit read operation where the Line Status Register (LSR) content in the UART channel register is paired along with the data byte. This operation further facilitates data unloading with the error tags without having to read the LSR register separately. Furthermore, the XR17C152 supports PCI burst mode for read/write operation of up to 64 bytes of data.

The second method is through each UART channel's transmit holding register (THR) and receive holding register (RHR). The THR and RHR registers are 16550 compatible so their access is limited to 8-bit format. The software driver must separately read the LSR content for the associated error tags before reading the data byte.

3.1 DATA LOADING AND UNLOADING VIA 32-BIT PCI BURST TRANSFERS

The XR17C152 supports PCI Burst Read and PCI Burst Write transactions anywhere in the mapped memory region (except reserved areas). In addition, to utilize this feature fully, the device provides a separate memory location (apart from the 16550 register set) where the RX and the TX FIFO can be read from/written to, as shown in Table 2 on page 10. The following is an extract from the table showing the burstable memory locations:

Channel 0:

RX FIFO	:	0x100 - 0x13F (64 bytes)
TX FIFO	:	0x100 - 0x13F (64 bytes)
RX FIFO + status	:	0x180 - 0x1FF (64 bytes data + 64 bytes status)

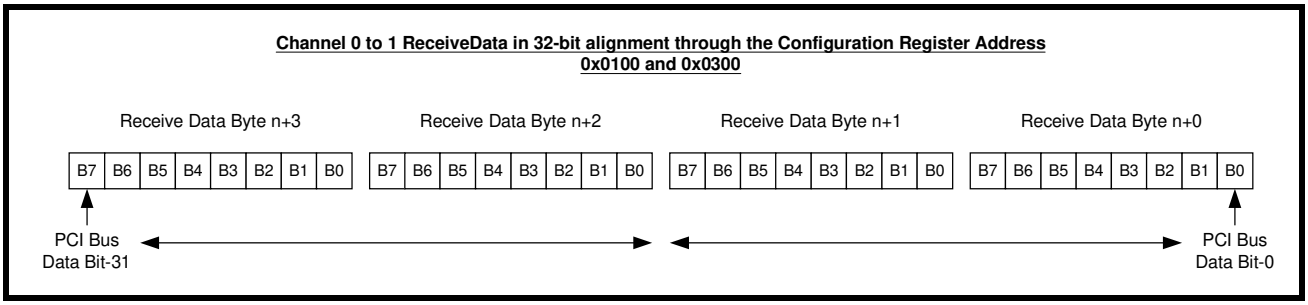
Channel 1:

RX FIFO	:	0x300 - 0x33F (64 bytes)
TX FIFO	:	0x300 - 0x33F (64 bytes)
RX FIFO + status	:	0x380 - 0x3FF (64 bytes data + 64 bytes status)

3.1.1 Normal Rx FIFO Data Unloading at locations 0x100 (channel 0) and 0x300 (channel 1)

The RX FIFO data (up to the maximum 64 bytes) can be read out in a single burst 32-bit read operation (maximum 16 DWORD reads) at memory locations 0x100 (channel 0) and 0x300 (channel 1). This operation is at least 16 times faster than reading the data in 64 separate 8-bit memory reads of RHR register (0x000 for channel 0 and 0x200 for channel 1).

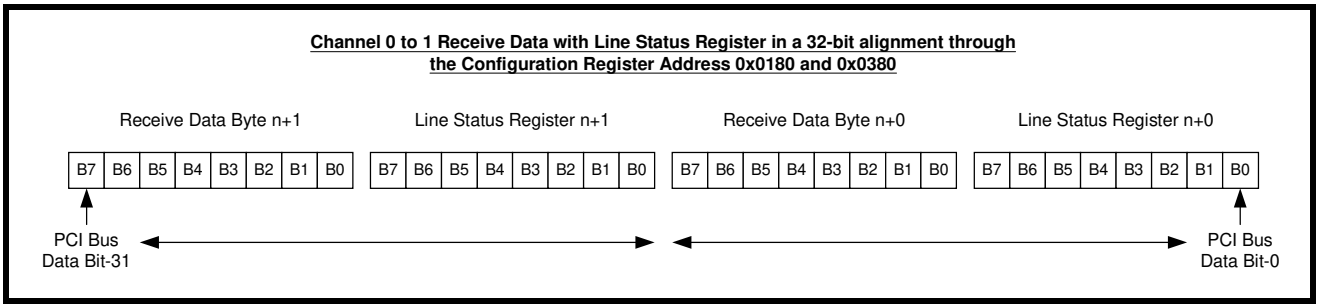
READ RX FIFO, WITH NO ERRORS	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Read n+0 to n+3	FIFO Data n+3	FIFO Data n+2	FIFO Data n+1	FIFO Data n+0
Read n+4 to n+7	FIFO Data n+7	FIFO Data n+6	FIFO Data n+5	FIFO Data n+4
Etc.				



3.1.2 Special Rx FIFO Data Unloading at locations 0x180 (channel 0) and 0x380 (channel 1)

The XR17C152 also provides the same RX FIFO data along with the LSR status information of each byte side-by-side, at locations 0x180 (channel 0) and 0x380 (channel 1). The entire RX data along with the status can be downloaded in a single PCI Burst Read operation of 32 DWORD reads. The Status and Data bytes must be read in 16 or 32 bits format to maintain data integrity. The following tables show this clearly.

READ RX FIFO, WITH LSR ERRORS	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Read n+0 to n+1	FIFO Data n+1	LSR n+1	FIFO Data n+0	LSR n+0
Read n+2 to n+3	FIFO Data n+3	LSR n+3	FIFO Data n+2	LSR n+2
Etc				

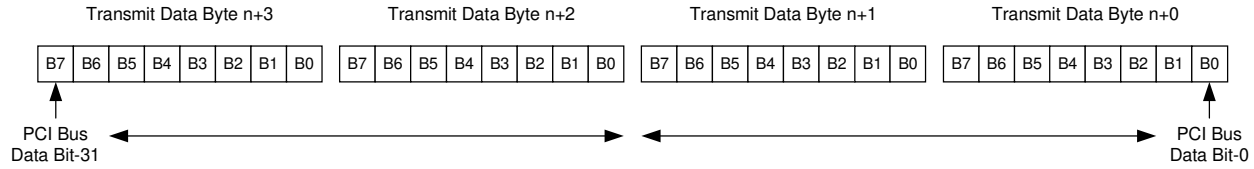


3.1.3 Tx FIFO Data Loading at locations 0x100 (channel 0) and 0x300 (channel 1)

The TX FIFO data (up to the maximum 64 bytes) can be loaded in a single burst 32-bit write operation (maximum 16 DWORD writes) at memory locations 0x100 (channel 0) and 0x300 (channel 1).

WRITE TX FIFO	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Write n+0 to n+3	FIFO Data n+3	FIFO Data n+2	FIFO Data n+1	FIFO Data n+0
Write n+4 to n+7	FIFO Data n+7	FIFO Data n+6	FIFO Data n+5	FIFO Data n+4
Etc.				

Channel 0 to 1 Transmit Data in 32-bit alignment through the Configuration Register Address 0x0100 and 0x0300



3.2 FIFO DATA LOADING AND UNLOADING THROUGH THE UART CHANNEL REGISTERS, THR AND RHR IN 8-BIT FORMAT

The THR and RHR register address for channel 0 to channel 1 is shown in Table 8 below. The THR and RHR for each channel 0 tand 1 are located sequentially at address 0x0000 and 0x0200. Transmit data byte is loaded to the THR when writing to that address and receive data is unloaded from the RHR register when reading that address. Both THR and RHR registers are 16C550 compatible in 8-bit format, so each bus operation can only write or read in bytes.

TABLE 8: TRANSMIT AND RECEIVE DATA REGISTER IN BYTE FORMAT, 16C550 COMPATIBLE

THR and RHR Address Locations For CH0 to CH1 (16C550 Compatible)

CH0	0x000	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH0	0x000	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH1	0x200	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH1	0x200	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

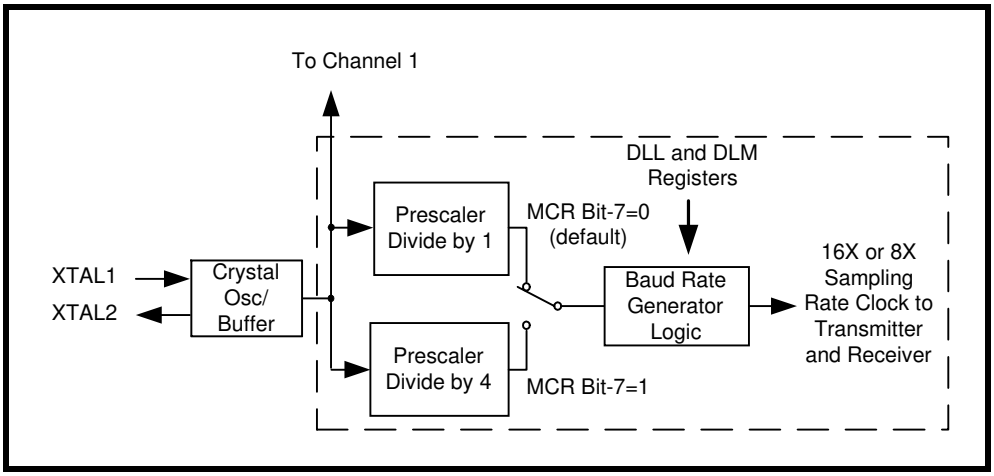
4.0 UART

There are 2 UARTs [channels 1:0] in the 152. Each has its own 64-byte of transmit and receive FIFO, a set of 16550 compatible control and status registers, and a baud rate generator for individual channel data rate setting. Eight additional registers per UART were added for the EXAR enhanced features.

4.1 Programmable Baud Rate Generator

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up. Therefore, the BRG must be programmed during initialization to the operating data rate.

FIGURE 9. BAUD RATE GENERATOR



Programming the Baud Rate Generator Registers DLM and DLL provides the capability for selecting the operating data rate. Table 9 shows the standard data rates available with a 14.7456 MHz crystal or external

clock at 16X clock rate. At 8X sampling rate, these data rates would double. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s).

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), **WITH 8XMODE [1:0] IS 0**

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 8), **WITH 8XMODE [1:0] IS 1**

TABLE 9: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

4.2 Transmitter

The transmitter section comprises of 64 bytes of FIFO, a byte-wide Transmit Holding Register (THR) and an 8-bit Transmit Shift Register (TSR). THR receives a data byte from the host (non-FIFO mode) or a data byte from the FIFO when the FIFO is enabled by FCR bit-0. TSR shifts out every data bit with the 16X or 8X internal clock. A bit time is 16 or 8 clock periods. The transmitter sends the start bit followed by the number of data bits, inserts the proper parity bit if enable, and adds the stop bit(s). The status of the THR and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

4.2.1 Transmit Holding Register (THR) - Write-Only

The Transmit Holding Register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is also the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. A THR empty interrupt can be generated when it is enabled in IER bit-1.

4.2.2 Transmitter Operation in non-FIFO mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.