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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



GENERAL DESCRIPTION

The XR17D154¹ (D154) is a quad PCI Bus Universal Asynchronous Receiver and Transmitter (UART) with same package and pin-out as the Exar XR17C158, XR17D158 and XR17C154. The device is designed to meet today's 32-bit PCI Bus and high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 4 channels to speed up interrupt parsing. Each UART is independently controlled and has its own 16C550 compatible 5G register set, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO trigger levels, transmit and receive FIFO level counters, automatic hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, IrDA (Infrared Data Association) encoder/decoder, 8 multi-purpose inputs/outputs and a 16-bit general purpose timer/counter.

NOTE: 1 Covered by U.S. Patents #5,649,122, #5,949,787

APPLICATIONS

- Universal Form Factor PCI Bus Add-in Card
- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

FEATURES

- High Performance Quad PCI UART
- Universal PCI Bus Buffers - Auto-sense 3.3V or 5V Operation
- 32-bit PCI Bus 2.3 Target Signalling Compliance
- A Global Interrupt Source Register for all 4 UARTs
- Data Transfer in Byte, Word and Double-word
- Data Read/Write Burst Operation
- Each UART is independently controlled with:
 - 16C550 Compatible 5G Register Set
 - 64-byte Transmit and Receive FIFOs
 - Transmit and Receive FIFO Level Counters
 - Automatic RTS/CTS or DTR/DSR Flow Control
 - Automatic Xon/Xoff Software Flow Control
 - Automatic RS485 Half-duplex Control Output with Selectable Turn-around Delay
 - Infrared (IrDA 1.0) Data Encoder/Decoder
 - Programmable Data Rate with Prescaler
 - Up to 6.25 Mbps Serial Data Rate at 8X
- Eight Multi-Purpose Inputs/outputs
- General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up
- EEPROM Interface for PCI Configuration
- Same package and pin-out as the XR17D158, XR17C158 and XR17C154 (20x20x1.4mm 144-LQFP)

FIGURE 1. BLOCK DIAGRAM

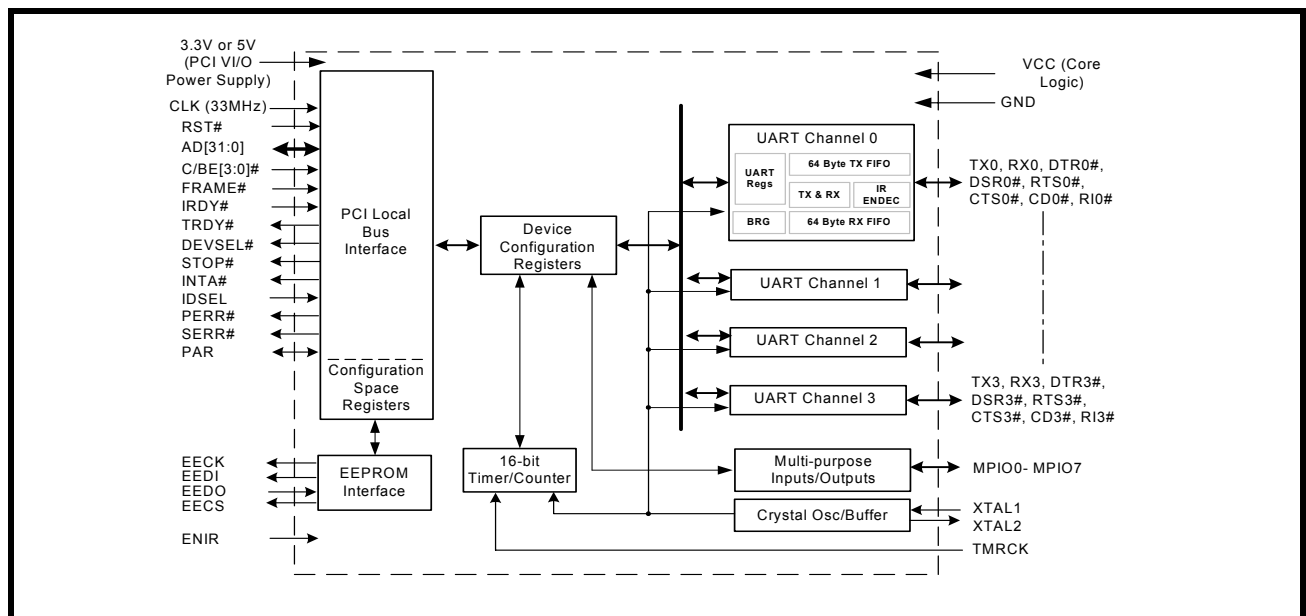
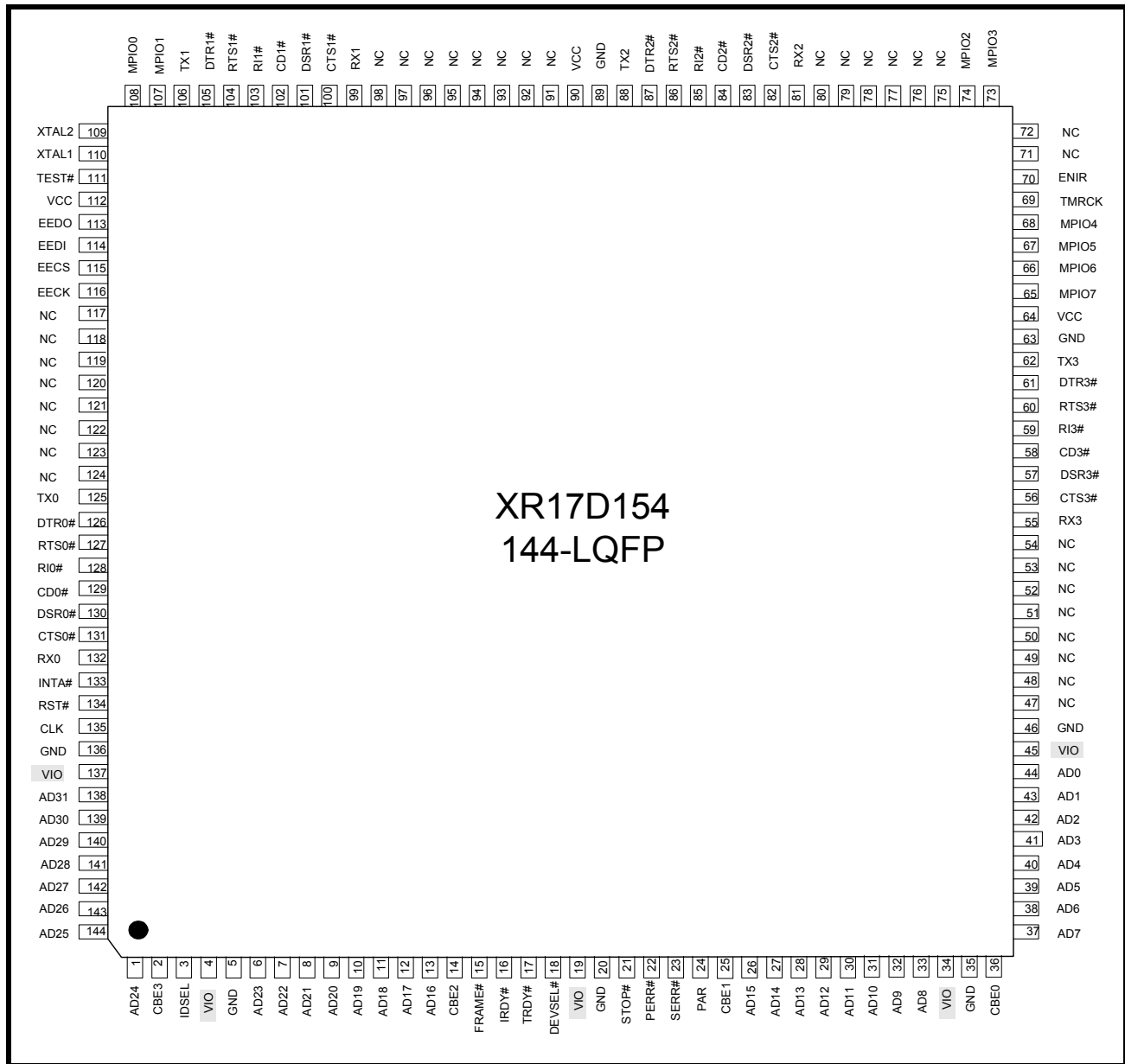


FIGURE 2. PIN OUT OF THE DEVICE



ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE | DEVICE STATUS |
|-------------|---------------|-----------------------------|---------------|
| XR17D154CV | 144-Lead LQFP | 0°C to +70°C | Active |
| XR17D154IV | 144-Lead LQFP | -40°C to +85°C | Active |

PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|---|--|------|--|
| PCI LOCAL BUS INTERFACE | | | |
| RST# | 134 | I | PCI Bus reset input (active low). It resets the PCI local bus configuration space registers, device configuration registers and UART channel registers to the default condition. |
| CLK | 135 | I | PCI Bus clock input of up to 33.34MHz. |
| AD31-AD25, AD24, AD23-AD16, AD15-AD8, AD7-AD0 | 138-144, 1, 6-13 26-33 37-44 | IO | Address data lines [31:0] (bidirectional). |
| FRAME# | 15 | I | Bus transaction cycle frame (active low). It indicates the beginning and duration of an access. |
| C/BE3#- C/BE0# | 2,14,25,36 | I | Bus Command/Byte Enable [3:0] (active low). This line is multiplexed for bus Command during the address phase and Byte Enable during the data phase. |
| IRDY# | 16 | I | Initiator Ready (active low). During a write, it indicates valid data is present on data bus. During a read, it indicates the master is ready to accept data. |
| TRDY# | 17 | O | Target Ready (active low). |
| STOP# | 21 | O | Target request to stop current transaction (active low). 5 |
| IDSEL | 3 | I | Initialization device select (active high). |
| DEVSEL# | 18 | O | Device select to the XR17D154 (active low). |
| INTA# | 133 | OD | Device interrupt from XR17D154 (open drain, active low). |
| PAR | 24 | IO | Parity is even across AD[31:0] and C/BE[3:0]# (bidirectional, active high). |
| PERR# | 22 | O | Parity error indicator to host (active low). Optional in bus target application. |
| SERR# | 23 | OD | System error indicator to host (open drain, active low). Optional in bus target application. |
| MODEM OR SERIAL I/O INTERFACE | | | |
| TX0 | 125 | O | UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX0 | 132 | I | UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS0# | 127 | O | UART channel 0 Request to Send or general purpose output (active low). |
| CTS0# | 131 | I | UART channel 0 Clear to Send or general purpose input (active low). |
| DTR0# | 126 | O | UART channel 0 Data Terminal Ready or general purpose output (active low). |
| DSR0# | 130 | I | UART channel 0 Data Set Ready or general purpose input (active low). |
| CD0# | 129 | I | UART channel 0 Carrier Detect or general purpose input (active low). |
| RI0# | 128 | I | UART channel 0 Ring Indicator or general purpose input (active low). |

PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|--------------------------|-------|------|--|
| TX1 | 106 | O | UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX1 | 99 | I | UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS1# | 104 | O | UART channel 1 Request to Send or general purpose output (active low). |
| CTS1# | 100 | I | UART channel 1 Clear to Send or general purpose input (active low). |
| DTR1# | 105 | O | UART channel 1 Data Terminal Ready or general purpose output (active low). |
| DSR1# | 101 | I | UART channel 1 Data Set Ready or general purpose input (active low). |
| CD1# | 102 | I | UART channel 1 Carrier Detect or general purpose input (active low). |
| RI1# | 103 | I | UART channel 1 Ring Indicator or general purpose input (active low). |
| TX2 | 88 | O | UART channel 2 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX2 | 81 | I | UART channel 2 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS2# | 86 | O | UART channel 2 Request to Send or general purpose output (active low). |
| CTS2# | 82 | I | UART channel 2 Clear to Send or general purpose input (active low). |
| DTR2# | 87 | O | UART channel 2 Data Terminal Ready or general purpose output (active low). |
| DSR2# | 83 | I | UART channel 2 Data Set Ready or general purpose input (active low). |
| CD2# | 84 | I | UART channel 2 Carrier Detect or general purpose input (active low). |
| RI2# | 85 | I | UART channel 2 Ring Indicator or general purpose input (active low). |
| TX3 | 62 | O | UART channel 3 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW. |
| RX3 | 55 | I | UART channel 3 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4]. |
| RTS3# | 60 | O | UART channel 3 Request to Send or general purpose output (active low). |
| CTS3# | 56 | I | UART channel 3 Clear to Send or general purpose input (active low).d. |
| DTR3# | 61 | O | UART channel 3 Data Terminal Ready or general purpose output (active low). |
| DSR3# | 57 | I | UART channel 3 Data Set Ready or general purpose input (active low). |
| CD3# | 58 | I | UART channel 3 Carrier Detect or general purpose input (active low). |
| RI3# | 59 | I | UART channel 3 Ring Indicator or general purpose input (active low). |
| ANCILLARY SIGNALS | | | |
| MPIO0 | 108 | I/O | Multi-purpose input/output 0. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT |

PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|-------|-------------|------|--|
| MPIO1 | 107 | I/O | Multi-purpose input/output 1. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT. |
| MPIO2 | 74 | I/O | Multi-purpose input/output 2. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT. |
| MPIO3 | 73 | I/O | Multi-purpose input/output 3. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT. |
| MPIO4 | 68 | I/O | Multi-purpose input/output 4. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT. |
| MPIO5 | 67 | I/O | Multi-purpose input/output 5. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT. |
| MPIO6 | 66 | I/O | Multi-purpose input/output 6. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT. |
| MPIO7 | 65 | I/O | Multi-purpose input/output 7. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOVLV, MPIOINV, MPIO3T and MPIOINT. |
| EECK | 116 | O | Serial clock to EEPROM. An internal clock of CLK divide by 256 is used for reading the vendor and sub-vendor ID and model number during power up or reset. However, it can be manually clocked thru the Configuration Register REGB. |
| EECS | 115 | O | Chip select to a EEPROM device like 93C46. It is manually selectable thru the Configuration Register REGB. Requires a pull-up 4.7KΩ resistor for external sensing of EEPROM during power up. See DAN112 for further details. |
| EEDI | 114 | O | Write data to EEPROM device. It is manually accessible thru the Configuration Register REGB. The D154 auto-configuration register interface logic uses the 16-bit format. |
| EEDO | 113 | I | Read data from EEPROM device. It is manually accessible thru the Configuration Register REGB. |
| XTAL1 | 110 | I | Crystal of up to 24MHz or external clock input of up to 50MHz for data rates up to 6.25Mbps at 5V and 8X sampling. See AC Characterization table. Caution: this input is not 5V tolerant at 3.3V. |
| XTAL2 | 109 | O | Crystal or buffered clock output. |
| TMRCK | 69 | I | 16-bit timer/counter external clock input. |
| ENIR | 70 | I | Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up all 4 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART. Software can override this pin thereafter and enable or disable it. |
| TEST# | 111 | I | Factory Test. Connect to VCC for normal operation. |
| VCC | 64, 90, 112 | PWR | 5V or 3.3V power supply for the core logic. This power supply determines the VOH level of the non-PCI bus interface outputs. Note that VCC ≥ VIO for normal device operation and see Table 1 for valid combinations of VCC and VIO. SEE "APPLICATION EXAMPLES" ON PAGE 8. However, VCC must equal VIO if sleep mode is used. See Sleep Mode section on page 19 . |

PIN DESCRIPTIONS

| NAME | PIN # | TYPE | DESCRIPTION |
|------|--------------------------------------|------|--|
| VIO | 4, 19, 34, 45, 137 | PWR | PCI bus I/O power supply - 3.3V or 5V, detected by the auto-sense circuitry of the XR17D154. This power supply determines the VOH level of the PCI bus interface outputs. (PCI 2.3 signalling compliant at both 3.3V and 5V operation, suitable for universal form factor add-in card application.) |
| GND | 5,20,35,46,63, 89,136 | PWR | Power supply common, ground. |
| NC | 47-54, 71, 72, 75-80, 91-98, 117-124 | | No Connection. These pins are reserved and used by the octal PCI UARTs XR17C158 and XR17D158. |

NOTE: Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

FUNCTIONAL DESCRIPTION

The XR17D154 (D154) integrates the functions of 4 enhanced 16550 UARTs with the PCI Local Bus interface and a non-volatile memory interface for PCI bus's plug-and-play auto-configuration, a 16-bit timer/counter, 8 multi-purpose inputs/outputs, and an on-chip oscillator. The PCI local bus is a synchronous timing bus where all bus transactions are associated to the bus clock of up to 33 MHz. The D154 supports 32-bit wide read and write data transfer operations including data burst mode through the PCI Local Bus interface. Read and write data operations maybe in byte, word or double-word (DWORD) format. The data transfer rate in a DWORD operation is 4 times faster than the single byte operation with 8-bit ISA bus. A single 32-bit interrupt status register provides interrupts status for all 4 UARTs, timer/counter, multipurpose inputs/outputs, and a special sleep wake up indicator. There are three sets of register in the device. First, the PCI local bus configuration registers for PCI auto configuration. A set of device configuration registers for overall control, 32-bit wide transmit and receive data transfer, and monitoring of the 4 UART channels. Lastly, each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status, and byte wide data transfer.

Each UART has the improved fifth generation (5G) register set, 64-byte FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger level, FIFO level counters, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of 1X or 4X, and data rate up to 6.25 Mbps. The XR17D154 bus timing and drive capability meets the PCI local bus specification revision 2.3 for 3.3V and 5V at 33.34 MHz over the temperature range. The XR17D154 is available in the same thin 144-pin LQFP (20x20x1.4mm) package and pin-out as the XR17C154, XR17D158 and XR17C158 in commercial and industrial temperature ranges.

PCI LOCAL BUS INTERFACE

This is the host interface and it meets the PCI Local Bus Specification revision 2.3. The PCI local bus operations are synchronous meaning each transaction is associated to the bus clock. The XR17D154 can operate with the bus clock of up to a 33.34 MHz. Data transfers operation can be formatted in 8-bit, 16-bit, 24-bit or 32-bit wide. With 32-bit data operations, it pushes the data transfer rate on the bus up to 132 MByte/sec. This increases the overall system's communication performance up to 16 times better than the 8-bit ISA bus. See PCI local bus specification revision 2.3 for bus operation details.

PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

A set of PCI local bus configuration space register is provided. These registers provide the PCI local bus operating system with the card's vendor ID, device ID, sub-vendor ID, product model number, and resources and capabilities. The PCI local bus operating system collects this data from all the cards on the bus during the auto configuration phase that follows immediately after a power up or system reset/reboot. After it has sorted out all devices on the bus, it defines and download the operating conditions to the cards. One of the definitions is the base address loaded into the Base Address Register (BAR) where the card will be operating in the PCI local bus memory space.

EEPROM INTERFACE

An external 93C46 EEPROM is only used to store the vendor's ID and model number, and the sub-vendor's ID and product model number. This information is only used with the plug-and-play auto configuration of the PCI local bus. These data provide automatic hardware installation onto the PCI bus. The EEPROM interface consists of 4 signals, EEDI, EEDO, EECS, and EECK. The EEPROM is not needed when auto configuration is not required in the application. However, If your design requires non-volatile memory for other purpose. It is possible to store and retrieve data on the EEPROM through a special PCI device configuration register. See application note [DAN112](#) for its programming details.

1.0 APPLICATION EXAMPLES

The XR17D154 is designed to operate with VCC (voltage to the UART Core Logic) greater than or equal to VIO. See Table 1 below for valid combinations of VCC and VIO that can be used with the device..

TABLE 1: VALID COMBINATIONS OF VCC AND VIO SUPPLY VOLTAGES

| VCC | VIO | |
|------|------|----------------|
| 5.0V | 5.0V | Valid |
| 5.0V | 3.3V | Valid |
| 3.3V | 5.0V | Invalid |
| 3.3V | 3.3V | Valid |

For a universal add-in card, it is usually unknown whether it will be plugged into a 3.3V or 5V PCI slot, therefore VCC must be 5V to guarantee proper functionality in any PCI slot as shown in **Figure 3**. In an embedded system, the designer can choose to use a 3.3V or 5V power supply for the UART core voltage. Of course, the core voltage can be 3.3V only when the VIO is 3.3V. In **Figure 4**, examples 1-3 show valid applications of the XR17D154 in an embedded system.

FIGURE 3. TYPICAL APPLICATION FOR A UNIVERSAL ADD-IN CARD

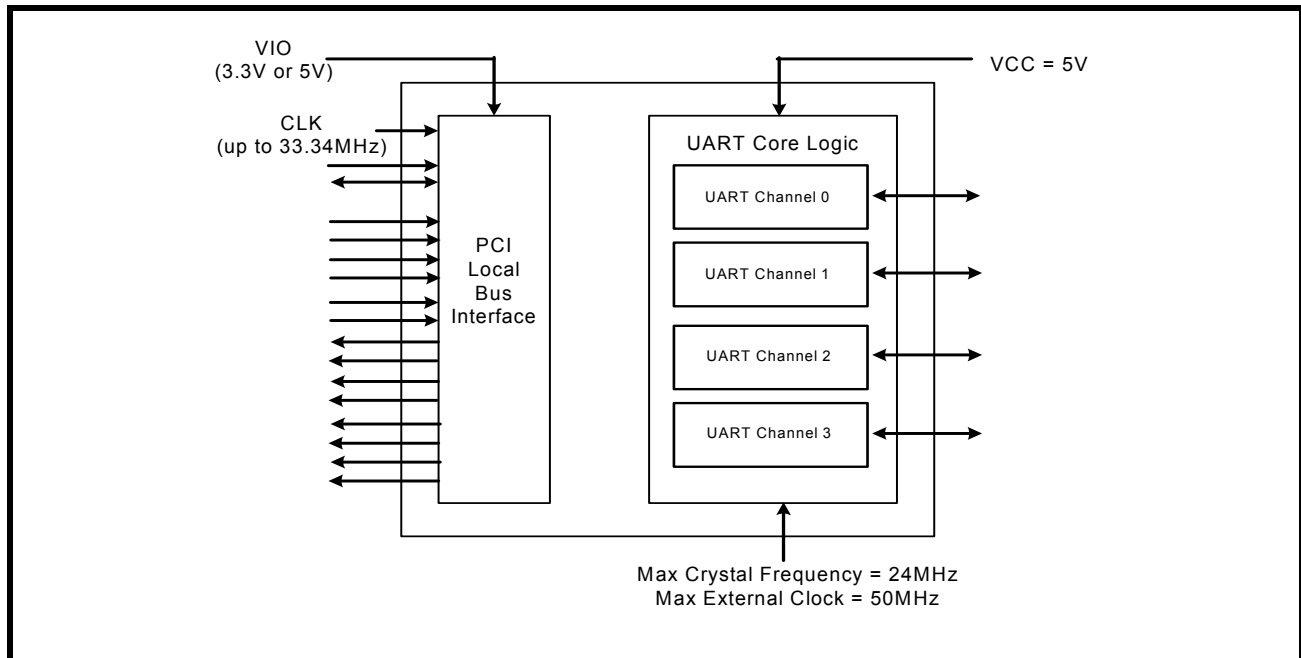
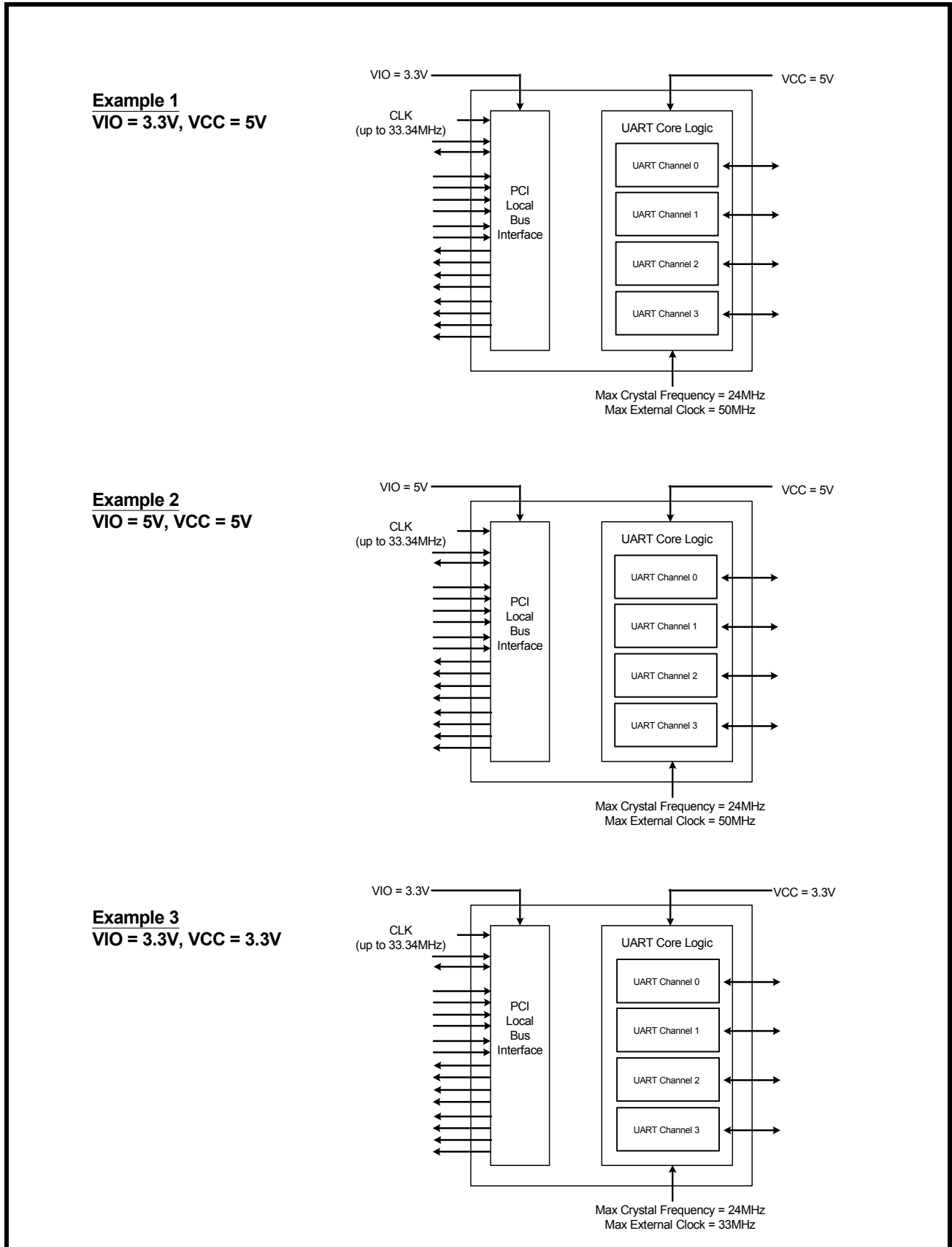


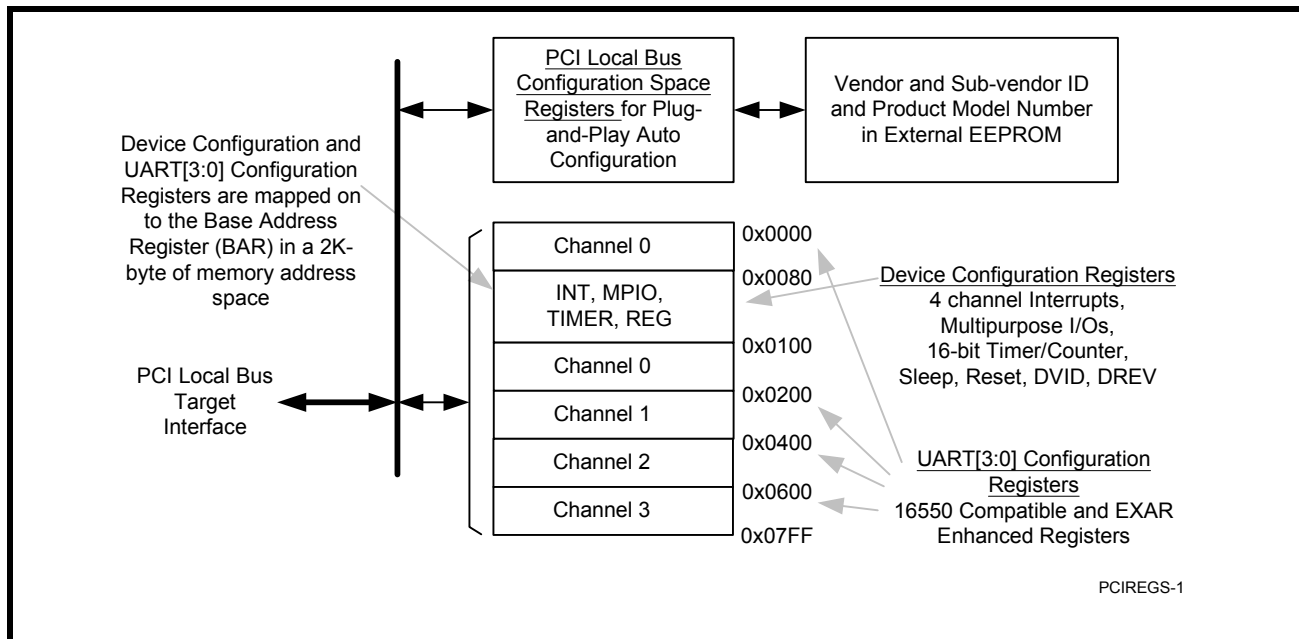
FIGURE 4. TYPICAL APPLICATIONS IN AN EMBEDDED SYSTEM



2.0 XR17D154 REGISTERS

The XR17D154 UART has three different sets of registers as shown in **Figure 5**. The PCI local bus configuration space registers are for plug-and-play auto-configuration when connecting the device to the PCI bus. This auto-configuration feature makes installation very easy into a PCI system and it is part of the PCI local bus specification. The second register set is the device configuration registers that are accessible directly from the PCI bus for programming general operating conditions of the device and monitoring the status of various functions. These registers are mapped into 2K of the PCI bus memory address space. These functions include all 4 channel UART's interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode, soft-reset, and device identification and revision. And lastly, each UART channel has its own set of 5G internal UART configuration registers for its own operation control and status reporting. All 4 sets of channel registers are embedded inside the device configuration registers space, which provides faster access. The following paragraphs describe all 3 sets of registers in detail.

FIGURE 5. THE XR17D154 REGISTER SETS



2.1 PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

The PCI local bus configuration space registers are responsible for setting up the device's operating environment in the PCI local bus. The pre-defined operating parameters of the device are read by the PCI bus plug-and-play auto-configuration manager in the operating system. After the PCI bus has collected all data from every device/card on the bus, it defines and downloads the memory mapping information to each device/card about their individual operation memory address location and conditions. The operating memory mapped address location is downloaded into the Base Address Register (BAR) register, 0x10. The plug-and-play auto configuration feature is only available when an external 93C46 EEPROM is used. The EEPROM contains the device vendor and sub-vendor data required by the auto-configuration setup.

TABLE 2: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

| ADDRESS | BITS | TYPE | DESCRIPTION | RESET VALUE (HEX) |
|---------|----------------|------------------|--|--------------------|
| 0x00 | 31:16 | RWR ¹ | Device ID (Exar device ID number or from EEPROM) | 0x0154 |
| | 15:0 | RWR ¹ | Vendor ID (Exar ID or from EEPROM) specified by PCISIG | 0x13A8 |
| 0x04 | 31:28 | RO | Status bits (error reporting bits) | 0000 |
| | 27 | R-Reset | Target Abort. Set whenever D154 terminates with a target abort. | 0 |
| | 26:25 | RO | DEVSEL# timing. | 00 |
| | 24 | RO | Unimplemented bus master error reporting bit | 0 |
| | 23 | RO | Fast back to back transactions are supported | 1 |
| | 22:16 | RO | Reserved Status bits | 000 0000 |
| | 15:9,7,5,4,3,2 | RO | Command bits (reserved) | 0x0000 |
| | 8 | WO | SERR# driver enable. Logic 1=enable driver and 0=disable driver | 0 |
| | 6 | WO | Parity error enable. Logic 1=respond to parity error and 0=ignore | 0 |
| | 1 | RWR | Command controls a device's response to mem space accesses: 0=disable mem space accesses, 1=enable mem space accesses | 0 |
| | 0 | RO | Command controls a device's response to I/O space accesses: 0 = disable I/O space accesses 1 = enable I/O space accesses | 0 |
| 0x08 | 31:8 | RO | Class Code (Simple 550 Communication Controller). | 0x070002 |
| | 7:0 | RO | Revision ID (Exar device revision number) | Current Rev. value |
| 0x0C | 31:24 | RO | BIST (Built-in Self Test) | 0x00 |
| | 23:16 | RO | Header Type (a single function device with one BAR) | 0x00 |
| | 15:8 | RO | Unimplemented Latency Timer (needed only for bus master) | 0x00 |
| | 7:0 | RO | Unimplemented Cache Line Size | 0x00 |
| 0x10 | 31:11 | RW | Memory Base Address Register (BAR) | 0x00 |
| | 10:0 | RO | Claims a 2K address space for the memory mapped UARTs | 0xX000 |
| 0x14 | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x18h | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x1C | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x20 | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x24 | 31:0 | RO | Unimplemented Base Address Register (returns zeros) | 0x00000000 |
| 0x28 | 31:0 | RO | Reserved | 0x00000000 |
| 0x2C | 31:16 | RWR ¹ | Subsystem ID (write from external EEPROM by customer) | 0x0000 |

TABLE 2: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

| ADDRESS | BITS | TYPE | DESCRIPTION | RESET VALUE (HEX) |
|---------|-------|------------------|--|-------------------|
| | 15:0 | RWR ¹ | Subsystem Vendor ID (write from external EEPROM by customer) | 0x0000 |
| 0x30 | 31:0 | RO | Expansion ROM Base Address (Unimplemented) | 0x00000000 |
| 0x34 | 31:0 | RO | Reserved (returns zeros) | 0x00000000 |
| 0x38 | 31:0 | RO | Reserved (returns zeros) | 0x00000000 |
| 0x3C | 31:24 | RO | Unimplemented MAXLAT | 0x00 |
| | 23:16 | RO | Unimplemented MINGNT | 0x00 |
| | 15:8 | RO | Interrupt Pin, use INTA#. | 0x01 |
| | 7:0 | RWR | Interrupt Line. | 0xXX |

NOTE: RWR¹=Read/Write from external EEPROM. RWR=Read/Write from AD[31:0]. RO= Read Only. WO=Write Only.

2.2 Device configuration Register Set

The device configuration registers and a special way to access each of the UART's transmit and receive data FIFOs are accessible directly from the PCI data bus. This provides easy programming of general operating parameters to the D154 UART and for monitoring the status of various functions. The registers occupy 2K of PCI bus memory address space. These addresses are offset onto the basic memory address, a value loaded into the Memory Base Address Register (BAR) in the PCI local bus configuration register set. These registers control or report on all 4 channel UARTs functions that include interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode control, soft-reset control, and device identification and revision, and others.

The registers set is mapped into 4 address blocks where each UART channel occupies 512 bytes memory space for its own 16550 compatible configuration registers. The device configuration and control registers are embedded inside the UART channel zero's address space between 0x0080 to 0x0093. All these registers can be accessed in 8, 16, 24 or 32 bit width depending on the starting address given by the host at beginning of the bus cycle. Transmit and receive data may be loaded or unloaded in 8, 16, 24 or 32 bit format to the register's address. Every time a read or write operation is made to the transmit or receive register, its FIFO data pointer is automatically bumped to the next sequential data location either in byte, word or dword. One special case applies to the receive data unloading when reading the receive data together with its LSR register content. The host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

TABLE 3: XR17D154 DEVICE CONFIGURATION REGISTERS

| OFFSET ADDRESS | MEMORY SPACE | READ/WRITE | DATA WIDTH | COMMENT |
|----------------|--------------------------------|-----------------------|------------|-----------------------------------|
| 0x000 - 0x00F | UART channel 0 Regs | (Table 12 & Table 13) | 8/16/24/32 | First 8 regs are 16550 compatible |
| 0x010 - 0x07F | Reserved | | | |
| 0x080 - 0x093 | DEVICE CONFIG. REGISTERS | (Table 4) | 8/16/24/32 | |
| 0x094 - 0x0FF | Reserved | Read/Write | | |
| 0x100 - 0x13F | UART 0 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x100 - 0x13F | UART 0 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x140 - 0x17F | Reserved | | | |
| 0x180 - 0x1FF | UART 0 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |
| | | | | |
| 0x200 - 0x20F | UART channel 1 Regs | (Table 12 & Table 13) | 8/16/24/32 | First 8 regs are 16550 compatible |
| 0x210 - 0x2FF | Reserved | Read/Write | | |
| 0x300 - 0x33F | UART 1 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x300 - 0x33F | UART 1 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x340 - 0x37F | Reserved | | | |
| 0x380 - 0x3FF | UART 1 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |
| | | | | |
| 0x400 - 0x40F | UART channel 2 Regs | (Table 12 & Table 13) | 8/16/24/32 | First 8 regs are 16550 compatible |
| 0x410 - 0x4FF | Reserved | Read/Write | | |
| 0x500 - 0x53F | UART 2 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x500 - 0x53F | UART 2 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x540 - 0x57F | Reserved | | | |
| 0x580 - 0x5FF | UART 2 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |
| | | | | |
| 0x600 - 0x60F | UART channel 3 Regs | (Table 12 & Table 13) | 8/16/24/32 | First 8 regs are 16550 compatible |
| 0x610 - 0x6FF | Reserved | Read/Write | | |
| 0x700 - 0x73F | UART 3 – Read FIFO | Read-Only | 8/16/24/32 | 64 bytes of RX FIFO data |
| 0x700 - 0x73F | UART 3 – Write FIFO | Write-Only | 8/16/24/32 | 64 bytes of TX FIFO data |
| 0x740 - 0x77F | Reserved | | | |
| 0x780 - 0x7FF | UART 3 – Read FIFO with errors | Read-Only | 16/32 | 64 bytes of RX FIFO data + LSR |

TABLE 4: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT

| ADDRESS [A7:A0] | REGISTER | READ/WRITE COMMENT | RESET STATE |
|-----------------|--------------|--|-----------------|
| 0x080 | INT0 [7:0] | Read-only Interrupt [3:0], Reserved [7:4] | Bits 7-0 = 0x00 |
| 0x081 | INT1 [15:8] | Read-only | Bits 7-0 = 0x00 |
| 0x082 | INT2 [23:16] | Read-only [3:0], Reserved [7:4] | Bits 7-0 = 0x00 |
| 0x083 | INT3 [31:24] | Reserved | Bits 7-0 = 0x00 |
| 0x084 | TIMERCNTL | Read/Write Timer Control | Bits 7-0 = 0x00 |
| 0x085 | TIMER | Reserved | Bits 7-0 = 0x00 |
| 0x086 | TIMERLSB | Read/Write Timer LSB | Bits 7-0 = 0x00 |
| 0x087 | TIMERMSB | Read/Write Timer MSB | Bits 7-0 = 0x00 |
| 0x088 | 8XMODE | Read/Write | Bits 7-0 = 0x00 |
| 0x089 | REGA | Reserved | Bits 7-0 = 0x00 |
| 0x08A | RESET | Write-only Self clear bits after executing Reset [3:0] | Bits 7-0 = 0x00 |
| 0x08B | SLEEP | Read/Write Sleep mode [3:0] | Bits 7-0 = 0x00 |
| 0x08C | DREV | Read-only Device revision | Bits 7-0 = 0x04 |
| 0x08D | DVID | Read-only Device identification | Bits 7-0 = 0x24 |
| 0x08E | REGB | Read/Write | Bits 7-0 = 0x00 |
| 0x08F | MPIOINT | Read/Write MPIO interrupt mask | Bits 7-0 = 0x00 |
| 0x090 | MPIOLVL | Read/Write MPIO level control | Bits 7-0 = 0x00 |
| 0x091 | MPIO3T | Read/Write MPIO output control | Bits 7-0 = 0x00 |
| 0x092 | MPIOINV | Read/Write MPIO input polarity select | Bits 7-0 = 0x00 |
| 0x093 | MPIOSEL | Read/Write MPIO select | Bits 7-0 = 0xFF |

TABLE 5: DEVICE CONFIGURATION REGISTERS SHOWN IN DWORD ALIGNMENT

| ADDRESS | REGISTER | BYTE 3 [31:24] | BYTE 2 [23:16] | BYTE 1 [15:8] | BYTE 0 [7:0] |
|-----------|-------------------------|----------------|----------------|------------------|--------------|
| 0x080-083 | INTERRUPT (read-only) | INT3 | INT2 | INT1 | INT0 |
| 0x084-087 | TIMER (read/write) | TIMERMSB | TIMERLSB | TIMER (reserved) | TIMERCNTL |
| 0x088-08B | ANCILLARY1 (read/write) | SLEEP | RESET | REGA (reserved) | 8XMODE |
| 0x08C-08F | ANCILLARY2 (read-only) | MPIOINT | REGB | DVID | DREV |
| 0x090-093 | MPIO (read/write) | MPIOSEL | MPIOINV | MPIO3T | MPIOLVL |

2.2.1 The Interrupt Status Register

The XR17D154 has a 32-bit wide register [INT0, INT1, INT2 and INT3] to provide interrupt information and supports two interrupt schemes. The first scheme uses bits 0 to 3 of an 8-bit indicator (INT0) representing channels 0 to 3 of the XR17D154, respectively. This permits the interrupt routine to quickly vector and serve that UART channel and determine the source(s) in each individual routines. INT0 bit-0 represents the interrupt status for UART channel 0 when its transmitter, receiver, line status, or modem port status requires service. Other bits in the INT0 register provide indication for the other channels with bit-3 representing UART channel 4 respectively, bits 4 to 7 are reserved and remain at logic zero.

The second scheme provides detail about the source of the interrupts for each UART channel. All the interrupts are encoded into a 3-bit code. This 3-bit code represents 7 interrupts corresponding to individual UART's transmitter, receiver, line status, modem port status. INT1 and INT2 registers provide the 12-bit interrupt status for all 4 channels. Bits 8, 9 and 10 representing channel 0 and bits 17,18 and 19 representing channel 3 respectively. Bits 20 to 31 are reserved and remain at logic zero. All 4 channel interrupts status are available with a single DWORD read operation. This feature allows the host quickly vectors and serves the interrupts, reducing service interval, hence, reduce host bandwidth requirement. **Figure 6** shows the 4-byte interrupt register and its make up.

GLOBAL INTERRUPT REGISTER (DWORD) - [default 0x00-00-00-00]

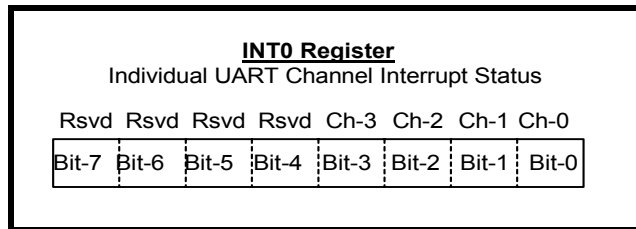
| | | | |
|--------------|--------------|-------------|------------|
| INT3 [31:24] | INT2 [23:16] | INT1 [15:8] | INT0 [7:0] |
|--------------|--------------|-------------|------------|

A special interrupt condition is generated by the 154 when it wakes up from sleep mode. This special interrupt is cleared by reading the INT0 register. If there are not any other interrupts pending, the value read from INT0 would be 0x00.

INT0 [7:0] Channel Interrupt Indicator

Each bit gives an indication of the channel that has requested for service. Bit-0 represents channel 0 and bit-3 indicates channel 3. Logic 1 indicates that a channel has called for service. Bits 4 to 7 are reserved and remain at logic 0 The interrupt bit clears after reading the appropriate register of the interrupting channel register, see Interrupt Clearing section.

INT0 register provides status for each channel



Registers INT3, INT2 and INT1 [32:8]

Twenty four bit encoded interrupt indicator. Each channel's interrupt is encoded into 3 bits for receive, transmit, and status. Bit [10:8] represent channel 0 and go up to channel 3 with bits [19:17]. The 3 bit encoding and their priority order are shown below in **Table 6**. The Timer and MPIO interrupts are for the device and therefore they exist within channel 0 space (bits [10:8]) only.

FIGURE 6. THE GLOBAL INTERRUPT REGISTER, INT0, INT1, INT2 AND INT3

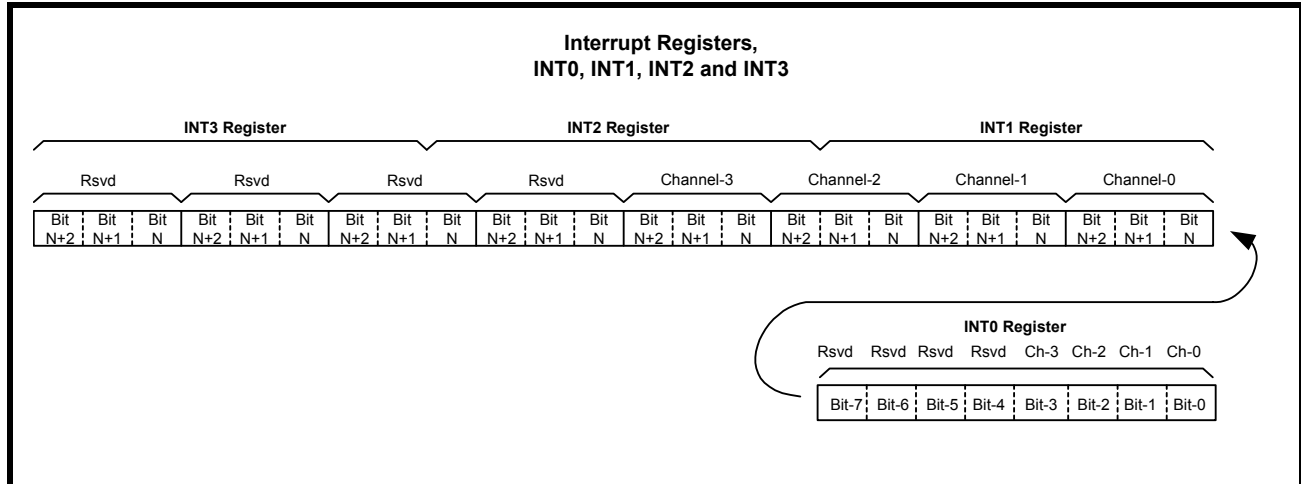


TABLE 6: UART CHANNEL [3:0] INTERRUPT SOURCE ENCODING

| PRIORITY | BIT[N+2] | BIT[N+1] | BIT[N] | INTERRUPT SOURCE(S) |
|----------|----------|----------|--------|--|
| x | 0 | 0 | 0 | None |
| 1 | 0 | 0 | 1 | RXRDY and RX Line Status (logic OR of LSR[4:1]) |
| 2 | 0 | 1 | 0 | RXRDY Time-out |
| 3 | 0 | 1 | 1 | TXRDY, THR or TSR (auto RS485 mode) empty |
| 4 | 1 | 0 | 0 | MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon det. or special char. detected |
| 5 | 1 | 0 | 1 | Reserved. |
| 6 | 1 | 1 | 0 | MPIO pin(s). Available only within channel 0, reserved in other channels. |
| 7 | 1 | 1 | 1 | TIMER Time-out. Available only within channel 0, reserved in other channels. |

TABLE 7: UART CHANNEL [3:0] INTERRUPT CLEARING:

| |
|--|
| RXRDY is cleared by reading data in the RX FIFO until it falls below the trigger level. |
| RXRDY Time-out is cleared by reading data until the RX FIFO is empty. |
| RX Line Status interrupt clears after reading the LSR register. |
| TXRDY interrupt clears after reading ISR register that is in the UART channel register set. |
| Modem Status Register interrupt clears after reading MSR register that is in the UART channel register set. |
| RTS/CTS or DTR/DSR delta interrupt clears after reading MSR register that is in the UART channel register set. |
| Xoff/Xon interrupt clears after reading the ISR register that is in the UART channel register set. |
| Special character detect interrupt is cleared by a read to ISR or after the next character is received. |
| TIMER Time-out interrupt clears after reading the TIMERCNTL register that is in the Device Configuration register set. |
| MPIO interrupt clears after reading the MPIOVLV register that is in the Device Configuration register set. |

2.2.2 General Purpose 16-bit Timer/Counter [TIMERMSB, TIMELSB, TIMER, TIMECNTL] (DEFAULT 0xXX-XX-00-00)

A 16-bit down-count timer for general purpose timer or counter. Its clock source may be selected from internal crystal oscillator or externally on pin TMRCK. The timer can be set to be a single-shot for a one-time event or re-triggerable for continue interval. An interrupt may be generated in the INT Register when the timer times out. It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. These registers provide start/stop and re-triggerable or one-shot operation. The time-out output of the Timer can be set to generate an interrupt for system or event alarm.

FIGURE 7. TIMER/COUNTER CIRCUIT.

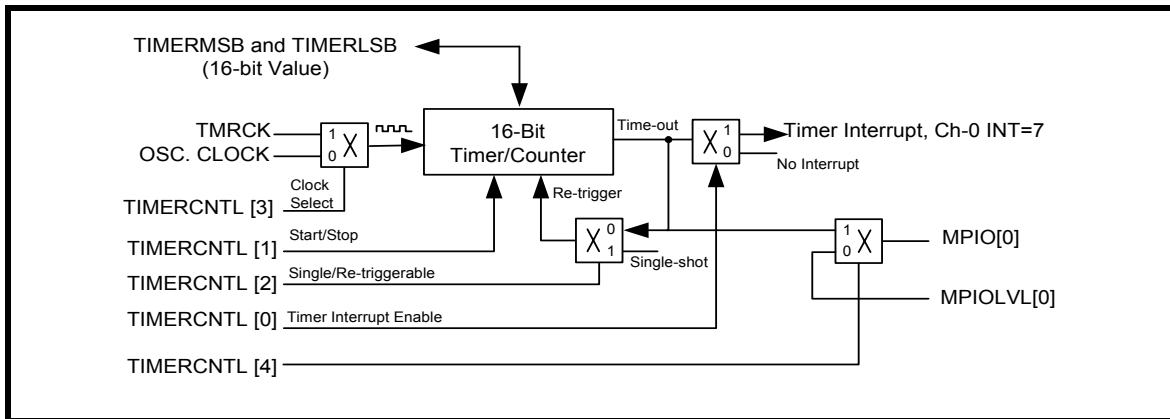
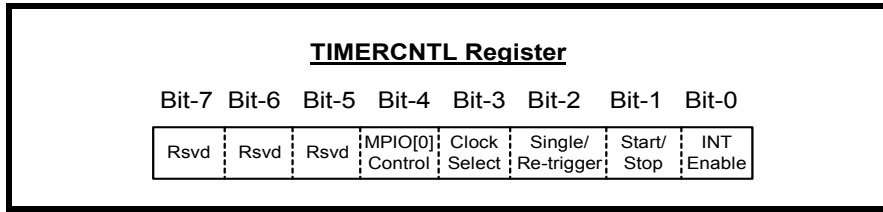


TABLE 8: TIMER CONTROL REGISTERS

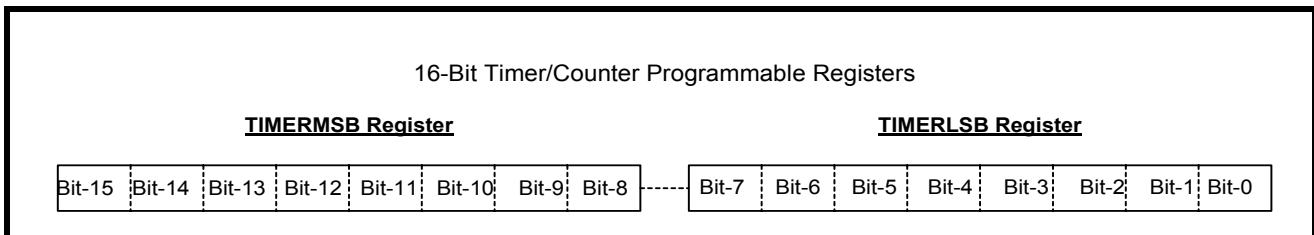
| | |
|-----------------|--|
| TIMERCNTL [0] | Logic zero (default) disables Timer-Counter interrupt and logic one enables the interrupt, reading the TIMERCNTL clears the interrupt. |
| TIMERCNTL [1] | Logic zero (default) stops/pauses the timer and logic one starts/re-starts the timer/counter. |
| TIMERCNTL [2] | Logic zero (default) selects re-trigger timer function and logic one selects one-shot (timer function). |
| TIMERCNTL [3] | Logic zero (default) selects internal and logic one selects external clock to the timer/counter. |
| TIMERCNTL [4] | Routes the Timer-Counter interrupt to MPIO[0] if MPIOSEL[0]=0 for external event control. |
| TIMERCNTL [7:5] | Reserved (defaults to zero) |



TIMER [15:8] - Reserved

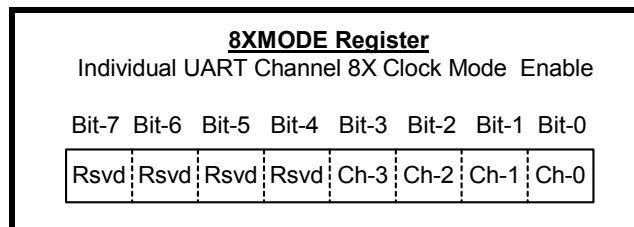
TIMERMSB [31:24] and TIMERLSB [23:16]

TIMERMSB and TIMERLSB form a 16-bit value. The least-significant bit of the timer is being bit [0] of the TIMERLSB with most-significant-bit being bit [7] in TIMERMSB. Notice that these registers do not hold the current counter value when read. Reading the TIMERCNTL register will clear its interrupt. Default value is zero (timer disabled) upon powerup and reset.



2.2.3 8XMODE [7:0] - (default 0x00)

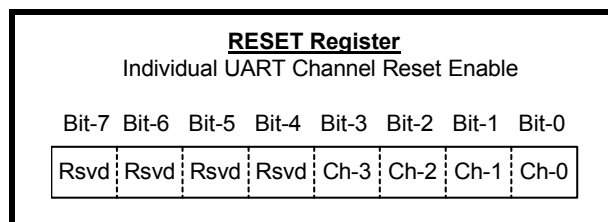
Each bit selects 8X or 16X sampling rate for that UART channel, bit-0 is channel 0. Logic 0 (default) selects normal 16X sampling with logic one selects 8X sampling rate. Transmit and receive data rates will double by selecting 8X.



2.2.4 REGA [15:8] Reserved

2.2.5 RESET [23:16] - (default 0x00)

The 8-bit Reset register [RESET] provides the software with the ability to reset the UART(s) when there is a need. Each bit is self-resetting after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition, see [Table 20](#) for details. Bit-0 =1 resets UART channel 0 with bit-3=1 resets channel 3..



2.2.6 SLEEP [31:24] - (default 0x00)

Each UART can be separately enabled to enter Sleep mode through the Sleep register. Sleep mode reduces power consumption when the system needs to put the UART(s) to idle. All of these conditions must be satisfied for the D154 to enter sleep mode:

- no interrupts pending (INT0 = 0x00)
- divisor is a non-zero value for all channels (ie. DLL = 0x1)
- sleep mode is enabled (SLEEP = 0x0F)
- modem inputs for all channels are not toggling (MSR bits 0-3 = 0)
- RX input pins for all channels are idling HIGH

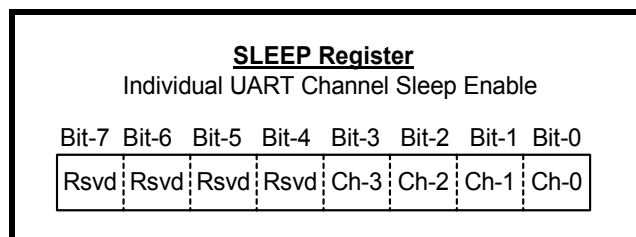
The D154 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The D154 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the D154 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the D154 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The D154 will stay in the sleep mode of operation until it is disabled by setting Sleep = 0x00. In this case, the quad UART is awoken by any of the UART channel from a receive data byte or a change on the serial port. The UART is ready after 32 crystal clocks to ensure full functionality. Also, a special interrupt is generated with an indication of no pending interrupt. Reading INT0 will clear this special interrupt. Logic 0 (default) is disable and logic 1 is enable to sleep mode.

Important: The XR17D154 is a versatile device designed to operate with different VCC (core power supply) and VIO(PCI bus I/O power supply). However, the VCC and VIO must be equal (VCC = VIO) for the sleep mode to reduce power consumption. Any difference in these voltages will result in high currents, when placed in sleep mode. If sleep mode is used, it is recommended that both VCC and VIO be powered by the PCI bus VIO power pins. If sleep mode is not used, there is no concern about high currents whether VCC = VIO or VCC > VIO. In any case, VCC should never be less than VIO.



2.2.7 Device Identification and Revision

There are two internal registers that provide device identification and revision, DVID and DREV registers. The 8-bit content in the DVID register provides device identification. A return value of 0x24 from this register indicates the device is an XR17D154 or an XR17C154. The DREV register returns an 8-bit value of 0x01 for revision A with 0x02 equals to revision B and so forth. This information is very useful to the software driver for identifying which device it is communicating with and to keep up with revision changes.

DVID [15:8]

Device identification for the type of UART. The upper nibble indicates it is a XR17xxxx series with lower nibble indicating the number of channels.

Examples:

XR17D158 or XR17C158 = 0x28

XR17D154 or XR17C154 = 0x24

XR17D152 or XR17C152 = 0x22

DREV [7:0]

Revision number of the XR17D154. A 0x01 represents "revision-A" with 0x02 for rev-B and so forth.

REGB [23:16] - (default 0x00)

REGB register provides a control for simultaneous write to all 4 UARTs configuration register or individually. This is very useful for device initialization in the power up and reset routines. Also, the register provides a facility to interface to the non-volatile memory device such as a 93C46 EEPROM. In embedded applications, the user can use this facility to store proprietary data.

2.2.8 REGB Register

| | |
|-----------------------|--|
| REGB[16] (Read/Write) | Logic 0 (default) write to each UART configuration registers individually. |
| | Logic 1 enables simultaneous write to all 4 UARTs configuration register. |
| REGB[19:17] | Reserved |
| REGB[20] (Write-Only) | Control the EECK, clock, output (pin 116) on the EEPROM interface. |
| REGB[21] (Write-Only) | Control the EECS, chips select, output (pin 115) to the EEPROM device. |
| REGB[22] (Write-Only) | EEDI (pin 114) data input. Write data to the EEPROM device. |
| REGB[23] (Read-Only) | EEDO (pin 113) data output. Read data from the EEPROM device. |

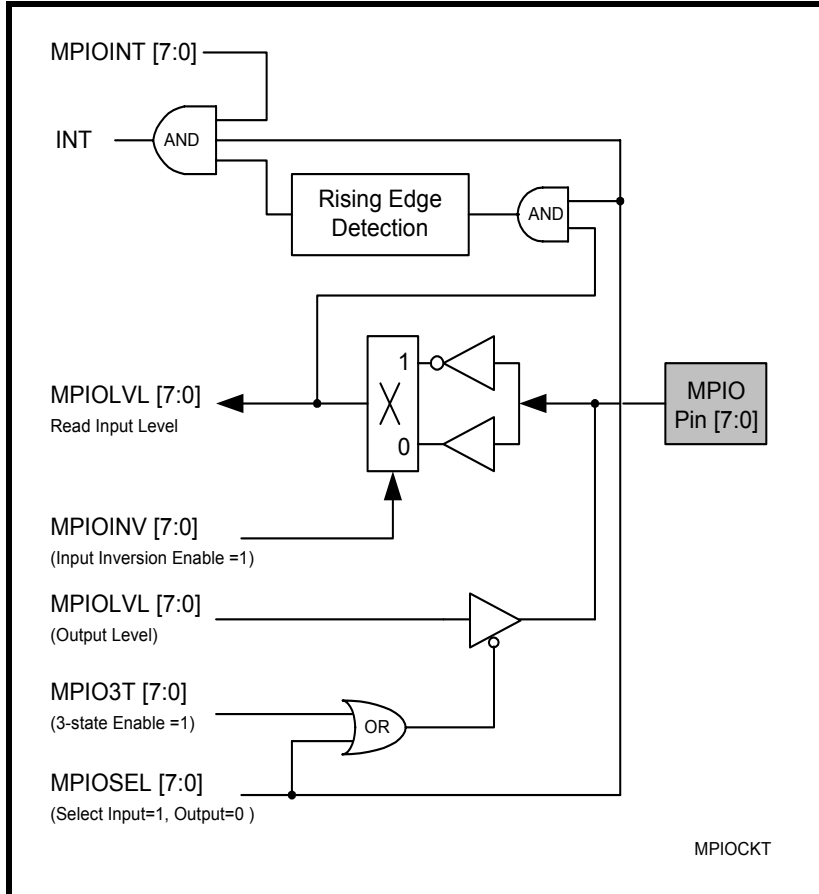
2.2.9 Multi-Purpose Inputs and Outputs

The D154 provides 8 multi-purpose inputs/outputs [MPIO7:0] for general use. Each pin can be programmed to be an input or output function. The input logic state can be set for normal or inverted level, and optionally set to generate an interrupt. The outputs can be set to be normal logic 1 or 0 state, or tri-state. Their functions and definitions are programmed through 5 registers: MPIOINT, MPIOVLV, MPIO3T, MPIOINV and MPIOSEL. If all 8 pins are set for inputs, all 8 interrupts would be OR'ed together. The Or'ed interrupt is reported in the channel 0 UART interrupt status, see Interrupt Status Register. The pins may also be programmed to be outputs and to the tri-state condition for signal sharing.

2.2.10 MPIO REGISTER

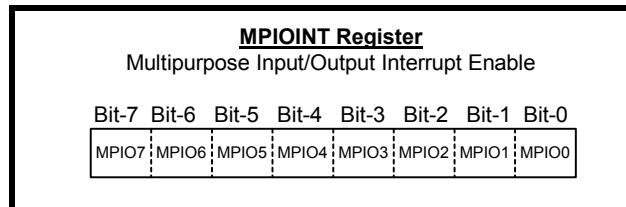
Bit 7 represents MPIO7 pin and bit 0 represents MPIO0 pin. There are 5 registers that select, control and monitor the 8 multipurpose inputs and outputs pins. **Figure 8** shows the internal circuitry.

FIGURE 8. MULTIPURPOSE INPUT/OUTPUT INTERNAL CIRCUIT



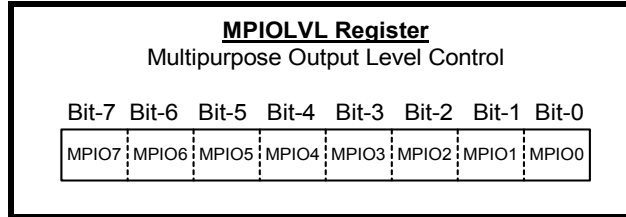
MPIOINT [7:0] - (default 0x00)

Enable multipurpose input pin interrupt. If the pin is selected by MPIOSEL as input then bit-0 enables input pin 0 for interrupt, and bit-7 enables input pin 7. No interrupt is enable if the pin is selected to be an output. The interrupt is edge sensing and determined by MPIOINV and MPIOLVL registers. The MPIO interrupt clears after a read to register MPIOLVL. The combination of MPIOLVL and MPIOINV determines the interrupt being active low or active high, it's level trigger. Logic 0 (default) disables the pin's interrupt and logic 1 enables it.



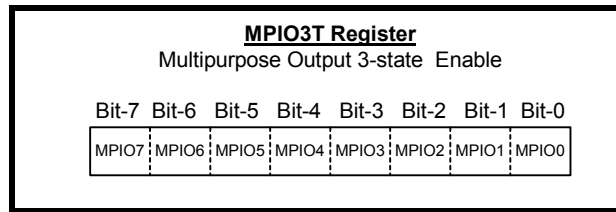
MPIOLVL [7:0] - (default 0x00)

Output pin level control and input level status. The status of the input pin(s) is read on this register and output pins are controlled on this register. A logic 0 (default) sets the output to low and a logic 1 sets the output pin to high. The MPIO interrupt will clear upon reading this register.



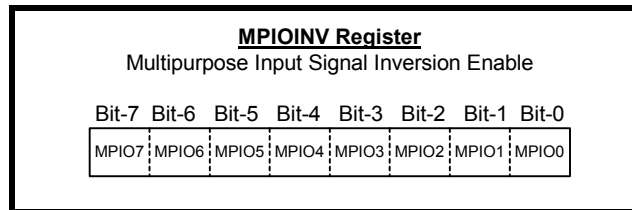
MPIO3T [7:0] - (default 0x00)

Output pin tri-state control. A logic 0 (default) sets the output to active level per register MPIOBIT settling, a logic 1 sets the output pin to tri-state.



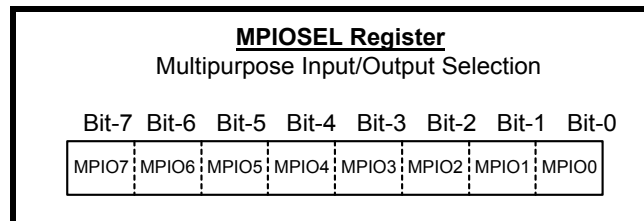
MPIOINV [7:0] - (default 0x00)

Input inversion control. A logic 0 (default) does not invert the input pin logic. A logic 1 inverts the input logic level.



MPIOSEL [7:0] - (default 0xFF)

Multipurpose input/output pin select. This register defines the functions of the pins. A logic 1 (default) defines the pin for input and a logic 0 for output.



3.0 CRYSTAL OSCILLATOR / BUFFER

The D154 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in each of the 4 UARTs, the 16-bit general purpose timer/counter and internal logics. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Caution: The XTAL1 input is not 5V tolerant. See Programmable Baud Rate Generator in the UART section for programming details.

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant with 10-22 pF capacitance load, 100ppm) connected externally between the XTAL1 and XTAL2 pins (see **Figure 9**). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal 4 baud rate generators for standard or custom rates. However, for external clock frequencies greater than 24MHz, a 2K pull-up may be necessary on the XTAL2 output (see **Figure 10**). Typically, the oscillator connections are shown in **Figure 9**. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

FIGURE 9. TYPICAL OSCILLATOR CONNECTIONS

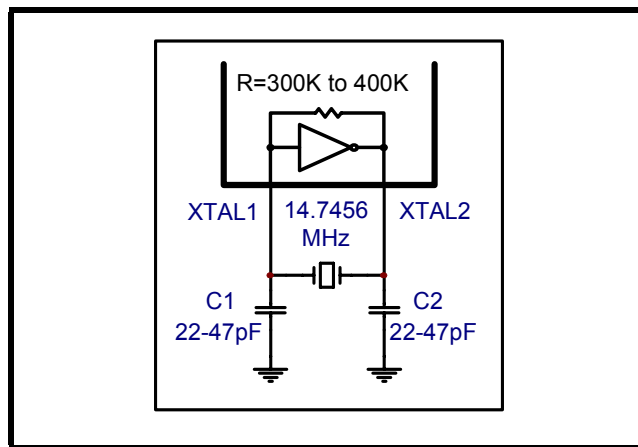
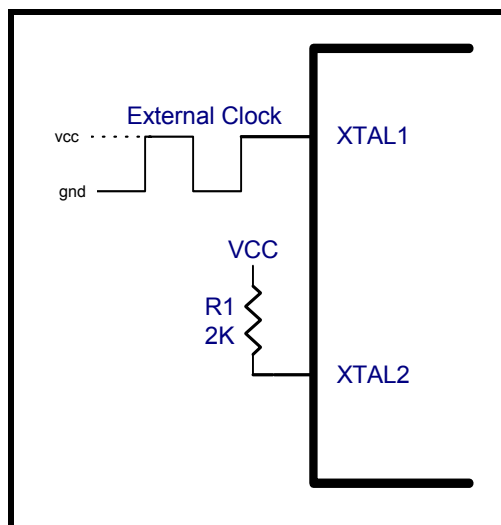


FIGURE 10. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE



4.0 TRANSMIT AND RECEIVE DATA

There are two methods to load transmit data and unload receive data from each UART channel. First, there is a transmit data register and receive data register for each UART channel in the device configuration register set to ease programming. These registers support 8, 16, 24 and 32 bits wide format. In the 32-bit format, it increases the data transfer rate on the PCI bus. Additionally, a special register location provides receive data byte with its associated error flags. This is a 16-bit or 32-bit read operation where the Line Status Register (LSR) content in the UART channel register is paired along with the data byte. This operation further facilitates data unloading with the error flags without having to read the LSR register separately. Furthermore, the XR17D154 supports PCI burst mode for read/write operation of up to 64 bytes of data.

The second method is through each UART channel's transmit holding register (THR) and receive holding register (RHR). The THR and RHR registers are 16550 compatible so their access is limited to 8-bit format. The software driver must separately read the LSR content for the associated error flags before reading the data byte.

4.1 DATA LOADING AND UNLOADING VIA 32-BIT PCI BURST TRANSFERS

The XR17D154 supports PCI Burst Read and PCI Burst Write transactions anywhere in the mapped memory region (except reserved areas). In addition, to utilize this feature fully, the device provides a separate memory location (apart from the 16550 register set) where the RX and the TX FIFO can be read from/written to, as shown in [Table 3](#). The following is an extract from the table showing the burstable memory locations:

Channel 0:

| | | |
|------------------|---|---|
| RX FIFO | : | 0x100 - 0x13F (64 bytes) |
| TX FIFO | : | 0x100 - 0x13F (64 bytes) |
| RX FIFO + status | : | 0x180 - 0x1FF (64 bytes data + 64 bytes status) |

Channel 1:

| | | |
|------------------|---|---|
| RX FIFO | : | 0x300 - 0x33F (64 bytes) |
| TX FIFO | : | 0x300 - 0x33F (64 bytes) |
| RX FIFO + status | : | 0x380 - 0x3FF (64 bytes data + 64 bytes status) |

Channel 2:

| | | |
|------------------|---|---|
| RX FIFO | : | 0x500 - 0x53F (64 bytes) |
| TX FIFO | : | 0x500 - 0x53F (64 bytes) |
| RX FIFO + status | : | 0x580 - 0x5FF (64 bytes data + 64 bytes status) |

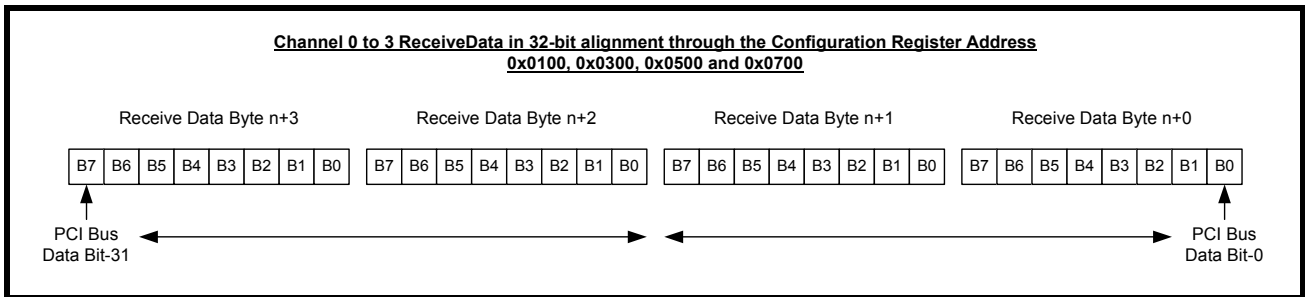
Channel 3:

| | | |
|------------------|---|---|
| RX FIFO | : | 0x700 - 0x73F (64 bytes) |
| TX FIFO | : | 0x700 - 0x73F (64 bytes) |
| RX FIFO + status | : | 0x780 - 0x7FF (64 bytes data + 64 bytes status) |

4.1.1 Normal Rx FIFO Data Unloading at locations 0x100, 0x300, 0x500, 0x700

The RX FIFO data (up to the maximum 64 bytes) can be read out in a single burst 32-bit read operation (maximum 16 DWORD reads) at memory locations 0x100 (channel 0), 0x300 (channel 1), 0x500 (channel 2), and 0x700 (channel 3). This operation is at least 16 times faster than reading the data in 64 separate 8-bit memory reads of RHR register (0x000 for channel 0, 0x200 for channel 1, 0x400 for channel 2, and 0x600 for channel 3).

| READ RX FIFO, WITH NO ERRORS | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 |
|---------------------------------|---------------|---------------|---------------|---------------|
| Read n+0 to n+3 | FIFO Data n+3 | FIFO Data n+2 | FIFO Data n+1 | FIFO Data n+0 |
| Read n+4 to n+7 | FIFO Data n+7 | FIFO Data n+6 | FIFO Data n+5 | FIFO Data n+4 |
| Etc. | | | | |



4.1.2 Special Rx FIFO Data Unloading at locations 0x180, 0x380, 0x580, and 0x780

The XR17D154 also provides the same RX FIFO data along with the LSR status information of each byte side-by-side, at locations 0x180 (channel 0), 0x380 (channel 1), 0x580 (channel 2), and 0x780 (channel 3). The entire RX data along with the status can be downloaded in a single PCI Burst Read operation of 32 DWORD reads. The Status and Data bytes must be read in 16 or 32 bits format to maintain data integrity. The following tables show this clearly.

| READ RX FIFO, WITH LSR ERRORS | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 |
|----------------------------------|---------------|---------|---------------|---------|
| Read n+0 to n+1 | FIFO Data n+1 | LSR n+1 | FIFO Data n+0 | LSR n+0 |
| Read n+2 to n+3 | FIFO Data n+3 | LSR n+3 | FIFO Data n+2 | LSR n+2 |
| Etc | | | | |

