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GENERAL DESCRIPTION

The XR17V354[1] (V354) is a single chip 4-channel PCI Express (PCIe) UART (Universal Asynchronous Receiver and Transmitter), optimized for higher performance and lower power. The V354 serves as a single lane PCIe bridge to 4 independent enhanced 16550 compatible UARTs. The V354 is compliant to PCIe 2.0 Gen 1 (2.5 GT/s).

In addition to the UART channels, the V354 has 16 multi-purpose I/Os (MPIOs), a 16-bit general purpose counter/timer and a global interrupt status register to optimize interrupt servicing.

Each UART of the V354 has many enhanced features such as the 256-bytes TX and RX FIFOs, programmable Fractional Baud Rate Generator, Automatic Hardware or Software Flow Control, Auto RS-485 Half-Duplex Direction Control, programmable TX and RX FIFO Trigger Levels, TX and RX FIFO Level Counters, infrared mode, and data rates up to 31.25 Mbps. The V354 is available in a 176-pin FPBGA package (13 x 13 mm).

NOTE 1: *Covered by U.S. Patents #5,649,122, #6,754,839, #6,865,626 and #6,947,999*

APPLICATIONS

- Next generation Point-of-Sale Systems
- Remote Access Servers
- Storage Network Management
- Factory Automation and Process Control
- Multi-port RS-232/RS-422/RS-485 Cards

FEATURES

- Single 3.3V power supply
- Internal buck regulator for 1.2V core
- PCIe 2.0 Gen 1 compliant
- x1 Link, dual simplex, 2.5 Gbps in each direction
- Expansion bus interface
- EEPROM interface for configuration
- Data read/write 32-bit operation
- Global interrupt status register for all four UARTs
- Up to 31.25 Mbps serial data rate
- 16 multi-purpose inputs/outputs (MPIOs)
- 16-bit general purpose timer/counter
- Sleep mode with wake-up Indicator
- Four independent UART channels controlled with
  - 16550 compatible register Set
  - 256-byte TX and RX FIFOs
  - Programmable TX and RX Trigger Levels
  - TX/RX FIFO Level Counters
  - Fractional baud rate generator
  - Automatic RTS/CTS or DTR/DSR hardware flow control with programmable hysteresis
  - Automatic Xon/Xoff software flow control
  - RS-485 half duplex direction control output with programmable turn-around delay
  - Multi-drop with Auto Address Detection
  - Infrared (IrDA 1.1) data encoder/decoder
- Software compatible to XR17C15x, XR17D15x, XR17V25x PCI UARTs

FIGURE 1. BLOCK DIAGRAM OF THE XR17V354

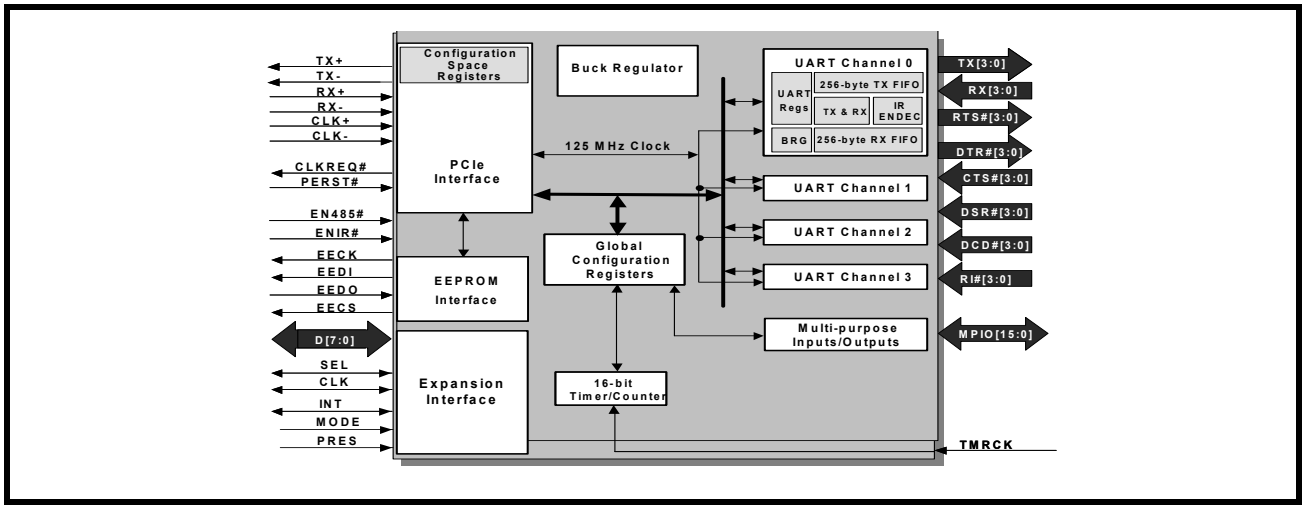
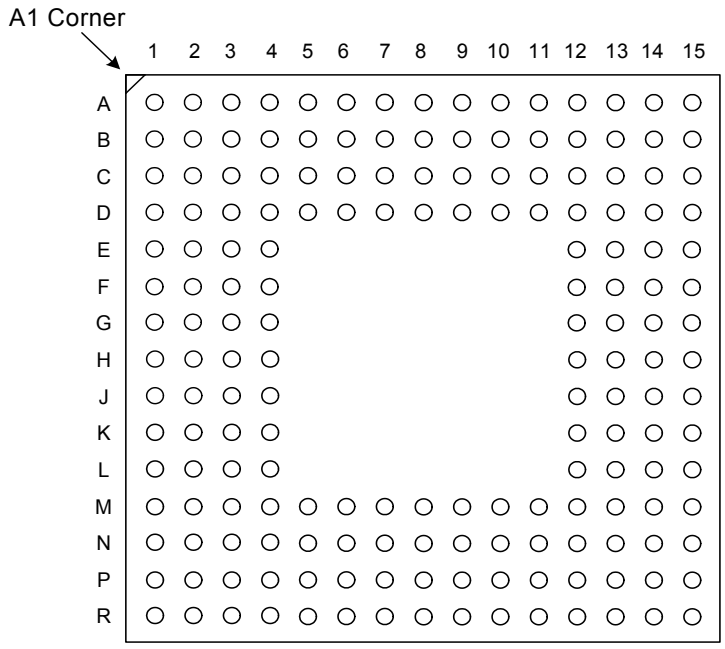


FIGURE 2. 176-FPBGA PINOUT



Transparent Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	NC	GND	NC	NC	DSR2#	GND	RTS2#	TMRCK	TEST2	GND	LX	LX	NC
B	NC	NC	NC	NC	NC	NC	CD2#	DTR2#	RX2	ENIR#	TEST1	GND	VCC33	VCC33	VCC33
C	MPIO0	NC	NC	NC	NC	NC	RI2#	CTS2#	TX2	EN485#	FB	GND	VCC33	ENABLE	D0
D	MPIO2	MPIO1	NC	GND	VCC33	GND	VCC12	GND	VCC33	GND	VCC12	GND	PWRGD	INT	D2
E	MPIO5	MPIO4	MPIO3	VCC12								VCC33	D1	D3	D4
F	GND	TEST0	MPIO6	GND								GND	D5	D6	D7
G	RX+	RX-	GND	CLK+								VCC12	SEL	CLK	MODE
H	GND	GND	REXT	CLK-								GND	RI1#	PRES	GND
J	TX+	TX-	GND	GND								VCC33	DTR1#	DSR1#	CD1#
K	GND	VCC12	VCC33	VCC12								GND	RTS1#	RX1	CTS1#
L	CLKREQ#	PERST#	MPIO7	GND								VCC12	CD0#	RI0#	TX1
M	GND	MPIO8	MPIO11	MPIO14	TMS	GND	VCC33	GND	VCC12	GND	NC	EEDO	RX0	DSR0#	GND
N	MPIO9	MPIO12	MPIO15	TRST#	TX3	CTS3#	CD3#	RI3#	NC	NC	NC	NC	TX0	CTS0#	DTR0#
P	MPIO10	MPIO13	TCK	TDO	RTS3#	DTR3#	NC	NC	NC	NC	NC	NC	EECK	EEDI	RTS0#
R	NC	RESET#	TDI	GND	RX3	DSR3#	NC	GND	NC	NC	NC	GND	NC	EECS	NC

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XR17V354IB176-F	176-FPBGA	-40°C to +85°C

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
PCIe SIGNALS			
CLK+ CLK-	G4 H4	I I	PCIe reference clock input. (Nominal single-ended swing from 0 to 700 mV.)
TX+ TX-	J1 J2	O O	PCIe differential TX outputs. Must be AC coupled using 0.1 uF non-polarized capacitor (0603 or smaller) near the transmitting source.
RX+ RX-	G1 G2	I I	PCIe differential RX inputs. Must be AC coupled using 0.1 uF non-polarized capacitor (0603 or smaller) near the transmitting source.
CLKREQ#	L1	O	PCIe edge connector clock request
PERST#	L2	I	PCIe edge connector reset
REXT	H3		Connect a 191 ohm 1% resistor to GND. This is used for PCIe PHY calibration.
MODEM OR SERIAL I/O INTERFACE			
TX0	N13	O	UART channel 0 Transmit Data or infrared transmit data.
RX0	M13	I	UART channel 0 Receive Data or infrared receive data. Normal RXD input idles at HIGH condition. The infrared pulses can be inverted internally prior to decoding by setting FCTR bit [4]. If unused, a pull-up or pull-down resistor is recommended on this pin.
RTS0#	P15	O	UART channel 0 Request to Send or general purpose output (active LOW).
CTS0#	N14	I	UART channel 0 Clear to Send or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
DTR0#	N15	O	UART channel 0 Data Terminal Ready or general purpose output (active LOW).
DSR0#	M14	I	UART channel 0 Data Set Ready or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
CD0#	L13	I	UART channel 0 Carrier Detect or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
RI0#	L14	I	UART channel 0 Ring Indicator or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
TX1	L15	O	UART channel 1 Transmit Data or infrared transmit data.
RX1	K14	I	UART channel 1 Receive Data or infrared receive data. Normal RXD input idles at HIGH condition. The infrared pulses can be inverted prior to decoding by setting FCTR bit [4]. If unused, a pull-up or pull-down resistor is recommended on this pin.
RTS1#	K13	O	UART channel 1 Request to Send or general purpose output (active LOW).
CTS1#	K15	I	UART channel 1 Clear to Send or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
DTR1#	J13	O	UART channel 1 Data Terminal Ready or general purpose output (active LOW).

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
DSR1#	J14	I	UART channel 1 Data Set Ready or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
CD1#	J15	I	UART channel 1 Carrier Detect or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
RI1#	H13	I	UART channel 1 Ring Indicator or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
TX2	C9	O	UART channel 2 Transmit Data or infrared transmit data.
RX2	B9	I	UART channel 2 Receive Data or infrared receive data. Normal RXD input idles at HIGH condition. The infrared pulses can be inverted prior to decoding by setting FCTR bit [4]. If unused, a pull-up or pull-down resistor is recommended on this pin.
RTS2#	A9	O	UART channel 2 Request to Send or general purpose output (active LOW).
CTS2#	C8	I	UART channel 2 Clear to Send or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
DTR2#	B8	O	UART channel 2 Data Terminal Ready or general purpose output (active LOW).
DSR2#	A7	I	UART channel 2 Data Set Ready or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
CD2#	B7	I	UART channel 2 Carrier Detect or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
RI2#	C7	I	UART channel 2 Ring Indicator or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
TX3	N5	O	UART channel 3 Transmit Data or infrared transmit data.
RX3	R5	I	UART channel 3 Receive Data or infrared receive data. Normal RXD input idles at HIGH condition. The infrared pulses can be inverted prior to decoding by setting FCTR bit [4]. If unused, a pull-up or pull-down resistor is recommended on this pin.
RTS3#	P5	O	UART channel 3 Request to Send or general purpose output (active LOW).
CTS3#	N6	I	UART channel 3 Clear to Send or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
DTR3#	P6	O	UART channel 3 Data Terminal Ready or general purpose output (active LOW).
DSR3#	R6	I	UART channel 3 Data Set Ready or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
CD3#	N7	I	UART channel 3 Carrier Detect or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.
RI3#	N8	I	UART channel 3 Ring Indicator or general purpose input (active LOW). If unused, a pull-up or pull-down resistor is recommended on this pin.

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
EXPANSION INTERFACE			
MODE	G15	I	Expansion Interface Mode Select. Connect this pin to VCC to enable master mode. Connect this pin to GND to enable slave mode.
CLK	G14	I/O	Expansion Interface Clock. In master mode, this pin is the clock output to the slave device. In slave mode, this pin is the clock input from the master device. The expansion interface clock is 62.5 MHz. The UARTs on the slave device will need to use different baud rate generator divisors than the master device. The trace capacitance between the master and slave device must be less than 25pF.
D7	F15	I/O	Expansion Interface Data 7 (MSB) with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
D6	F14	I/O	Expansion Interface Data 6 with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
D5	F13	I/O	Expansion Interface Data 5 with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
D4	E15	I/O	Expansion Interface Data 4 with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
D3	E14	I/O	Expansion Interface Data 3 with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
D2	D15	I/O	Expansion Interface Data 2 with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
D1	E13	I/O	Expansion Interface Data 1 with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
D0	C15	I/O	Expansion Interface Data 0 (LSB) with internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
SEL	G13	I/O	Expansion Interface Read/Write Select. This is the the read/write select input in the slave mode. This is the read/write select output in the master mode. This pin has an internal pull-down resistor. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
INT	D14	I/O	Expansion Interface Interrupt. This is the expansion interface interrupt output in the slave mode. This is the expansion interface interrupt input in the master mode. This pin has an internal pull-down resistor and can be left unconnected if there is no slave device. If a slave device is present, connect between master and slave with trace capacitance of less than 25 pF. Leave unconnected if no slave device is present.
PRES	H14	I	Slave Present, has internal pull-down resistor. In master mode, pull this pin to VCC to check if a slave is device present. Connect this pin to GND or leave unconnected if there is no slave device or to disable checking for a slave device.

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
MPIO SIGNALS			
MPIO0	C1	I/O	Multi-purpose input/output 0. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO1	D2	I/O	Multi-purpose input/output 1. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO2	D1	I/O	Multi-purpose input/output 2. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO3	E3	I/O	Multi-purpose input/output 3. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO4	E2	I/O	Multi-purpose input/output 4. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO5	E1	I/O	Multi-purpose input/output 5. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO6	F3	I/O	Multi-purpose input/output 6. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO7	L3	I/O	Multi-purpose input/output 7. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO8	M2	I/O	Multi-purpose input/output 8. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO9	N1	I/O	Multi-purpose input/output 9. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO10	P1	I/O	Multi-purpose input/output 10. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
MPIO11	M3	I/O	Multi-purpose input/output 11. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO12	N2	I/O	Multi-purpose input/output 12. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO13	P2	I/O	Multi-purpose input/output 13. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO14	M4	I/O	Multi-purpose input/output 14. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
MPIO15	N3	I/O	Multi-purpose input/output 15. This pin defaults to an input with interrupts disabled and is controlled using the MPIOSEL, MPIOLVL, MPIOINV, MPIO3T, MPIOOD and MPIOINT configuration registers. If unused, a pull-up or pull-down resistor is recommended on this pin.
EEPROM SIGNALS			
EECK	P13	I/O	Serial clock output uses the internal 125 MHz clock divided by 256 (488 KHz) following power-up or reset to read an external EEPROM. This pin may also be manually clocked using the Configuration Register REGB.
EECS	R14	I/O	Active high chip select output to an external EEPROM with internal weak pull-down resistor. Connect an external 4.7K ohm pull-up resistor to this pin to enable reading of an external EEPROM. This pin may also be manually enabled using the Configuration Register REGB.
EEDI	P14	O	Write data to EEPROM device. It is manually accessible thru the Configuration Register REGB.
EEDO	M12	I	Read data from EEPROM device with internal pull-down resistor. It is manually accessible thru the Configuration Register REGB.
JTAG SIGNALS			
TRST#	N4	I	JTAG Test Reset. This signal is active LOW with internal pull-up resistor
TCK	P3	I	JTAG Test Clock
TMS	M5	I	JTAG Test Mode Select with internal pull-up resistor
TDI	R3	I	JTAG Data Input with internal pull-up resistor
TDO	P4	O	JTAG Data Output

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
BUCK REGULATOR SIGNALS			
ENABLE	C14	I	Logic '1' enables, logic '0' disables buck regulator output.
LX LX	A13 A14	O O	Output of internal buck regulator. Use 4.7 uH inductor and connect to FB pin as shown in **Figure 3**.
FB	C11	I	Buck regulator feedback. Decouple with 47uF capacitor and connect to LX pins through 4.7 uH inductor as shown in **Figure 3**.
PWRGD	D13	O	Indicates that 1.2V core has been powered up.
ANCILLARY SIGNALS			
RESET#	R2	I	System reset (active low). In normal operation, this signal should be HIGH.
TMRCK	A10	I	16-bit timer/counter external clock input.
EN485#	C10	I	Auto RS-485 mode enable (active low). This pin is sampled during power up, following a hardware reset (RST#) or soft reset (register RESET). It can be used to start up all 4 UARTs in the Auto RS-485 Half-Duplex Direction control mode. The sampled logic state is transferred to FCTR bit-5 in the UART channel.
ENIR#	B10	I	Infrared mode enable (active low). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up all 4 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART.
TEST0 TEST1 TEST2	F2 B11 A11	I I I	Factory Test Modes. For normal operation, connect to GND.
POWER / GROUND / NO CONNECT			
VCC33	D5, D9, E12, J12, M7	Pwr	3.3V I/O power supply.
VCC33A	K3	Pwr	3.3V analog PHY power supply. A ferrite bead is recommended on this pin.
VCC33P	B13, C13	Pwr	3.3V power supply voltage for output stage of buck regulator.
VCC33B	B14, B15	Pwr	3.3V power supply for the analog blocks of the buck regulator.
VCC12	D7, D11, E4, G12, K4, L12, M9	Pwr	1.2V core power supply. A ferrite bead is recommended on these pins.
VCC12A	K2	Pwr	1.2V analog PHY power supply. A ferrite bead is recommended on this pin.

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
GND	A4, A8, A12, B12, C12, D4, D6, D8, D10, D12, F1, F4, F12, G3, H1, H2, H12, H15, J3, J4, K1, K12, L4, M1, M6, M8, M10, M15, R4, R8, R12	Pwr	Power supply common, ground.
NC	A1, A2, A3, A5, A6, A15, B1, B2, B3, B4, B5, B6, C2, C3, C4, C5, C6, D3, M11, N9, N10, N11, N12, P7, P8, P9, P10, P11, P12, R1, R7, R9, R10, R11, R13, R15	-	No internal connection.

NOTE: *Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain, OT=Output Tristate, IS=Input Schmitt Trigger.*

FUNCTIONAL DESCRIPTION

The XR17V354 (V354) integrates the functions of four independent enhanced 16550 UARTs, a general purpose 16-bit timer/counter, and 16 multi-purpose I/Os (MPIOs). Each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status and data transfer. The device configuration registers include a set of four consecutive interrupt source registers that provides interrupt status for all four UARTs, timer/counter, MPIOs and a sleep wake-up indicator. Additionally, each UART channel has 256-byte of transmit and receive FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control, automatic XON/XOFF, special character flow control, programmable transmit and receive FIFO trigger levels, infrared encoder/decoder (IrDA ver. 1.1), and a programmable fractional baud rate generator with a prescaler of divide by 1 or 4, and a data rate up to 31.25 Mbps with the 4X sampling rate.

PCI Local Bus Configuration Space Registers

A set of local bus configuration space register is provided. These registers provide the PCI vendor ID, device ID, sub-vendor ID, product model number, resources and capabilities which is collected by the host during the auto configuration phase that follows immediately after a power up or system reset/reboot. After the host has sorted out all devices on the bus, it defines and download the operating conditions to the cards. One of the definitions is the base address loaded into the Base Address Register (BAR) where the card will be operating in the PCI local bus memory space. All this is described in more detail in **"Section 1.1, PCI LOCAL BUS CONFIGURATION SPACE REGISTERS" on page 11**.

EEPROM Interface

An external 93C46 EEPROM is used to store words of information such as PCI Vendor ID, PCI Device ID, Class Code, etc. Details of this information can be found in **"Section 1.2, EEPROM Interface" on page 15**. This information is only used with the plug-and-play auto configuration of the PCI local bus. These data provide automatic hardware installation onto the PCI bus. The EEPROM interface consists of 4 signals, EEDI, EEDO, EECS, and EECK. The EEPROM is not needed when auto configuration is not required in the application. However, if your design requires non-volatile memory for other purpose, it is possible to store and retrieve data on the EEPROM through a special PCI device configuration register. See application note DAN112 for its programming details.

Expansion Interface

The expansion interface of the V354 is used to connect a master device to a slave device in order to add additional UART ports. All pins of the expansion interface must be connected between the two devices or to logic levels as specified in the pin descriptions for each of the signals.

Buck Regulator

The on chip buck regulator provides a 1.2V output from the device when enabled. This voltage can in turn be used to provide power to the digital core and analog Phy as depicted in **Figure 3**.

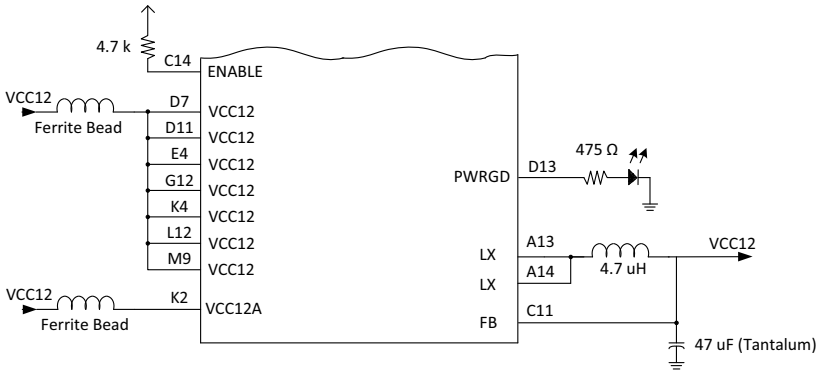


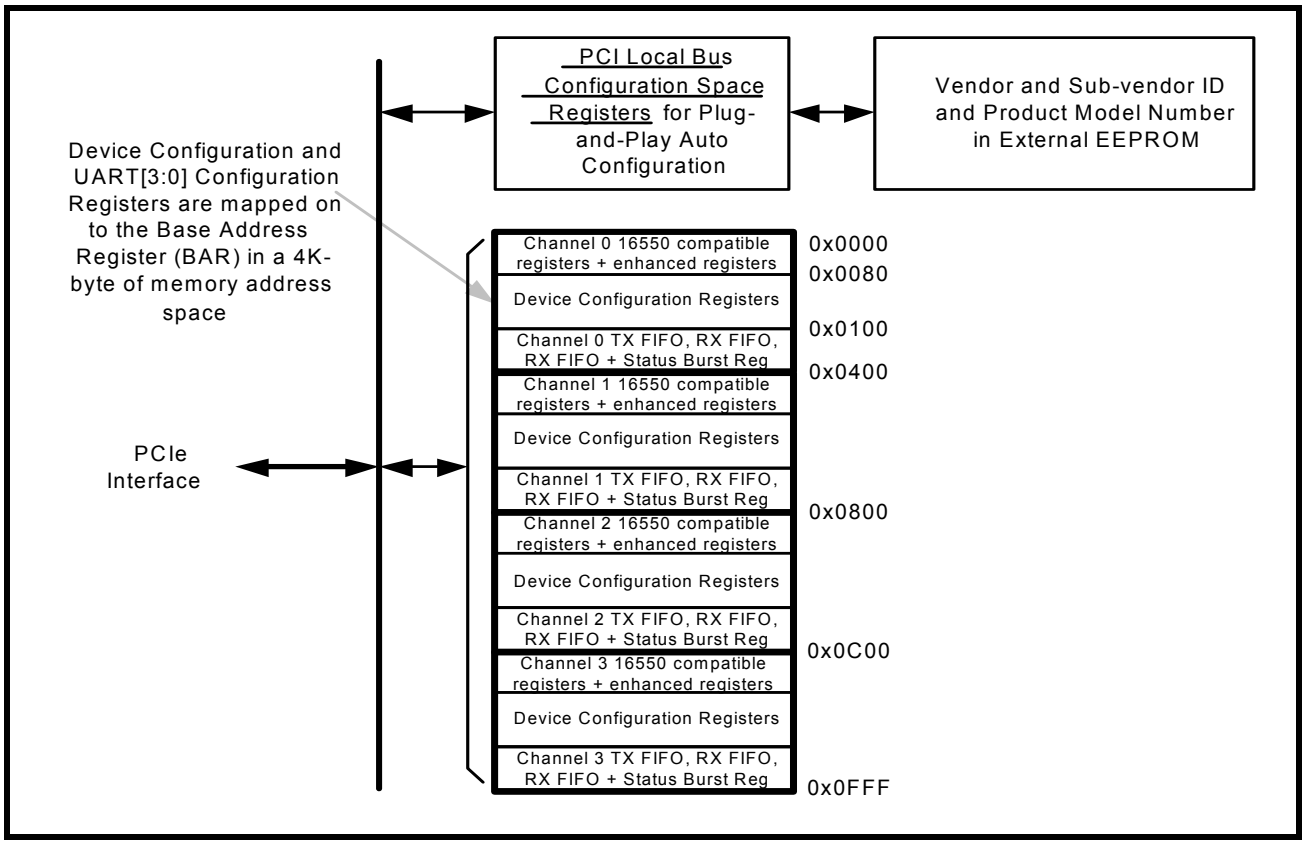
Figure 3. Buck Regulator

1.0 XR17V354 INTERNAL REGISTERS

The XR17V354 UART register set is very similar to the previous generation PCI UARTs. This makes the V354 software compatible with the previous generation PCI UARTs. Minimal changes are needed to the software driver of an existing Exar PCI UART driver so that it can be used with the V354 PCIe UART.

There are three different sets of registers as shown in Figure 4. The ***PCI Local Bus Configuration Space Registers*** are needed for plug-and-play auto-configuration. This auto-configuration feature makes installation very easy into a PCI system and it is part of the PCI local bus specification. The second register set is the ***Device Configuration Registers*** that are also accessible directly from the PCI bus for programming general operating conditions of the device and monitoring the status of various functions common to all four channels. These functions include all 4 channel UARTs' interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode, soft-reset, and device identification and revision. And lastly, each UART channel has its own set of internal ***UART Configuration Registers*** for its own operation control and status reporting. All 4 sets of channel registers are embedded inside the device configuration registers space, which provides faster access. The second and third set of registers are mapped into 4K of the PCI bus memory address space. The following paragraphs describe all 3 sets of registers in detail.

FIGURE 4. THE XR17V354 REGISTER SETS



1.1 PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

The PCI local bus configuration space registers are responsible for setting up the device's operating environment in the PCI local bus. The pre-defined operating parameters of the device is read by the PCI bus plug-and-play auto-configuration manager in the operating system. After the PCI bus has collected all data from every device/card on the bus, it defines and downloads the memory mapping information to each device/card about their individual operation memory address location and conditions. The operating memory mapped address location is downloaded into the Base Address Register (BAR) register, located at an address offset of 0x10 in the configuration space. Custom modification of certain registers is possible by using an external

93C46 EEPROM. The EEPROM contains the device vendor and sub-vendor data, along with 6 other words of information (see **"Section 1.2, EEPROM Interface" on page 15**) required by the auto-configuration setup.

TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS OFFSET	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX OR BINARY)
0x00	31:16	EWR	Device ID - No slave device on expansion interface Device ID - XR17V358 slave device on expansion interface Device ID - XR17V354 slave device on expansion interface	0x0354 0x8354 0x4354
	15:0	EWR	Vendor ID (Exar) specified by PCISIG	0x13A8
0x04	31 30	RWC RWC	Parity error detected. Cleared by writing a logic 1. System error detected. Cleared by writing a logic 1.	0b 0b
	29:28	RO	Unused	00b
	27	RO	Target Abort.	0b
	26:25	RO	DEVSEL# timing.	00b
	24	RO	Unimplemented bus master error reporting bit	0b
	23	RO	Fast back to back transactions are supported	0b
	22	RO	Reserved Status bit	0b
	21	RO	66MHz capable	0b
	20	RO	Capabilities List	1b
	19:16	RO	Reserved Status bits	0000b
	15:11, 9,7, 5, 4, 3, 2	RO	Command bits (reserved)	0x0000
	10	RWR	This bit disables the device from asserting INTx#. logic 1 = disable assertion of INTx# and logic 0 = enables assertion of INTx#	0b
	8	RWR	SERR# driver enable. logic 1=enable driver and 0=disable driver	0b
	6	RWR	Parity error enable. logic 1=respond to parity error and 0=ignore	0b
	1	RWR	Command controls a device's response to mem space accesses: 0=disable mem space accesses, 1=enable mem space accesses	0b
	0	RO	Device's response to I/O space accesses is disabled. (0 = disable I/O space accesses)	0b
0x08	31:8	EWR	Class Code (Default is 'Simple 550 Communication Controller')	0x070002
	7:0	RO	Revision ID (Exar device revision number)	Current Rev. value
0x0C	31:24	RO	BIST (Built-in Self Test)	0x00
	23:16	RO	Header Type (a single function device with one BAR)	0x00
	15:8	RO	Unimplemented Latency Timer (needed only for bus master)	0x00
	7:0	RO	Unimplemented Cache Line Size	0x00

TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS OFFSET	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX OR BINARY)
0x10	31:14	RWR	Memory Base Address Register (BAR0)	0x00000
	13:0	RO	Claims an 16K address space for the memory mapped UARTs including the UARTs on the expansion interface.	0x0000
0x14	31:0	RWR	Unimplemented Base Address Register (returns zeros)	0x00000000
0x18h	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x1C	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x20	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x24	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x28	31:0	RO	Reserved	0x00000000
0x2C	31:16	EWR	Subsystem ID (write from external EEPROM by customer)	0x0000
	15:0	EWR	Subsystem Vendor ID (write from external EEPROM by customer)	0x0000
0x30	31:0	RO	Expansion ROM Base Address (Unimplemented)	0x00000000
0x34	31:8	RO	Reserved (returns zeros)	0x000000
	7:0	RO	Capability Pointer	0x50
0x38	31:0	RO	Reserved (returns zeros)	0x00000000
0x3C	31:24	RO	Unimplemented MAXLAT	0x00
	23:16	RO	Unimplemented MINGNT	0x00
	15:8	RO	Interrupt Pin, use INTA#.	0x01
	7:0	RWR	Interrupt Line.	0xXX
0x40	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000
0x44	31:0	RO	CSR	0x02106160
0x48	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000
0x4C	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000
0x50	31:16	RO	64-bit address capable	0x0080
	15:8	RO	Next Capability Pointer	0x78
	7:0	RO	MSI Capable Capability ID	0x05
0x54-0x67	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000
0x68	31:0	RO	Not implemented or not applicable	0x0000xxxx
0x6C-0x77	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000

TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS OFFSET	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX OR BINARY)
0x78	31:16	RO	PME# support (PME# can be asserted from D3hot and D0) PCI Power Management 1.2	0x4803
	15:8	RO	Next Capability Pointer	0x80
	7:0	RO	Power Management Capability ID	0x01
0x7C	31:0	RO	No soft reset when transitioning from D3hot to D0 state	0x00000008
0x80	31:16	RO	PCI Express 2.0 capable endpoint, Interrupt Message Number 1	0x0202
	15:8	RO	Next Capability Pointer	0x00
	7:0	RO	PCI Express Capability ID	0x10
0x84	31:16	RO	Not implemented or not applicable (return zeros)	0x0000
	15:8	RO	Role-Based Error Reporting	0x80
	7:0	RO	256 bytes max payload size	0x01
0x88	31:16	RW	Not implemented or not applicable (return zeros)	0x0000
	15:8	RW	512 bytes max read request, Enable No Snoop	0x28
	7:0	RW	256 bytes max TLP payload size	0x10
0x8C	31:24	RO	Port Number	0x01
	23:22	RO	Not implemented or not applicable (return zeros)	00b
	21:18	RO	Not implemented or not applicable (return zeros)	0000b
	17:15	RO	L1 Exit Latency < 1 us	000b
	14:12	RO	L0s Exit Latency < 64 ns	000b
	11:10	RO	Active State Power Management (ASPM) Support L0s and L1 Supported	11b
	9:4	RO	x1 max Link Width	000001b
	3:0	RO	2.5 GT/s Link speed supported	0001b
0x90	31:21	RO	Not implemented or not applicable (return zeros)	00000000000b
	20	RO	Data Link Layer Active Reporting capable	1b
	19	RO	Surprise Down Error Reporting not supported	0b
	18	RO	Reference clock must not be removed.	0b
	17:15	RO	L1 Exit Latency - 2 us to less than 4 us	010b
	14:10	RO	Not implemented or not applicable (return zeros)	00000b
	9:4	RO	x1 negotiated Link Width	000001b
	3:0	RO	Current Link Speed is 2.5 GT/s	0001b
0x94	31:0	RO	PCIe Capability Offset 0x14 - Slot Capabilities Register	0x00040000
0x98-0xAF	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000

TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS OFFSET	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX OR BINARY)
0xB0	31:0	RO	PCIe Capability Offset 0x30 - Link Status2/Control2	0x00010001
0xB4-0xFF	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000
0x100	31:0	RO	VC Resource Capability Register	0x00010002
0x104-0x113	31:0	RO	Not implemented or not applicable (return zeros)	0x00000000
0x114	31:0	RO	VC Offset 0x4	0x8000000FF

NOTE: *EWR=Read/Write from external EEPROM. RWR=Read/Write. RO= Read Only. RWC=Read/Write-Clear.*

1.2 EEPROM Interface

The V354 provides an interface to an Electrically Erasable Programmable Read Only Memory (EEPROM). The EEPROM must be a 93C46-like device, with its memory configured as 16-bit words. This interface is provided in order to program the registers in the PCI Configuration Space of the PCI UART during power-up. The EEPROM must be organized into address/data pairs. The first word of the pair is the address and the second word is the data. Table 2 below shows the format of the 16-bit address:

TABLE 2: EEPROM ADDRESS BIT DEFINITIONS

BIT(S)	DEFINITION
15	Parity Bit - Odd parity over entire address/data pair If there is a parity error, it will be reported in bit-3 of the REGB register in the Device Configuration Registers (offset 0x08E).
14	Final Address If 1, this will be the last data to be read. If 0, there will be more data to be read after this.
13:8	Reserved - Bits must be ’0’
7:0	Target Address - See Table 3

Table 3 shows the Target Addresses available for programming into bits 7:0 of the 16-bit address word. All other Target Addresses are reserved and must not be used.

TABLE 3: TARGET ADDRESS FOR EEPROM VALUES

TARGET ADDRESS	DATA	EXAR DEFAULT
0x00	Vendor ID	0x13A8
0x01	Device ID	0x0354 - No slave 0x4354 - XR17V354 slave present 0x8354 - XR17V358 slave present
0x02	Class Code [7:0] lower 8-bits are reserved	0x0200
0x03	Class Code [23:8]	0x0700
0x04	Subsystem Vendor ID	0x0000
0x05	Subsystem ID	0x0000

The second 16-bit word of the address/data pair is the data. The default values are shown in Table 3. The address/data pairs can be in any order. Only the contents which need to be changed from the Exar defaults need to be included in the EEPROM.

1.3 Device Internal Register Sets

The ***Device Configuration Registers*** and the four individual ***UART Configuration Registers*** of the V354 occupy 4K of PCI bus memory address space. These addresses are offset onto the basic memory address, a value loaded into the Memory Base Address Register (BAR) in the PCI local bus configuration register set. The UART Configuration Registers are mapped into 4 address blocks where each UART channel occupies 1024 bytes memory space for its own registers that include the 16550 compatible registers. The Device Configuration Registers are accessible from all UART channels. However, not all bits can be controlled by all channels. The UART channel can only control the 8XMODE, 4XMODE, RESET and SLEEP register bits that apply to that particular channel. For example, this prevents channel 0 from accidentally resetting channel 1.

All these registers can be accessed in 8, 16, 24 or 32 bits width depending on the starting address given by the host at the beginning of the bus cycle. Transmit and receive data may be loaded or unloaded in 8, 16, 24 or 32 bits format in special locations given in the Table 4 below. Every time a read or write operation is made to the transmit or receive register, its FIFO data pointer is automatically bumped to the next sequential data location either in byte, word or DWORD. One special case applies to the receive data unloading when reading the receive data together with its LSR register content. The host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags. These special registers are further discussed in **"Section 2.1, FIFO DATA LOADING AND UNLOADING IN 32-BIT FORMAT" on page 30**.

TABLE 4: XR17V354 UART AND DEVICE CONFIGURATION REGISTERS

OFFSET ADDRESS	MEMORY SPACE	READ/WRITE	COMMENT
0x0000 - 0x000F	UART channel 0 Regs	(Table 13 & Table 14)	First 8 regs are 16550 compatible
0x0010 - 0x007F	Reserved		
0x0080 - 0x009A	DEVICE CONFIGURATION REGISTERS	(Table 5)	
0x009B - 0x00FF	Reserved		
0x0100 - 0x01FF	UART 0 – Read FIFO	Read-Only	256 bytes of RX FIFO data
0x0100 - 0x01FF	UART 0 – Write FIFO	Write-Only	256 bytes of TX FIFO data
0x0200 - 0x03FF	UART 0 – Read FIFO with errors	Read-Only	256 bytes of RX FIFO data + LSR
0x0400 - 0x040F	UART channel 1 Regs	(Table 13 & Table 14)	First 8 regs are 16550 compatible
0x0410 - 0x047F	Reserved		
0x0480 - 0x049A	DEVICE CONFIGURATION REGISTERS	(Table 5)	
0x049B - 0x04FF	Reserved		
0x0500 - 0x05FF	UART 1 – Read FIFO	Read-Only	256 bytes of RX FIFO data
0x0500 - 0x05FF	UART 1 – Write FIFO	Write-Only	256 bytes of TX FIFO data
0x0600 - 0x07FF	UART 1 – Read FIFO with errors	Read-Only	256 bytes of RX FIFO data + LSR
0x0800 - 0x080F	UART channel 2 Regs	(Table 13 & Table 14)	First 8 regs are 16550 compatible
0x0810 - 0x087F	Reserved		
0x0880 - 0x089A	DEVICE CONFIGURATION REGISTERS	(Table 5)	
0x089B - 0x08FF	Reserved		
0x0900 - 0x09FF	UART 2 – Read FIFO	Read-Only	256 bytes of RX FIFO data
0x0900 - 0x09FF	UART 2 – Write FIFO	Write-Only	256 bytes of TX FIFO data
0x0A00 - 0x0BFF	UART 2 – Read FIFO with errors	Read-Only	256 bytes of RX FIFO data + LSR
0x0C00 - 0x0C0F	UART channel 3 Regs	(Table 13 & Table 14)	First 8 regs are 16550 compatible
0x0C10 - 0x0C7F	Reserved		
0x0C80 - 0x0C9A	DEVICE CONFIGURATION REGISTERS	(Table 5)	
0x0C9B - 0x0CFF	Reserved		
0x0D00 - 0x0DFF	UART 3 – Read FIFO	Read-Only	256 bytes of RX FIFO data
0x0D00 - 0x0DFF	UART 3 – Write FIFO	Write-Only	256 bytes of TX FIFO data
0x0E00 - 0x0FFF	UART 3 – Read FIFO with errors	Read-Only	256 bytes of RX FIFO data + LSR

1.4 Device Configuration Registers

The Device Configuration Registers provide easy programming of general operating parameters to the V354 and for monitoring the status of various functions. These registers control or report on all 4 channel UARTs functions that include interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode control, soft-reset control, and device identification and revision, and others. Table 5 and Table 6 below show these registers in BYTE and DWORD alignment. Each of these registers is described in detail in the following paragraphs.

TABLE 5: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT

ADDRESS [A7:A0]	REGISTER	READ/WRITE COMMENT	RESET STATE
Ox080	INT0 [7:0]	Read-only Interrupt [7:0]	Bits [7:0] = 0x00
Ox081	INT1 [15:8]	Read-only	Bits [7:0] = 0x00
Ox082	INT2 [23:16]	Read-only	Bits [7:0] = 0x00
Ox083	INT3 [31:24]	Read-only	Bits [7:0] = 0x00
Ox084	TIMERCNTL	Read/Write Timer Control	Bits [7:0] = 0x00
Ox085	REGA	Reserved	Bits [7:0] = 0x00
Ox086	TIMERLSB	Read/Write Timer LSB	Bits [7:0]= 0x00
Ox087	TIMERMSB	Read/Write Timer MSB	Bits [7:0]= 0x00
		Individual UART channels can only control the bit pertaining to that channel in the registers at address offset 0x088-0x08B.	
Ox088	8XMODE	Read/Write	Bits [7:0] = 0x00
Ox089	4XMODE	Read/Write	Bits [7:0] = 0x00
Ox08A	RESET	Write-only Self clear bits after executing Reset	Bits [7:0] = 0x00
Ox08B	SLEEP	Read/Write Sleep mode	Bits [7:0]= 0x00
Ox08C	DREV	Read-only Device revision	Bits [7:0] = Current Rev.
Ox08D	DVID	Read-only Device identification	Bits [7:0] = 0x84
Ox08E	REGB	Read/Write EEPROM control	Bits [7:0] = 0x00
Ox08F	MPIOINT[7:0]	Read/Write MPIO[7:0] interrupt mask	Bits [7:0] = 0x00
Ox090	MPIOLVL[7:0]	Read/Write MPIO[7:0] level control	Bits [7:0] = 0x00
Ox091	MPIO3T[7:0]	Read/Write MPIO[7:0] output control	Bits [7:0] = 0x00
Ox092	MPIOINV[7:0]	Read/Write MPIO[7:0] input polarity select	Bits [7:0] = 0x00
Ox093	MPIOSEL[7:0]	Read/Write MPIO[7:0] select	Bits [7:0] = 0xFF
0x094	MPIOOD[7:0]	Read/Write MPIO[7:0] open-drain output control	Bits [7:0] = 0x00
Ox095	MPIOINT[15:8]	Read/Write MPIO[15:8] interrupt mask	Bits [15:8] = 0x00
Ox096	MPIOLVL[15:8]	Read/Write MPIO[15:8] level control	Bits [15:8] = 0x00
Ox097	MPIO3T[15:8]	Read/Write MPIO[15:8] output control	Bits [15:8] = 0x00

TABLE 5: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT

ADDRESS [A7:A0]	REGISTER	READ/WRITE COMMENT	RESET STATE
Ox098	MPIOINV[15:8]	Read/Write MPIO[15:8] input polarity select	Bits [15:8] = 0x00
Ox099	MPIOSEL[15:8]	Read/Write MPIO[15:8] select	Bits [15:8] = 0xFF
0x09A	MPIOOD[15:8]	Read/Write MPIO[15:8] open-drain output control	Bits [15:8] = 0x00
0x09B	Reserved		0x00

TABLE 6: DEVICE CONFIGURATION REGISTERS SHOWN IN DWORD ALIGNMENT

ADDRESS	REGISTER	BYTE 3 [31:24]	BYTE 2 [23:16]	BYTE 1 [15:8]	BYTE 0 [7:0]
0x0080-0x0083	INTERRUPT (read-only)	INT3	INT2	INT1	INT0
0x0084-0x0087	TIMER (read/write)	TIMERMSB	TIMERLSB	Reserved	TIMERCNTL
0x0088-0x008B	ANCILLARY1 (read/write)	SLEEP	RESET	4XMODE	8XMODE
0x008C-0x008F	ANCILLARY2 (read-only)	MPIOINT[7:0]	REGB	DVID	DREV
0x0090-0x0093	MPIO1 (read/write)	MPIOSEL[7:0]	MPIOINV[7:0]	MPIO3T[7:0]	MPIOLVL[7:0]
0x0094-0x0097	MPIO2 (read/write)	MPIO3T[7:0]	MPIOLVL[15:8]	MPIOINT[15:8]	MPIOOD[7:0]
0x0098-0x009B	MPIO3 (read/write)	Reserved	MPIOOD[15:8]	MPIOSEL[15:8]	MPIOINV[15:8]

1.4.1 The Global Interrupt Registers - INT0, INT1, INT2 and INT3

The XR17V354 has a 32-bit wide register [INT0, INT1, INT2 and INT3] to provide interrupt information and supports two interrupt schemes. The first scheme is an 4-bit indicator representing all 4 channels with each bit representing each channel from 0 to 3. This permits the interrupt service routine to quickly determine which UART channels need servicing so that it can go to the appropriate UART channel interrupt service routines. INT0 bit [0] represents the interrupt status for UART channel 0 when its transmitter, receiver, line status, or modem port status requires service. Other bits in the INT0 register provide indication for the other channels with bit [3] representing UART channel 3 respectively.

The second scheme provides detail about the source of the interrupts for each UART channel. All the interrupts are encoded into a 3-bit code. This 3-bit code represents 7 interrupts corresponding to individual UART's transmitter, receiver, line status, modem port status. INT1, INT2 and INT3 registers provide the 24-bit interrupt status for all 4 channels. bits [10:8] representing channel 0 and bits [19:17] representing channel 3 respectively. The rest bits are reserved. All 4 channel interrupts status are available with a single DWORD read operation. This feature allows the host another method to quickly service the interrupts, thus reducing the service interval and host bandwidth requirement.

Note that the interrupts reported in this register is specific to each UART channel. If there is a global interrupt such as the wake-up interrupt, timer/counter interrupt or MPIO interrupt, they would be reported in the 3-bit code for channel 0 in INT1.

GLOBAL INTERRUPT REGISTER (DWORD) [default 0x00-00-00-00]

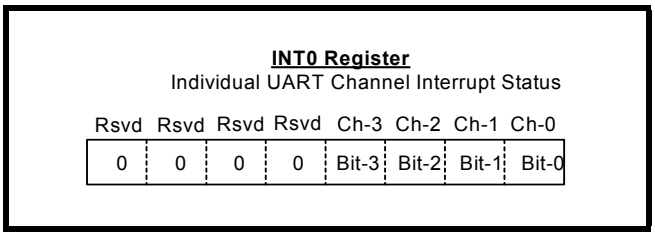
INT3 [31:24]	INT2 [23:16]	INT1 [15:8]	INT0 [7:0]

All bits start up zero. A special interrupt condition is generated by the V354 upon awakening from sleep after all four channels were put to sleep mode earlier. This wake-up interrupt is cleared by a read to the INT0 register. Figure 5 shows the 4-byte interrupt register and its make up.

INT0 [7:0] Channel Interrupt Indicator

Each bit gives an indication of the channel that has requested for service. Bit [0] represents channel 0 and bit [3] indicates channel 3. The upper four bits INT0[7:4] are reserved. Logic 1 indicates the channel N [3:0] has called for service. The interrupt bit clears after reading the appropriate register of the interrupting channel register, see Interrupt Clearing section.

The INT0 register provides individual status for each channel



INT3, INT2 and INT1 [31:8] 3-bit Channel Interrupt Encoding

Each channel's interrupt is encoded into 3 bits for receive, transmit, and status. Bits [10:8] represent channel 0 and go up to channel 3 with bits [19:17]. The 3-bit encoding and their priority order are shown below in **Table 7**. The wake-up interrupt, timer/counter interrupt and MPIO interrupt are only reported in channel 0 of INT1 (bits[10:8]). These interrupts are not reported in any other location.

FIGURE 5. THE GLOBAL INTERRUPT REGISTER, INT0, INT1, INT2 AND INT3

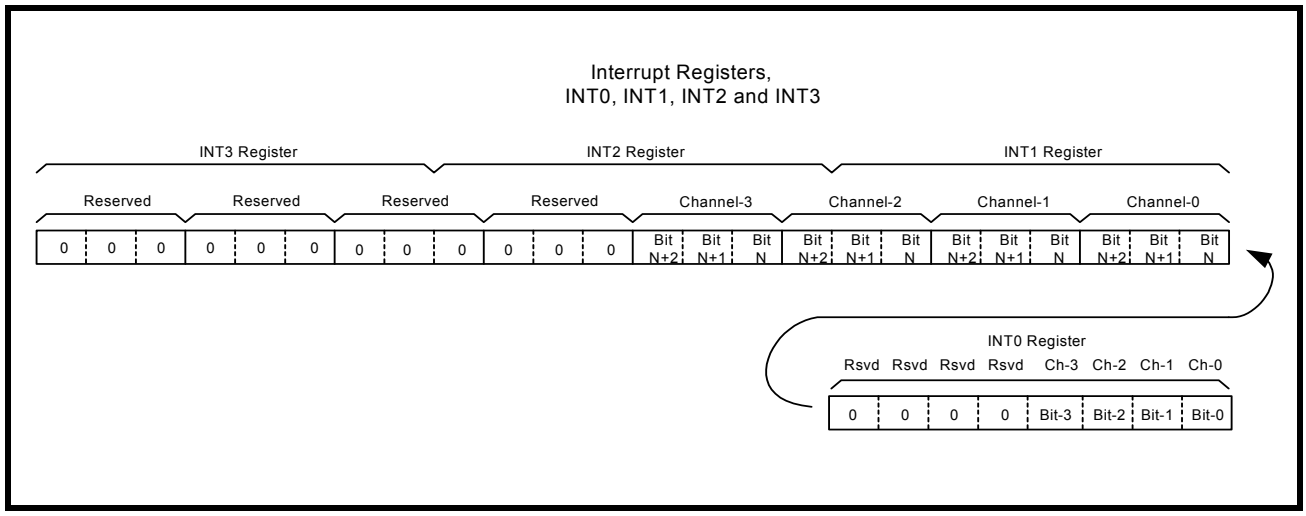


TABLE 7: UART CHANNEL [3:0] INTERRUPT SOURCE ENCODING

PRIORITY	BIT[N+2]	BIT[N+1]	BIT[N]	INTERRUPT SOURCE(S)
x	0	0	0	None or wake-up indicator (wake-up indicator is reported in channel 0 only)
1	0	0	1	RXRDY and RX Line Status (logic OR of LSR[4:1])
2	0	1	0	RXRDY Time-out
3	0	1	1	TXRDY, THR or TSR (auto RS485 mode) empty
4	1	0	0	MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon det. or special char. detected
5	1	0	1	Reserved.
6	1	1	0	MPIO pin(s). Reported in channel 0 only.
7	1	1	1	Timer/Counter. Reported in channel 0 only.

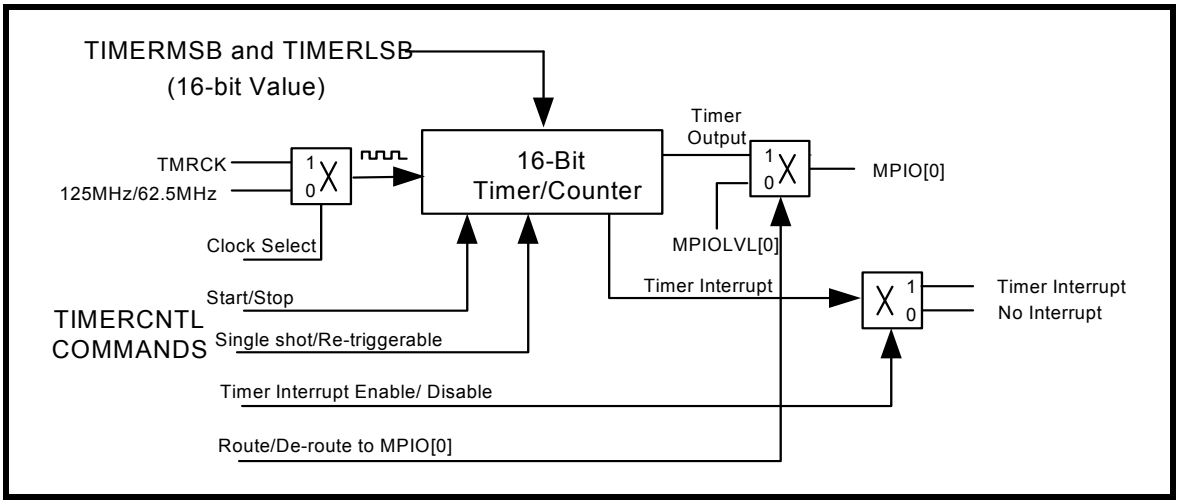
TABLE 8: UART CHANNEL [3:0] INTERRUPT CLEARING

Wake-up Indicator is cleared by reading the INT0 register.
RXRDY and RXRDY Time-out is cleared by reading data in the RX FIFO.
RX Line Status interrupt clears after reading the LSR register that is in the UART channel register set.
TXRDY interrupt clears after reading ISR register that is in the UART channel register set.
Modem Status Register interrupt clears after reading MSR register that is in the UART channel register set.
RTS/CTS or DTR/DSR delta interrupt clears after reading MSR register that is in the UART channel register set.
Xoff/Xon delta and special character detect interrupt clears after reading the ISR register that is in the UART channel register set.
TIMER Time-out interrupt clears after reading the TIMERCNTL register that is in the Device Configuration register set.
MPIO interrupt clears after reading the MPIOLVL register that is in the Device Configuration register set.

1.4.2 General Purpose 16-bit Timer/Counter [TIMERMSB, TIMELSB, TIMER, TIMECNTL] (DEFAULT 0xXX-XX-00-00)

The XR17V354 has a general purpose 16-bit timer/counter. The internal 125 MHz clock (master mode) or 62.5 MHz clock (slave mode) or the external clock at the TMRCK input pin can be selected as the clock source for the timer/counter. The timer can be set to be a single-shot for a one-time event or re-triggerable for a periodic signal. An interrupt may be generated when the timer times out and will show up as a Channel 0 interrupt (see Table 7). It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. The TIMERCNTL register provides the Timer commands such as start/stop, as shown in Table 9 below. The time-out output of the Timer can also be optionally routed to the MPIO[0] pin. The block diagram of the Timer/Counter circuit is shown below:

FIGURE 6. TIMER/COUNTER CIRCUIT

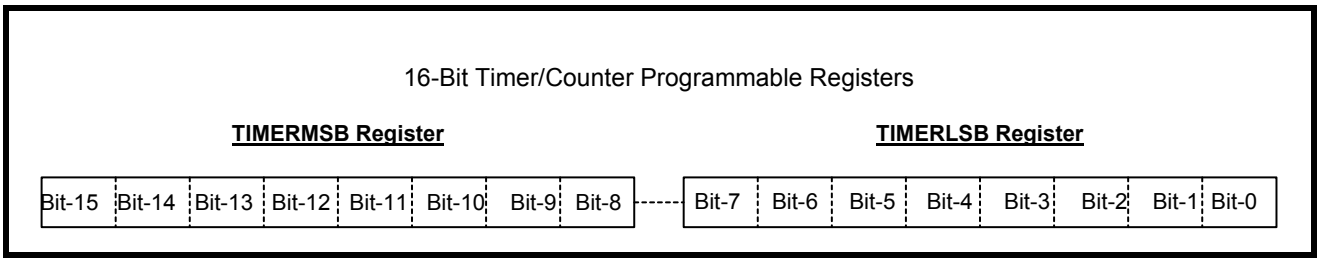


TIMERMSB [31:24] and TIMERLSB [23:16] registers

The concatenation of the 8-bit registers TIMERMSB and TIMERLSB forms a 16-bit value which decides the time-out period of the Timer, per the following equation:

Timer output frequency = Timer input clock / 16-bit Timer value

The least-significant bit of the timer is being bit [0] of the TIMERLSB with most-significant-bit being bit [7] in TIMERMSB. Notice that these registers do not hold the current counter value when read. Default value is zero (timer disabled) upon powerup and reset. The 'Reset Timer' command does not have any effect on this register.



REGA [15:8] Register

Reserved.

TIMERCNTL [7:0] Register

The bits [3:0] of this register are used to issue commands. The commands are self-clearing, so reading this register does not show the last written command. Reading this register returns a value of 0x01 when the Timer interrupt is enabled and there is a pending Timer interrupt. It returns a value of 0x00 at all other times. The default settings of the Timer, upon power-up, a hardware reset or upon the issue of a 'Timer Reset' command are:

- Timer Interrupt Disabled
- Re-triggerable mode selected
- Internal 125 MHz clock (master) or 62.5 MHz clock (slave) selected as clock source
- Timer output not routed to MPIO[0]
- Timer stopped

TABLE 9: TIMER CONTROL REGISTERS

TIMERCNTL [7:4]	Reserved
TIMERCNTL [3:0]	These bits are used to invoke a series of commands that control the function of the Timer/Counter. The commands 1100 to 1111 are reserved. 0001: Enable Timer Interrupt 0010: Disable Timer Interrupt 0011: Select One-shot mode 0100: Select Re-triggerable mode 0101: Select Internal 125 MHz clock (master) or 62.5 MHz clock (slave) as clock input for the Timer 0110: Select External Clock input through the TMRCK pin for the Timer 0111: Route Timer output to MPIO[0] pin 1000: De-route Timer output from MPIO[0] 1001: Start Timer 1010: Stop Timer 1011: Reset Timer

TIMER OPERATION

The following paragraphs describe the operation of the 16-bit Timer/Counter. The following conventions will be used in this discussion:

- 'N' is the 16-bit value programmed in the TIMER MSB, LSB registers
- P +Q = N, where 'P' and 'Q' are approximately half of 'N'.
- If N is even, P = Q = N/2.
- If N is odd, P = (N – 1)/2 and Q = (N + 1)/2.
- 'N' can take any value from 0x0002 to 0xFFFF.

Timer Operation in One-Shot Mode:

In the one-shot mode, the Timer output will stay HIGH when started (default state) and will continue to stay HIGH until it times out (reaches the terminal count of 'N' clocks), at which time it will become LOW and stay LOW. If the Timer is re-started before the Timer times out, the counter is reset and the Timer will wait for another time-out period before setting its output LOW (See **Figure 7**). If the Timer times out, re-starting the Timer does not have any effect and a 'Stop Timer' command needs to be issued first which will set the Timer output to its default HIGH state. The Timer must be programmed while it is stopped since the following operations are blocked after the Timer has been started:

- Any write to TIMER MSB, LSB registers
- Issue of any command other than 'Start Timer', 'Stop Timer' and 'Reset Timer'

Timer Operation in Re-triggerable Mode:

In the re-triggerable mode, when the Timer is started, the Timer output will stay HIGH until it reaches half of the terminal count N (= P clocks) and toggle LOW and stay LOW for a similar amount of time (Q clocks). The above step will keep repeating until the Timer is stopped at which time the output will become HIGH (default state). See **Figure 7**. Also, after the Timer is started, re-starting the Timer does not have any effect in re-triggerable mode. The Timer must be programmed while it is stopped since the following operations are blocked when the Timer is running:

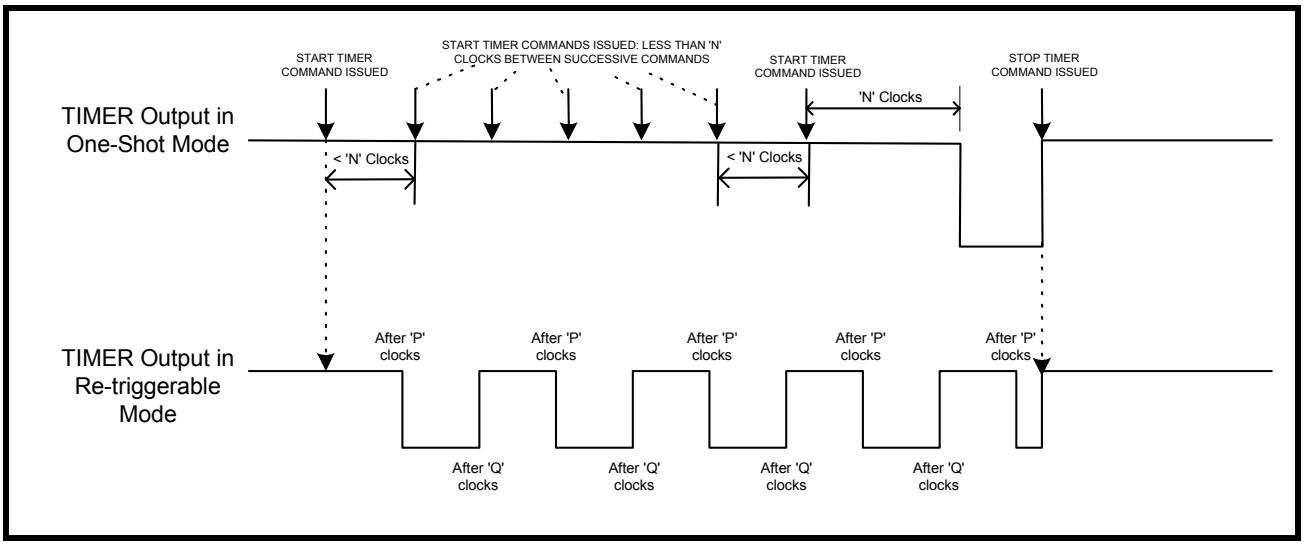
- Any write to TIMER MSB, LSB registers
- Issue of any command other than 'Stop Timer' and 'Reset Timer' ('Start Timer' is not allowed)

Routing the Timer Output to MPIO[0] Pin:

MPIO[0] pin is by default (on power up or reset, for example) an input. However, whenever the Timer output is routed to MPIO[0] pin,

- MPIO[0] will be automatically selected as an output
- MPIO[0] will become HIGH (the default state of Timer output)
- All MPIO control registers (MPIOLVL, MPIOSEL etc) lose control over MPIO[0] and get the control back only when the Timer output is de-routed from MPIO[0].

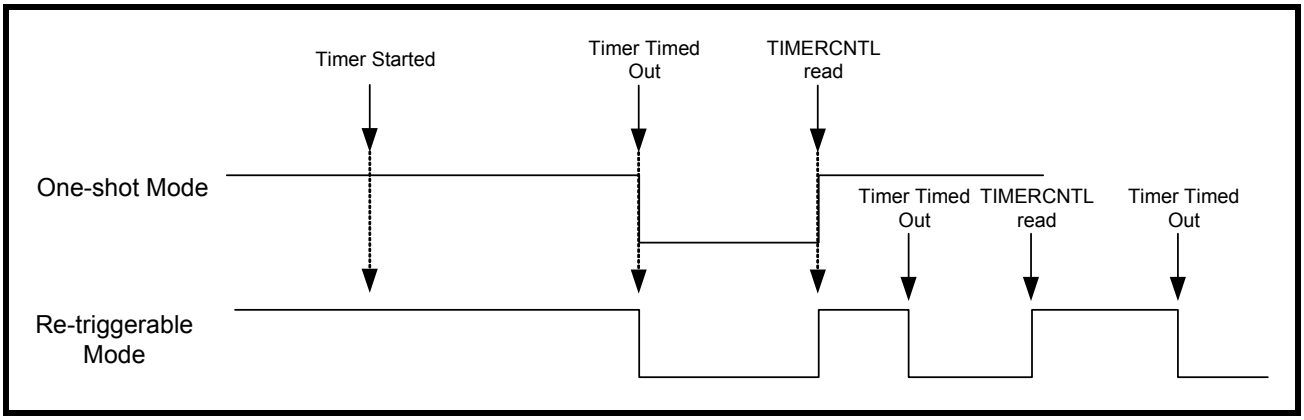
FIGURE 7. TIMER OUTPUT IN ONE-SHOT AND RE-TRIGGERABLE MODES



Timer Interrupt

In the one-shot mode, the Timer will issue an interrupt upon timing out which is 'N' clocks after the Timer is started. In the re-triggerable mode, the Timer will keep issuing an interrupt every 'N' clocks which is on every rising edge of the Timer output. The Timer interrupt can be cleared by reading the TIMERCNTL register or when a Timer Reset command is issued which brings the Timer back to its default settings. The TIMERCNTL will read a value of 0x01 when the Timer interrupt is enabled and there is a pending interrupt. It reads a value of 0x00 at all other times. Stopping the Timer does not clear the interrupt and neither does subsequent re-starting.

FIGURE 8. INTERRUPT OUTPUT (ACTIVE LOW) IN ONE-SHOT AND RE-TRIGGERABLE MODES



1.4.3 8XMODE [7:0] (default 0x00)

Each bit selects 8X or 16X sampling rate for that UART channel. The 8XMODE register is accessible from the Device Configuration Registers in all UART channels but the UART channel can only control the bit for that channel. For example, bit [0] is for channel 0 and can only be controlled by channel 0. All other bits are read-only in channel 0. Logic 0 (default) selects normal 16X sampling (and 4XMODE = 0x00) with logic one selects

8X sampling rate. Transmit and receive data rates will double by selecting 8X. If using the 4XMODE, the corresponding bit in this register should be logic 0

8XMODE Register
Individual UART Channel 8X Clock Mode Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	0	0	Ch-3	Ch-2	Ch-1	Ch-0

1.4.4 4XMODE [15:8] (default 0x00)

Each bit selects 4X or 16X sampling rate for that UART channel. The 4XMODE register is accessible from the Device Configuration Registers in all UART channels but the UART channel can only control the bit for that channel. For example, bit [0] is channel 0 and can only be controlled by channel 0. All other bits are read-only in channel 0. Logic 0 (default) selects normal 16X sampling (and 8XMODE = 0x00) with logic one selects 4X sampling rate. Transmit and receive data rates will quadruple by selecting 4X. If using the 8XMODE, the corresponding bit in this register should be logic 0

4XMODE Register
Individual UART Channel 4X Clock Mode Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	0	0	Ch-3	Ch-2	Ch-1	Ch-0

RESET [23:16] (default 0x00)

The 8-bit RESET register provides the software with the ability to reset the UART(s) when there is a need. The RESET register is accessible from the Device Configuration Registers in all UART channels but the UART channel can only control the bit for that channel. For example, writing 0xFF to the RESET register in channel 0 will only reset channel 0. Each bit is self-clearing after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition, see **Table 21** for details. .

RESET Register
Individual UART Channel Reset Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	0	0	Ch-3	Ch-2	Ch-1	Ch-0

1.4.5 SLEEP [31:24] (default 0x00)

SLEEP Register
Individual UART Channel Sleep Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	0	0	Ch-3	Ch-2	Ch-1	Ch-0