GENERAL DESCRIPTION

The XR19L210 (L210) is a highly integrated device that combines a full-featured single channel Universal Asynchronous Receiver and Transmitter (UART) and an RS-232 transceiver. The L210 is designed to operate with a single 3.3V or 5V power supply. The L210 is fully compliant with EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply. The device operates at 250 Kbps data rate with worst case 3K ohms load. Both RS-232 driver outputs and receiver inputs can operate in harsh electrical environments of +/-15V without damage and can survive multiple +/-15kV ESD on the RS-232 lines, while maintaining RS-232 output levels.

The L210 operates in four different modes: Awake, Partial Sleep, Full Sleep and Power-Save. Each mode can be invoked via hardware and/or software. In the Awake mode, all functions are active. In the Partial Sleep mode, the internal crystal oscillator or charge pump is turned off. In Full Sleep mode, the internal crystal oscillator and the charge pump is shut down. In the Power-Save mode, the core logic is isolated from the control signals (chip select, read/write strobes, address and data bus lines). All the RS-232 receivers remain active in any of these four modes.

APPLICATIONS

- Battery-Powered Equipment
- Handheld and Mobile Devices
- Handheld Terminals
- Industrial Peripheral Interfaces
- Point-of-Sale (POS) Systems

FEATURES

- Meets true EIA/TIA-232-F Standards from a 3.0 V to 5.5V operation
- Up to 250 Kbps data transmission rate
- 45us sleep mode exit (charge pump to full power)
- ESD protection for RS-232 I/O pins at
  - +/-15kV - Human Body Model
  - +/-15kV - IEC 61000-4-2, Air-Gap Discharge
  - +/- 8kV - IEC 61000-4-2, Contact Discharge
- Software compatible with industry standard 16550 UART
- Intel/Motorola bus select
- Half-modem interface (TXD, RXD, RTS, CTS)
- Sleep and Power-save modes to conserve battery power
- Wake-up interrupt upon exiting low power modes

FIGURE 1. BLOCK DIAGRAM

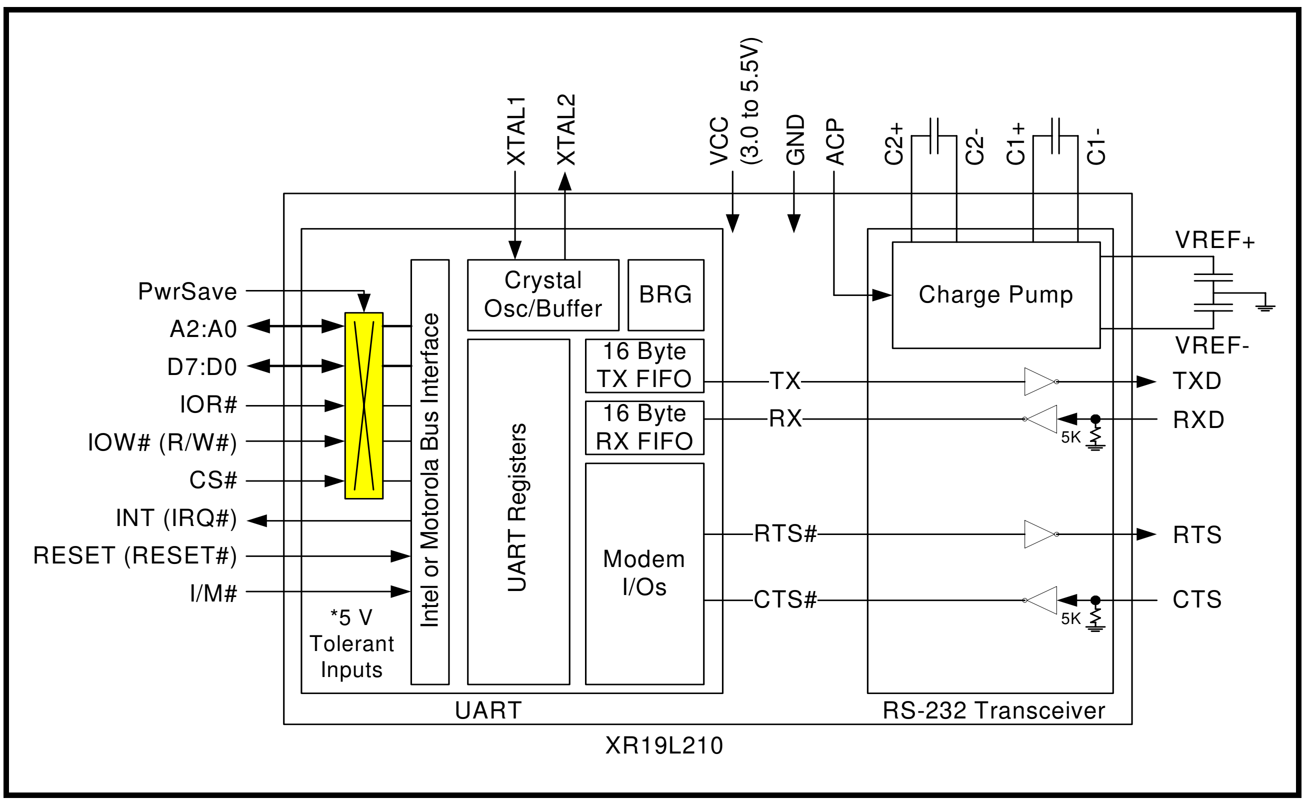
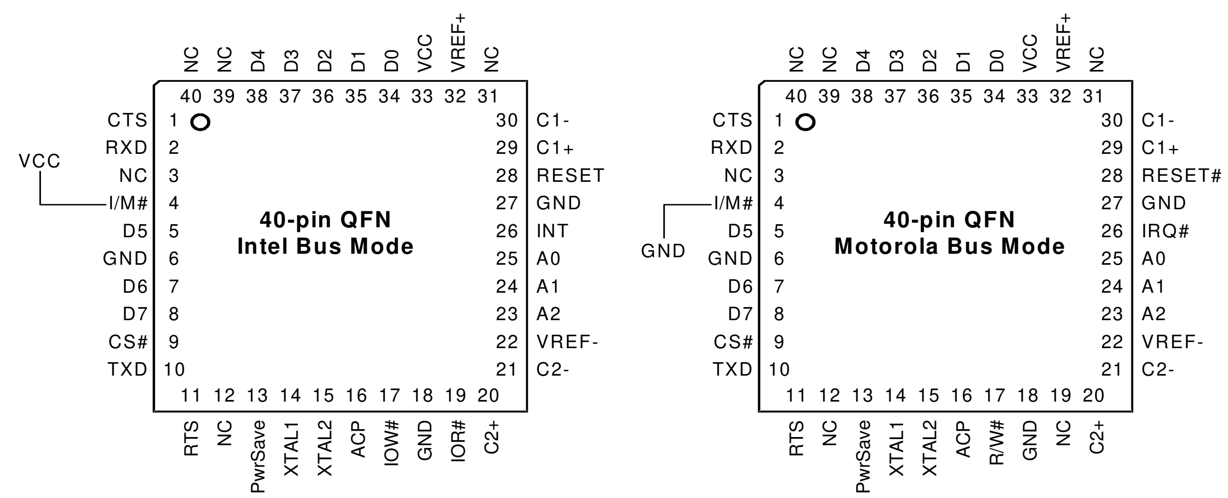


FIGURE 2. PIN OUT OF THE DEVICE



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR19L210IL40	40-QFN	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Descriptions

NAME	40-QFN PIN#	TYPE	DESCRIPTION
DATA BUS INTERFACE (CMOS/TTL Voltage Levels)			
A2 A1 A0	23 24 25	I	Address bus lines [2:0]. These 3 address lines select one of the internal registers in the UART during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	8 7 5 38 37 36 35 34	I/O	Data bus lines [7:0] (bidirectional).
IOR# (NC)	19	I	When I/M# pin is HIGH, the Intel bus interface is selected and this input becomes read strobe (active LOW). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When I/M# pin is LOW, the Motorola bus interface is selected and this input is not used.
IOW# (R/W#)	17	I	When I/M# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active LOW). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When I/M# pin is LOW, the Motorola bus interface is selected and this input becomes read (HIGH) and write (LOW) signal.
CS#	9	I	This input is chip select (active LOW) to enable the device.
INT (IRQ#)	26	O (OD)	When I/M# pin is HIGH, it selects Intel bus interface and this output become the active HIGH device interrupt output. This output is enabled through the software setting of MCR[3]: set to the active mode when MCR[3] is set to a logic 1, and set to the three state mode when MCR[3] is set to a logic 0. See MCR[3]. When I/M# pin is LOW, it selects Motorola bus interface and this output becomes the active LOW, open-drain interrupt output. An external pull-up resistor is required for proper operation. MCR[3] must be set to a logic 0 for proper operation of the interrupt.
MODEM OR SERIAL I/O INTERFACE (EIA-232/RS-232 Voltage Levels)			
TXD	10	O	UART Transmit Data. The TX signal will be LOW (< -5V) during reset or idle (no data).
RXD	2	I	UART Receive Data. The RX data input must idle LOW (< -3V).
RTS	11	O	UART Request-to-Send or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1] and IER[6].
CTS	1	I	UART Clear-to-Send or general purpose input. It can be used for auto CTS flow control, see EFR[7], MSR[4] and IER[7]. This input has an internal pull-down resistor and can be left unconnected when not used.
ANCILLARY SIGNALS (CMOS/TTL Voltage Levels)			
XTAL1	14	I	Crystal or external clock input. This input is not 5V tolerant.
XTAL2	15	O	Crystal or buffered clock output. This output may be use to drive a clock buffer which can drive other device(s).

Pin Descriptions

NAME	40-QFN PIN#	TYPE	DESCRIPTION
PwrSave	13	I	Power-Save (active high). This feature isolates the L210's data bus interface from the host preventing other bus activities that cause higher power drain during sleep mode. See Sleep Mode with Auto Wake-up and Power-Save Feature section for details.
ACP	16	I	Autosleep for Charge Pump (active HIGH). When this pin is HIGH, the charge pump is shut off if the L210 is already in partial sleep mode, i.e. the crystal oscillator is stopped.
I/M#	4	I	Intel or Motorola Bus Select. When I/M# pin is HIGH, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When I/M# pin is LOW, 68 or Motorola mode, the device will operate in the Motorola bus type of interface.
RESET (RESET#)	28	I	When I/M# pin is HIGH for Intel bus interface, this input becomes RESET (active high). When I/M# pin is LOW for Motorola bus interface, this input becomes RESET# (active low). A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs of the UART. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (see Table 11).
C2+ C2-	20 21	-	Charge pump capacitors. As shown in Figure 1, a 0.1 uF capacitor should be placed between these 2 pins.
C1+ C1-	29 30	-	Charge pump capacitors. As shown in Figure 1, a 0.1 uF capacitor should be placed between these 2 pins.
VREF+	32	Pwr	+5.0V generated by the charge pump.
VREF-	22	Pwr	-5.0V generated by the charge pump.
VCC	33	Pwr	3.0V to 5.5V power supply. All CMOS/TTL input pins, except XTAL1, are 5V tolerant.
GND	6, 18, 27	Pwr	Power supply common, ground.
-	PAD	Pwr	The center pad on the backside of the 40-QFN package is metallic and is not electrically connected to anything inside the device. It must be soldered on to the PCB and may be optionally connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.
NC	3, 12, 31, 39, 40	-	No Connect. Note that in Motorola mode, the IOR# pin also becomes an NC pin.

NOTE: *Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain. For CMOS/TTL Voltage levels, 'LOW' indicates a voltage in the range 0V to VIL and 'HIGH" indicates a voltage in the range VIH to VCC. For RS-232 input voltage levels, 'LOW' is any voltage < -3V and 'HIGH' is any voltage > 3V. For RS-232 output voltage levels, 'LOW' is any voltage < -5V and 'HIGH' is any voltage > 5V.*

1.0 PRODUCT DESCRIPTION

The XR19L210 interface converter consists of a full-functional UART with 16 bytes of transmit and receive FIFO, a charge pump, two RS-232 drivers, two RS-232 receivers, and a sleep/PowerSave mode circuitry. It operates from a single +3V to 5.5V supply at 250Kbps data rate, while meeting all EIA RS-232F specifications. Its feature set is fully compatible to the XR16L580 device. Unlike the XR16L580, the modem signals are not CMOS/TTL level, but conform to EIA/TIA 232 or RS-232 voltage levels. The configuration registers set is 16550 UART compatible for control, status and data transfer. Also, the L210 has 16-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, transmit and receive FIFO trigger levels, and a programmable baud rate generator with a prescaler of divide by 1 or 4. Additionally, the L210 includes the ACP pin which the user can shut down the charge pump for the RS-232 drivers when the L210 is already in sleep mode. The Power-Save feature further isolates the databus interface to further reduce power consumption in the sleep mode. The L210 is fabricated using an advanced CMOS process.

Enhanced Features

The L210 UART provides a solution that supports 16 bytes of transmit and receive FIFO memory. The L210 is designed to work with low supply voltage and high performance data communication systems that require fast data processing time. Increased performance is realized in the L210 by the transmit and receive FIFOs, FIFO trigger level controls and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the L210 provides the Power-Save mode that drastically reduces the power consumption when the device is not used. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

Intel or Motorola Data Bus Interface

The L210 provides a host interface that supports Intel or Motorola microprocessor (CPU) data bus interface. The Intel bus compatible interface allows direct interconnect to Intel compatible type of CPUs using IOR#, IOW# and CS# inputs for data bus operation. The Motorola bus compatible interface instead uses the R/W# and CS# signals for data bus transactions. See pin description section for details on all the control signals. The Intel and Motorola bus interface selection is made through the pin, I/M#.

Data Rate

The L210 is capable of operation up to 250Kbps data rate using the 16X internal sampling clock rate. The UART section can operate at much higher speeds, but the speed of the RS-232 transceiver is limited to 250Kbps beyond which the L210 cannot comply with the EIA/TIA-232 electrical characteristics. The device can operate either with a crystal on pins XTAL1 and XTAL2, or external clock source on XTAL1 pin.

Internal Enhanced Register Sets

The L210 UART has a set of enhanced registers providing control and monitoring functions. Interrupt enable/disable and status, FIFO enable/disable, selectable TX and RX FIFO trigger levels, automatic hardware/software flow control enable/disable, programmable baud rates, modem interface controls and status, sleep mode and Power-Save mode are all standard features. Following a power on reset or an external reset (and operating in 16 or Intel Mode), the registers defaults to the reset condition and is compatible with the XR16L580.

RS-232 Interface

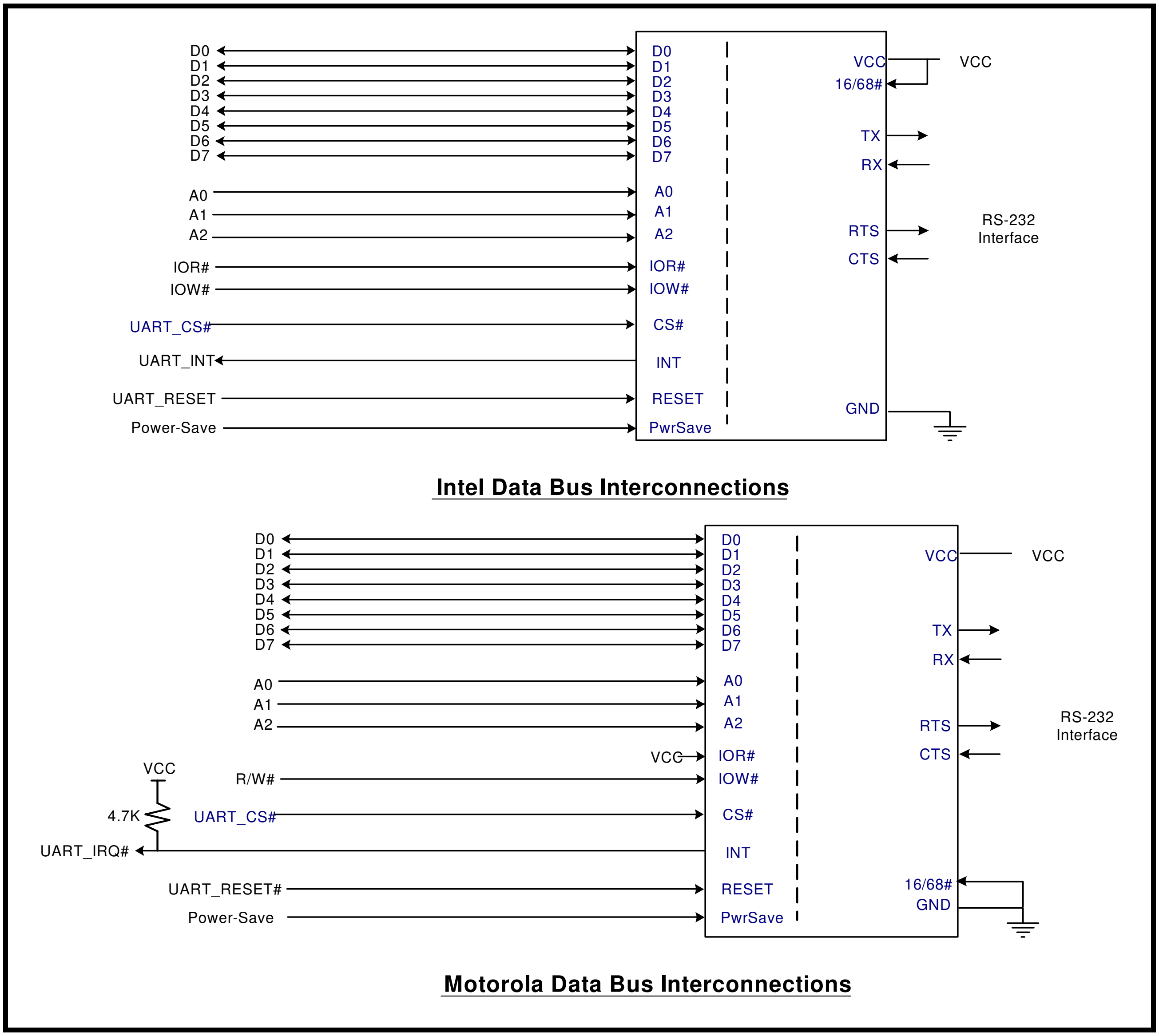
The L210 includes RS-232 drivers/receivers for the TXD, RXD, RTS and CTS signals (For a device with the complete modem interface, please see the XR19L220). This feature eliminates the need for an external RS-232 transceiver. The charge pump provides output voltages of +5V and -5V for its drivers over the 3.0V to 5.5V VCC supply voltage. The serial outputs TX and RTS swing between -5V (inactive) and 5V (active) RS-232 voltage levels. The serial inputs RX and CTS are RS-232 receivers and can take any voltage swing from -15V to +15V. The receivers are always active, even in Full Sleep and Power-Save modes. The RS-232 drivers guarantee a data rate of 250Kbps even when fully loaded with 3Kohm in parallel with 1000pF load. Also, the slew rate of the driver output is internally limited to a maximum of 30V/us in order to meet the EIA-232F standard.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The L210 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# or R/W# inputs. A typical data bus interconnection for Intel and Motorola mode is shown in **Figure 3**.

FIGURE 3. XR19L210 TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS



2.2 5-Volt Tolerant Inputs

The CMOS/TTL level inputs of the L210 can accept up to 5V inputs when operating at 3.3V. Note that the XTAL1 pin is not 5V tolerant when an external clock supply is used.

2.3 Device Hardware Reset

The RESET or RESET# input resets the internal registers and the serial interface outputs in both channels to their default state (see **Table 11**). An active pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Device Identification and Revision

The XR19L210 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x01 to indicate functional compatibility with XR16L580 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 Internal Registers

The L210 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers, (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and an user accessible Scratchpad register (SPR).

Beyond the general 16C550 features and capabilities, the L210 offers enhanced feature registers just like the XR16L580, namely, EFR, Xon1, Xoff 1, Xon1 and Xoff2 that provide automatic RTS and CTS hardware flow control and Xon/Xoff software flow control. All the register functions are discussed in full detail later in **"Section 3.0, UART INTERNAL REGISTERS" on page 18**.

2.6 DMA Mode

The DMA Mode (a legacy term) refers to data block transfer operation. The DMA mode affects the state of the RXRDY# and TXRDY# output pins available in the original 16C550. These pins are not available in the XR19L210. The DMA Enable bit (FCR bit-3) does not have any function in this device and can be a '0' or a '1'.

2.7 INT (IRQ#) Output

The interrupt output changes according to the operating mode and enhanced features setup. **Table 1** and **Table 2** below summarize the operating behavior for the transmitter and receiver in the Intel and Motorola modes. Also see Figures 18 through 21.

TABLE 1: INT (IRQ#) PIN OPERATION FOR TRANSMITTER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (I/M# = 1)	0 = one byte in THR 1 = THR empty	0 = FIFO above trigger level 1 = FIFO below trigger level or FIFO empty
IRQ# Pin (I/M# = 0)	1 = one byte in THR 0 = THR empty	1 = FIFO above trigger level 0 = FIFO below trigger level or FIFO empty

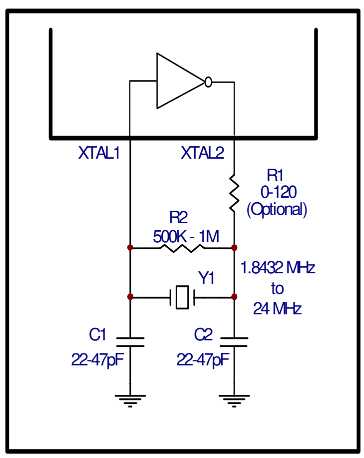
TABLE 2: INT (IRQ#) PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (I/M# = 1)	0 = no data 1 = 1 byte	0 = FIFO below trigger level 1 = FIFO above trigger level
IRQ# Pin (I/M# = 0)	1 = no data 0 = 1 byte	1 = FIFO below trigger level 0 = FIFO above trigger level

2.8 Crystal or External Clock Input

The L210 includes an on-chip oscillator (XTAL1 and XTAL2) to generate a clock when a crystal is connected between the XTAL1 and XTAL2 pins of the device. Alternatively, an external clock can be supplied through the XTAL1 pin. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock input and XTAL2 pin is the bufferred output which can be used as a clock signal for other devices in the system. Please note that the input XTAL1 is not 5V tolerant and therefore, the maximum voltage at the pin should be VCC when an external clock is supplied. For programming details, see "Programmable Baud Rate Generator."

FIGURE 4. TYPICAL CRYSTAL CONNECTIONS

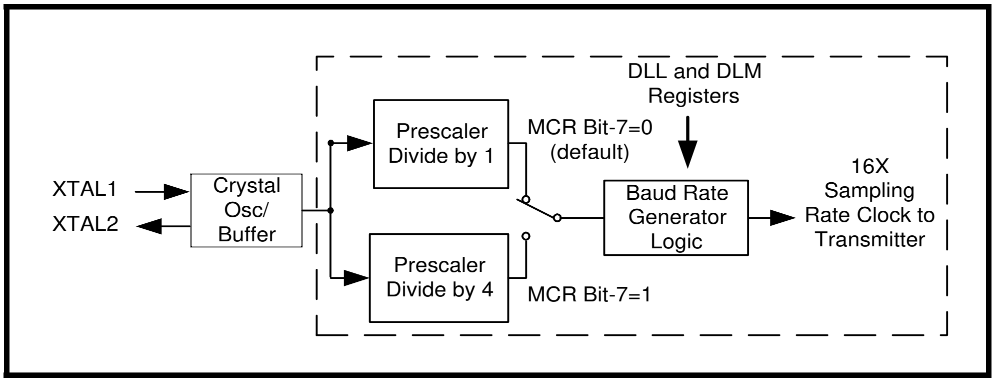


The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins. When VCC = 5V, the on-chip oscillator can operate with a crystal whose frequency is not greater than 24 MHz. On the other hand, the L210 can accept an external clock of up to 50MHz at XTAL1 pin also. Although the L210 can accept an exteran clock of up to 50MHz, the maximum data rate supported by the RS-232 drivers is 250Kbps. For further reading on the oscillator circuit please see the Application Note DAN108 on the EXAR web site at **http://www.exar.com.**

2.9 Programmable Baud Rate Generator

The L210 UART has its own Baud Rate Generator (BRG) with a prescaler. The prescaler is controlled by a software bit (bit-7) in the MCR register. This bit selects the prescaler to divide the input crystal or external clock by a factor of 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor (via DLL and DLM registers) between 1 and (2^{16} -1) to obtain a 16X sampling rate clock of the serial data rate. The sampling rate clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor defaults to the maximum baud rate (DLL = 0x01 and DLM = 0x00) upon power up.

FIGURE 5. BAUD RATE GENERATOR AND PRESCALER



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 3 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X sampling rate clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 3: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0 (DEFAULT)	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0

2.10 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 16 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

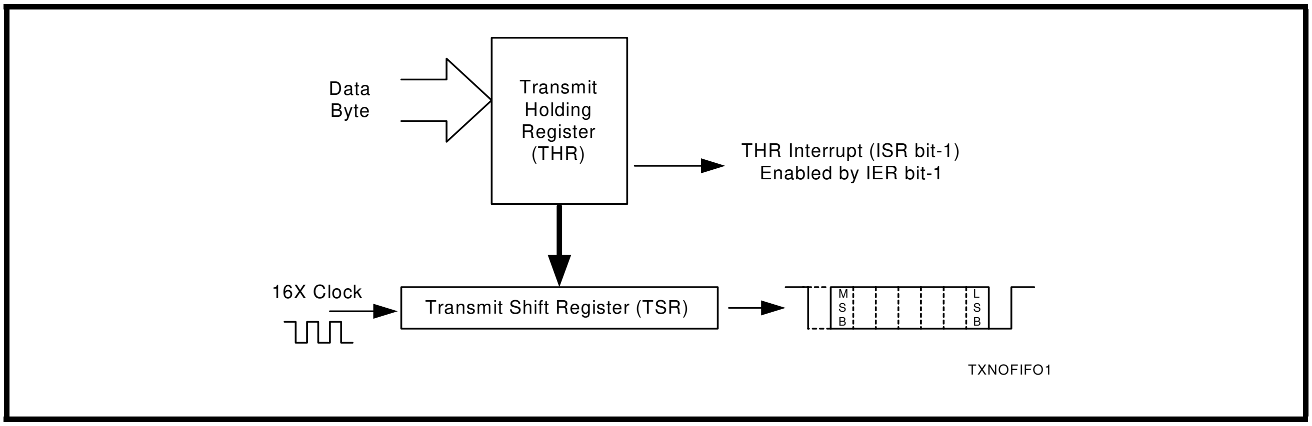
2.10.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 16 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.10.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

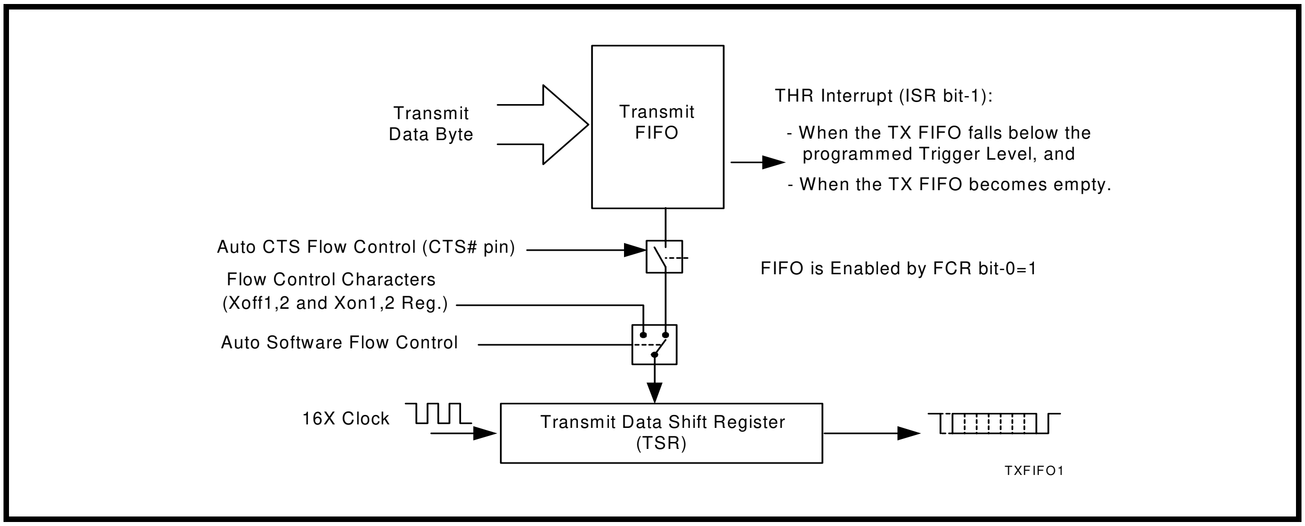
FIGURE 6. TRANSMITTER OPERATION IN NON-FIFO MODE



2.10.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 16 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The Transmitter Empty Flag (LSR bit-6) is set when both the TSR and the FIFO become empty.

FIGURE 7. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.11 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 16 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. On the rising edge of RXD (or falling edge of RX) of a start or a false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still LOW it is validated as a start bit. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Each of the data, parity and stop bits is sampled at the middle of the bit to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.11.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 16 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 8. RECEIVER OPERATION IN NON-FIFO MODE

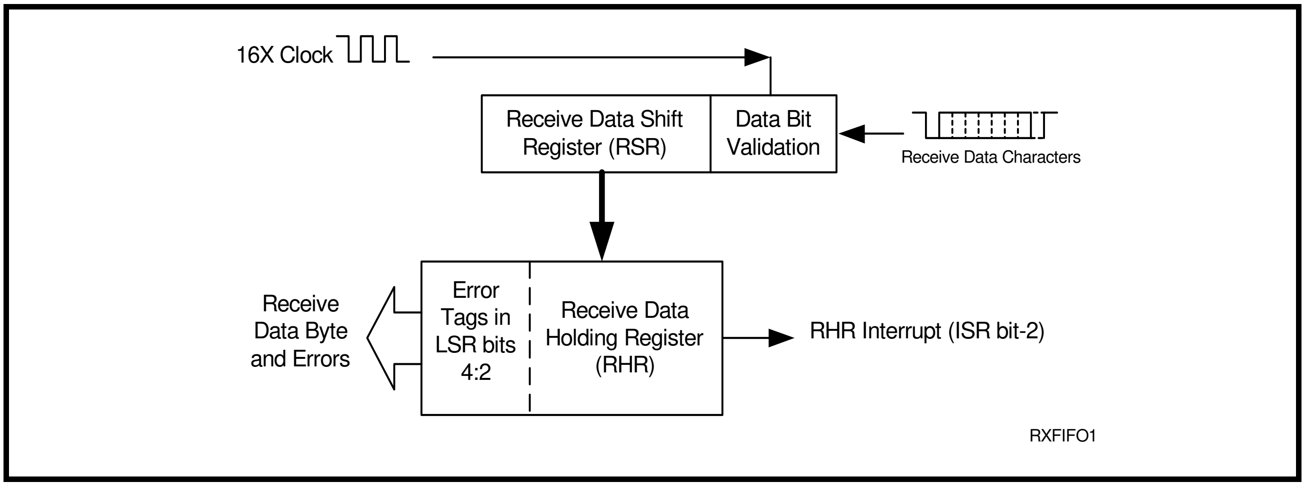
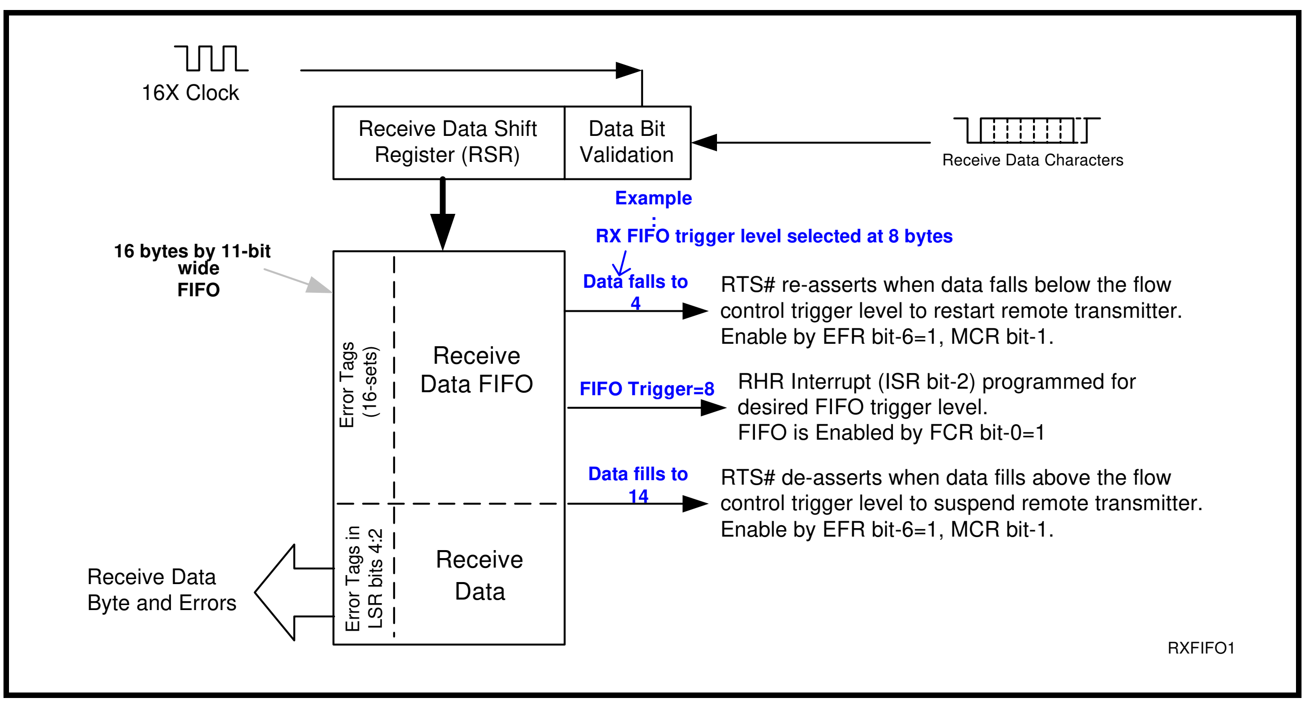


FIGURE 9. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.12 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 10**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.13 Auto RTS Hysteresis

The L210 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the ST16C550 UART. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS pin will not be de-asserted until the receive FIFO reaches one trigger level above the programmed trigger level in the trigger table (**Table 8**). The RTS pin will be re-asserted after the RX FIFO is unloaded to one trigger level lower than the programmed trigger level. This is described in **Figure 10**. Under the above described conditions, the L210 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS output pin is asserted.

2.14 Auto CTS Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 10**):

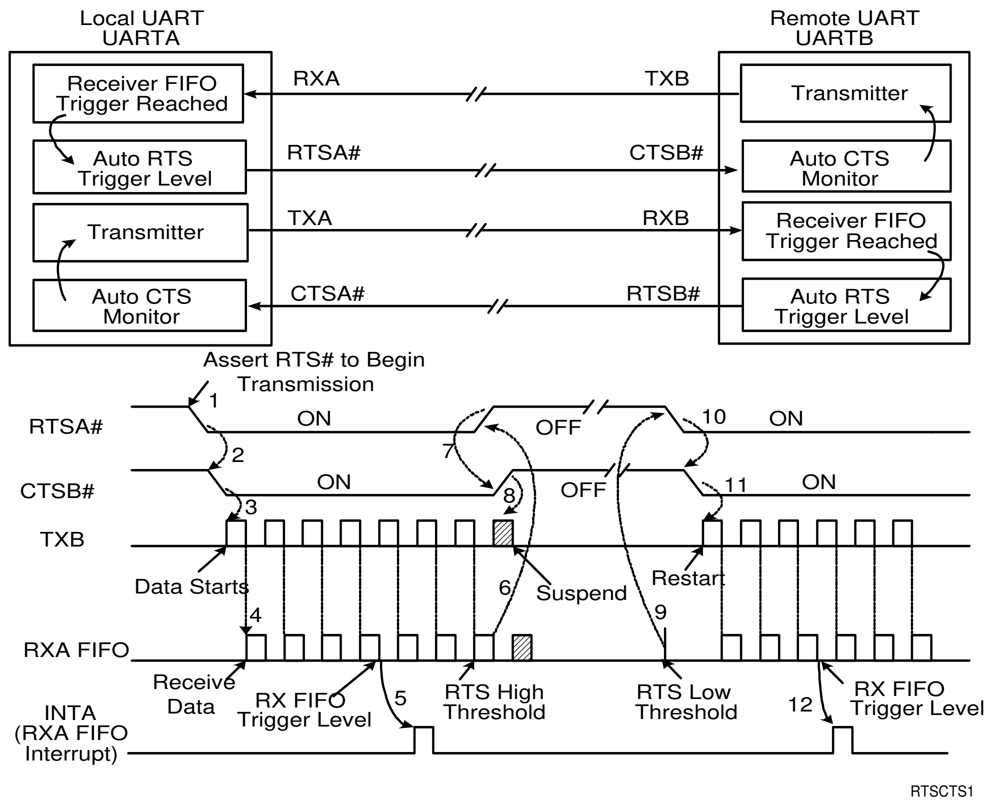
- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS pin is de-asserted: ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS input is re-asserted, indicating more data may be sent.

FIGURE 10. AUTO RTS AND CTS FLOW CONTROL OPERATION

The signals shown in this figure are the signals at the UART and not at the RS-232 transceiver.



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.15 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 10), the L210 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the L210 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the L210 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the L210 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/ Xoff characters (See Table 10) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the L210 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the L210 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The L210 sends the Xoff character(s) two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the L210 will transmit the programmed Xon character(s) as soon as receive FIFO is less than one trigger level below the programmed trigger level (see Table 8). **The table below describes this**.

TABLE 4: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
1	1	1*	0
4	4	4*	1
8	8	8*	4
14	14	14*	8

* *After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 8-bit word length, no parity and 1 stop bit setting.*

2.16 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The L210 compares each incoming receive character with the programmed Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

2.17 Sleep Modes and Power-Save Feature with Wake-Up Interrupt

There are three levels of power management integrated in the L210. The device is low power with low operational and standby supply currents. In the Partial Sleep mode, the internal oscillator of the UART or charge pump of the RS-232 transceiver is turned off to reduce the power consumption. In the Full Sleep mode, both the oscillator and the charge pump are turned off. The Power-save mode provides additional power saving by isolating the UART address, data and control signals during Sleep mode to minimize the power consumption.

2.17.1 Partial Sleep Mode

There are two different partial sleep modes. In the first mode, the UART is in sleep mode and the RS-232 transceiver is active. In the other mode, the UART is active but the charge pump of the RS-232 transceiver is turned off.

2.17.1.1 UART in sleep mode, RS-232 transceiver active

If the ACP pin is LOW, then the charge pump for the RS-232 transceiver will always be active. But the UART portion in the L210 can still enter sleep mode if all of these conditions are satisfied:

- no interrupts pending (ISR bit-0 = 1)
- the 16-bit divisor programmed in DLM and DLL registers is a non-zero value
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RXD input pin is idling LOW

The L210 stops its crystal oscillator to conserve power in this mode. The user can check the XTAL2 pin for no clock output as an indication that the device has entered the partial sleep mode.

The UART portion in the L210 resumes normal operation or active mode by any of the following:

- a receive data start bit transition on the RXD input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: i.e., any of the MSR bits 0-3 shows a '1'

The UART portion in the L210 will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the UART portion of the L210 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The UART portion of the L210 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

2.17.1.2 UART active, charge pump of RS-232 transceiver shut down

If the ACP pin is HIGH and the UART portion of the L210 is not in sleep mode, then the charge pump will automatically shut down to conserve power if the following conditions are true:

- no activity on the TXD output signal
- modem input signals (RX, CTS) are LOW
- modem inputs have been idle for approximately 30 seconds

When these conditions are satisfied, the L210 shuts down the charge pump and tri-states the RS-232 drivers to conserve power. In this mode, the RS-232 receivers are fully active and the internal registers of the L210 can be accessed. The time for the charge pump to resume normal operation after exiting the sleep mode is typically 45µs. It will wake up by any of the following:

- a receive data start bit transition on the RXD input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a LOW to HIGH transition on the CTS input

Because the receivers are fully active when the charge pump is turned off, any data received will be transferred to/from the UART without any issues.

2.17.2 Full Sleep Mode

In full sleep mode, the UART will be in sleep mode and the charge pump of the RS-232 transceiver will be shut down. The L210 enters the full sleep mode if the following conditions are satisfied:

- the UART portion of the L210 is already in sleep mode (no output on XTAL2)
- the ACP (Autosleep for Charge Pump) pin is HIGH

When these conditions are satisfied, both the UART and the RS-232 transceiver will be in the sleep mode. In this mode, the RS-232 receivers are fully active and the internal registers of the L210 can be accessed. The L210 exits the full sleep mode if either the ACP pin becomes LOW or the internal oscillator starts up. The time for the charge pump to resume normal operation after exiting the full sleep mode is typically 45µs.

2.17.3 Power-Save Feature

This mode is in addition to the sleep mode and in this mode, the core logic of the L210 is isolated from the CPU interface. If the address lines, data bus lines, IOW#, IOR# and CS# remain steady when the L210 is in full sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 32. However, if the input lines are floating or are toggling while the L210 is in sleep mode, the current can be up to 100 times more. If not using the Power-Save feature, an external buffer would be required to keep the address and data bus lines from toggling or floating to achieve the low current. But if the Power-Save feature is enabled (PwrSave pin connected to VCC), this will eliminate the need for an external buffer by internally isolating the address, data and control signals from other bus activities that could cause wasteful power drain (see Figure 1). The L210 enters Power-Save mode when this pin is connected to VCC, and the UART portion of the L210 is already in sleep mode.

Since Power-Save mode isolates the address, data and control signals, **the device will wake-up only by**:

- a receive data start bit transition
- a change of logic state on any of the modem or general purpose serial inputs: i.e., any of the MSR bits 0-3 shows a '1'

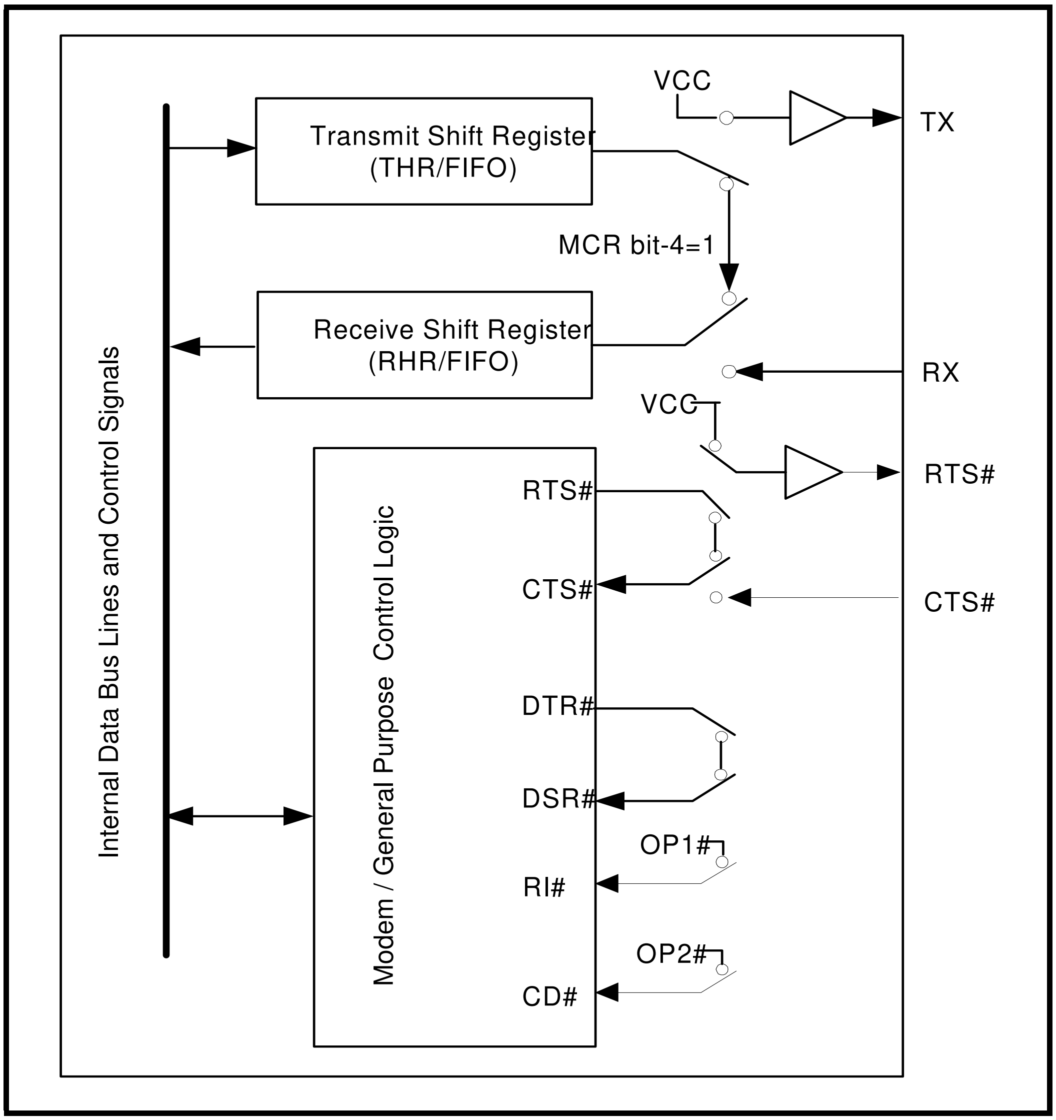
The L210 will return to the Power-Save mode automatically after a read to the MSR (to reset the modem inputs) and all interrupting conditions have been serviced and cleared. The L210 will stay in the Power-Save mode of operation until it is disabled by setting IER bit-4 to a logic 0 and/or the Power-Save pin is connected to GND.

If the L210 is awakened by any one of the above conditions, it issues an interrupt as soon as the oscillator circuit is up and running and the device is ready to transmit/receive. This interrupt has the same encoding (bit-0 of ISR register = 1) as "no interrupt pending" and will clear when the ISR register is read. This will show up in the ISR register only if no other interrupts are enabled.

2.18 Internal Loopback

The L210 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally including automatic hardware and software flow control. Figure 11 below shows how the internal UART signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX and RTS# pins are held HIGH while RX and CTS# inputs are ignored. Caution: the RX input pin must be held at inactive during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal.

FIGURE 11. INTERNAL LOOP BACK



3.0 UART INTERNAL REGISTERS

The L210 has a set of configuration registers selected by address lines A0, A1 and A2 with CS# asserted. The complete register set is shown on Table 5 and Table 6.

TABLE 5: UART INTERNAL REGISTERS

ADDRESSES A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor Latch Low Byte	Read/Write	LCR[7] = 1
0 0 1	DLM - Divisor Latch High Byte	Read/Write	
0 0 0	DREV - Device Revision Code	Read-only	DLL = 0x00, DLM = 0x00 and LCR[7] = 1
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR ≠ 0xBF
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register	Read-only	
1 1 0	MSR - Modem Status Register	Read-only	
1 1 1	SPR - Scratchpad Register	Read/Write	LCR ≠ 0xBF
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Register	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Write	
1 0 1	Xon-2 - Xon Character 2	Write	
1 1 0	Xoff-1 - Xoff Character 1	Write	
1 1 1	Xoff-2 - Xoff Character 2	Write	

Table 6: Internal Registers Descriptions. Shaded bits are enabled when EFR Bit-4=1

Address A2-A0	Reg Name	Read/ Write	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	Comment
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR ≠ 0xBF
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Prescaler	0	0/ XonAny	Internal Loopback Enable	INT Output Enable (OP2#)	(OP1#)	RTS Output Control	DTR# Output Control	LCR ≠ 0xBF
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Overrun Error	RX Data Ready	
1 1 0	MSR	RD	CD Input	RI Input	DSR Input	CTS Input	Delta CD	Delta RI	Delta DSR	Delta CTS	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR ≠ 0xBF
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	0	0	0	1	

TABLE 6: INTERNAL REGISTERS DESCRIPTIONS. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Enhanced Registers											
0 1 0	EFR	RD/WR	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5], MCR[2]	Software Flow Cntl Bit-3	Software Flow Cntl Bit-2	Software Flow Cntl Bit-1	Software Flow Cntl Bit-0	LCR=0xBF
1 0 0	XON1	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTERS DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

SEE ”RECEIVER” ON PAGE 10.

4.2 Transmit Holding Register (THR) - Write-Only

SEE ”TRANSMITTER” ON PAGE 9.

4.3 Baud Rate Generator Divisors (DLL and DLM) - Read/Write

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter. The rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to ‘1’. SEE ”PROGRAMMABLE BAUD RATE GENERATOR” ON PAGE 8. for more details.

4.4 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.4.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.4.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR bit-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR19L210 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS interrupt (default).
- Logic 1 = Enable the RTS interrupt. The UART issues an interrupt when the RTS pin makes a transition from low to high.

IER[7]: CTS Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS interrupt (default).
- Logic 1 = Enable the CTS interrupt. The UART issues an interrupt when CTS pin makes a transition from low to high.

4.5 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, **Table 7**, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.5.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.
- CTS is when the CTS pin is de-asserted during auto CTS flow control enabled by EFR bit-7.
- RTS is when the RTS pin is de-asserted during auto RTS flow control enabled by EFR bit-6.
- Wake-up Interrupt is when the device wakes up from sleep mode. See Sleep Mode section for more details.

4.5.2 Interrupt Clearing:

- LSR interrupt is cleared by reading the LSR register (but FIFO error bit does not clear until the character(s) that generated the interrupt(s) is (are) read from the FIFO).
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading the RHR register.
- TXRDY interrupt is cleared by reading the ISR register or writing to the THR register.
- MSR interrupt is cleared by reading the MSR register.
- Xoff interrupt is cleared by reading the ISR or when Xon character(s) is received.
- Special character interrupt is cleared by reading the ISR or after the next character is received.
- RTS and CTS flow control interrupts are cleared by reading the MSR register.
- Wake-up interrupt is cleared by reading the ISR register.

TABLE 7: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or Special character)
7	1	0	0	0	0	0	CTS, RTS change of state
-	0	0	0	0	0	1	None (default) or Wake-up Interrupt

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition) or wake-up interrupt. The wake-up interrupt is issued when the L210 has been awakened from sleep mode.

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 7).

ISR[4]: Xoff/Xon or Special Character Interrupt Status

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s). If this is an Xoff/Xon interrupt, it can be cleared by a read to the ISR. If it is a special character interrupt, it can be cleared by reading ISR or it will automatically clear after the next character is received.

ISR[5]: RTS#/CTS# Interrupt Status

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-5 indicates that the CTS# or RTS# has been de-asserted.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.6 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a ‘1’.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select (Legacy)

This bit has no function and should be left at '0'.

FCR[5:4]: Transmit FIFO Trigger Select

('00' = default, TX trigger level = 1)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 8 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed.

FCR[7:6]: Receive FIFO Trigger Select

('00' = default, RX trigger level =1)

These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. Table 8 shows the selections.

TABLE 8: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION

FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
		0	0		1 (default)	16L580 and 16C580 compatible.
		0	1		4	
		1	0		8	
		1	1		14	
0	0			1 (default)		16L580, 16C550, 16C580, 16C554, 16C2550 and 16C2552 compatible
0	1			4		
1	0			8		
1	1			14		

4.7 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 9 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 9: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"