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GENERAL DESCRIPTION

The XR19L212 (L212) is a highly integrated device that combines a full-featured two channel Universal Asynchronous Receiver and Transmitter (UART) and RS-232 transceivers. The L212 is designed to operate with a single 3.3V or 5V power supply. The L212 is fully compliant with EIA/TIA-232-F Standards from a +3.3V to +5.5V power supply. The device operates at 1 Mbps data rate with worst case 3K ohms load. Both RS-232 driver outputs and receiver inputs can operate in harsh electrical environments of +/-15V without damage and can survive multiple +/-15kV ESD on the RS-232 lines, while maintaining RS-232 output levels.

The L212 operates in four different modes: Active, Partial Sleep, Full Sleep and Power-Save. Each mode can be invoked via hardware or software. Upon power-up, the L212 is in the Active mode where the UART and RS-232 transceiver function normally. In the Partial Sleep mode, the internal crystal oscillator of the UART or charge pump of the RS-232 transceiver is turned off. In Full Sleep mode, both the crystal oscillator and the charge pump are turned off. While the UART is in the Sleep mode, the Power-Save mode isolates the core logic from the control signals (chip select, read/write strobes, address and data bus lines) to minimize the power consumption. The RS-232 receivers remain active in any of these four modes.

APPLICATIONS

- Battery-Powered Equipment
- Handheld and Mobile Devices
- Handheld Terminals
- Industrial Peripheral Interfaces
- Point-of-Sale (POS) Systems

FEATURES

- Meets true EIA/TIA-232-F Standards from +3.3V to +5.5V operation
- Up to 1 Mbps data transmission rate
- 45us sleep mode exit (charge pump to full power)
- ESD protection for RS-232 I/O pins at
  - +/-15kV - Human Body Model
  - +/-15kV - IEC 61000-4-2, Air-Gap Discharge
  - +/- 8kV - IEC 61000-4-2, Contact Discharge
- Software compatible with industry standard 16550 UART
- Intel/Motorola bus select
- Complete modem interface
- Sleep and Power-save modes to conserve battery power
- Wake-up interrupt upon exiting low power modes

FIGURE 1. BLOCK DIAGRAM

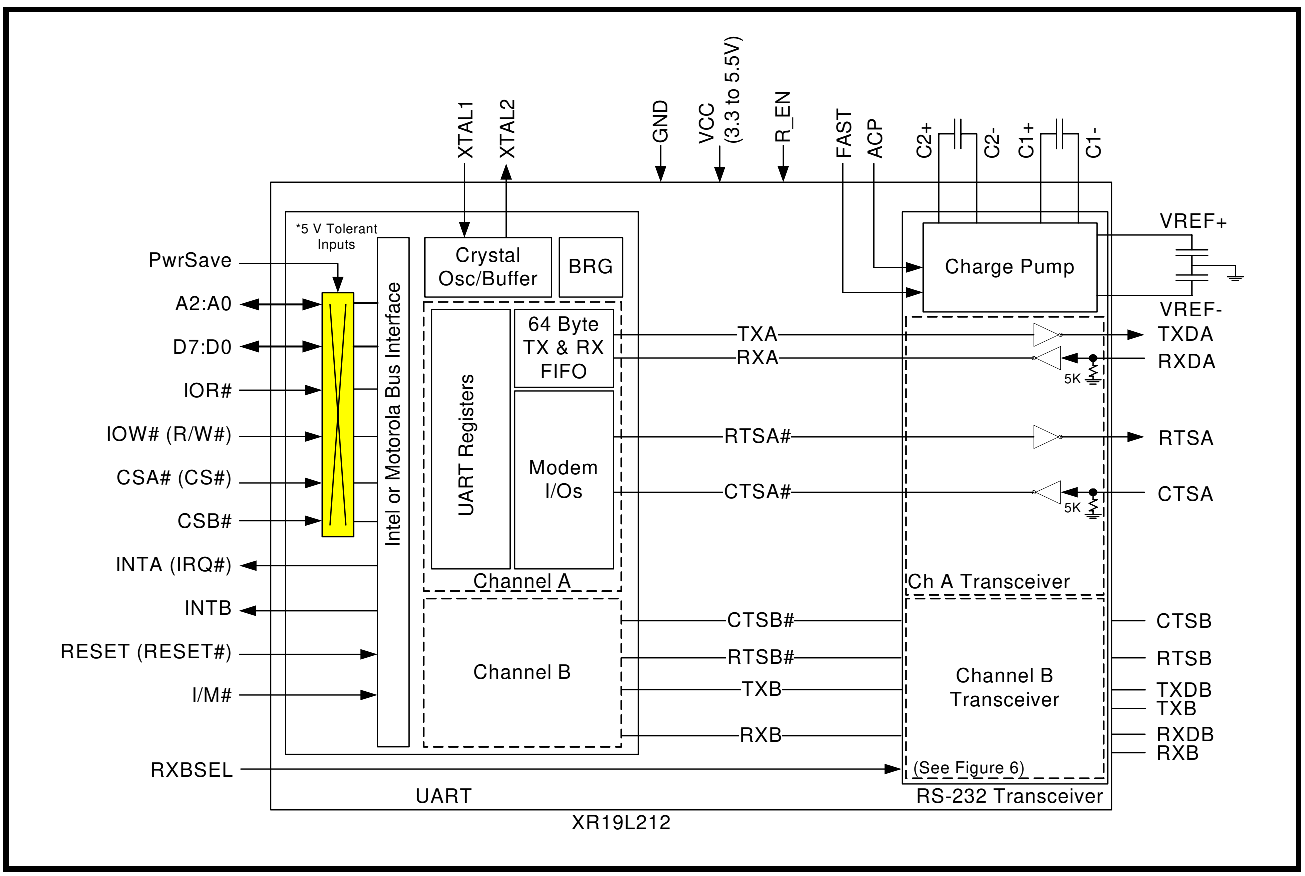
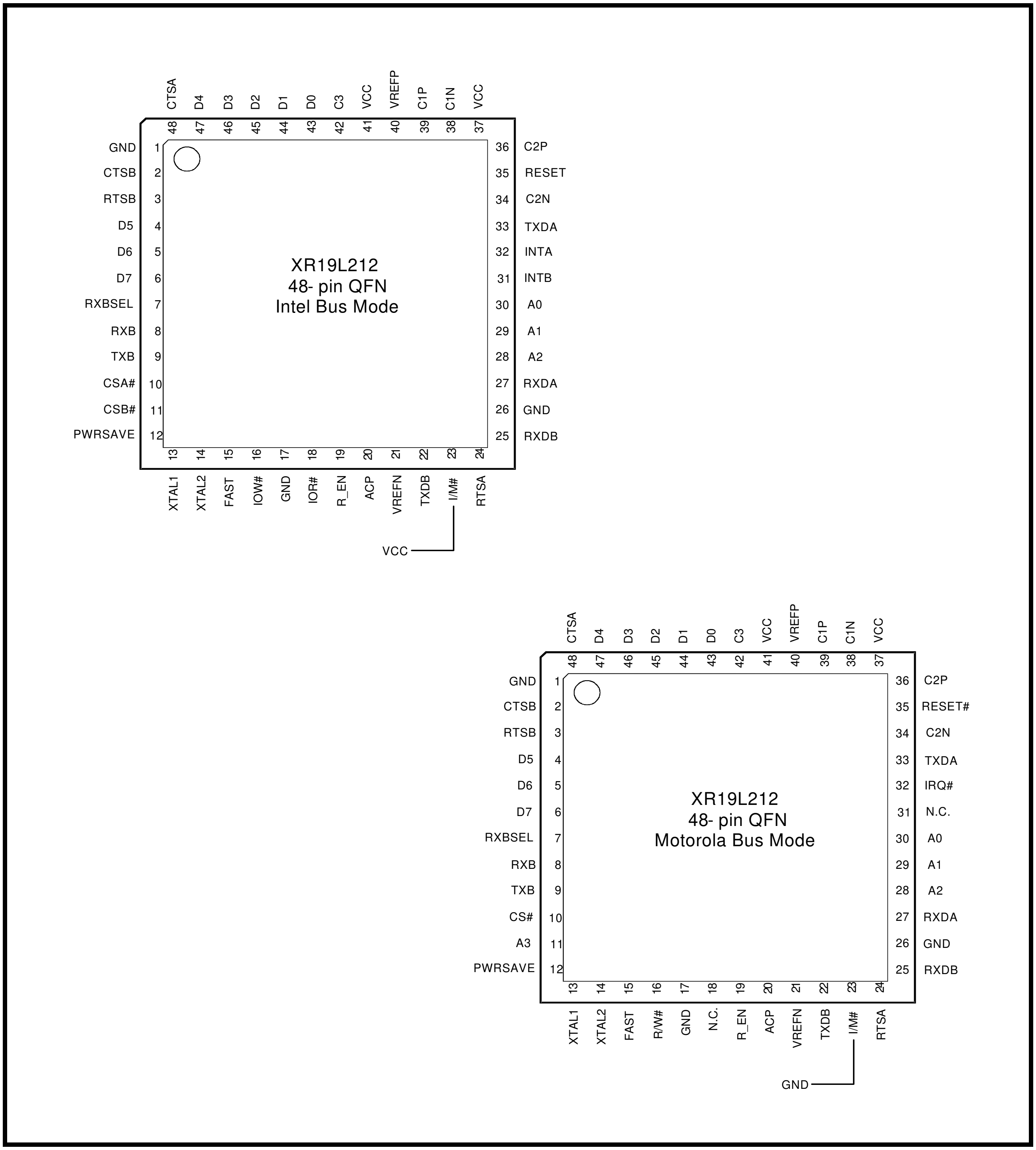


FIGURE 2. PIN OUT OF THE DEVICE



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR19L212IL48	48-pin QFN	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Descriptions

NAME	48-QFN PIN#	TYPE	DESCRIPTION
DATA BUS INTERFACE (CMOS/TTL Voltage Levels)			
A2 A1 A0	28 29 30	I	Address bus lines [2:0]. These 3 address lines select one of the internal registers in the UART during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	6 5 4 47 46 45 44 43	I/O	Data bus lines [7:0] (bidirectional).
IOR# (NC)	18	I	When I/M# pin is HIGH, the Intel bus interface is selected and this input becomes read strobe (active LOW). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], puts the data byte on the data bus to allow the host processor to read it on the rising edge. When I/M# pin is LOW, the Motorola bus interface is selected and this input is not used.
IOW# (R/W#)	16	I	When I/M# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active LOW). The falling edge instigates the internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines. When I/M# pin is LOW, the Motorola bus interface is selected and this input becomes read (HIGH) and write (LOW) signal.
CSA# (CS#)	10	I	When I/M# pin is HIGH, this input is chip select A (active low) to enable channel A in the device. When I/M# pin is LOW, this input becomes the chip select (active low) for the Motorola bus interface.
CSB# (A3)	11	I	When I/M# pin is HIGH, this input is chip select B (active low) to enable channel B in the device. When I/M# pin is LOW, this input becomes address line A3 which is used for channel selection in the Motorola bus interface. Input logic 0 selects channel A and logic 1 selects channel B.
INTA (IRQ#)	32	O (OD)	When I/M# pin is HIGH, it selects Intel bus interface and this output become the active HIGH device interrupt output for channel A. This output is enabled through the software setting of MCR[3]: set to the active mode when MCR[3] is set to a logic 1, and set to the three state mode when MCR[3] is set to a logic 0. See MCR[3]. When I/M# pin is LOW, it selects Motorola bus interface and this output becomes the active LOW, open-drain interrupt output for both channels. An external pull-up resistor is required for proper operation. MCR[3] must be set to a logic 0 for proper operation of the interrupt.
INTB (NC)	31	O (OD)	When I/M# pin is HIGH, it selects Intel bus interface and this output become the active HIGH device interrupt output for channel B. This output is enabled through the software setting of MCR[3]: set to the active mode when MCR[3] is set to a logic 1, and set to the three state mode when MCR[3] is set to a logic 0. See MCR[3]. When I/M# pin is LOW, it selects Motorola bus interface and this output is not used and can be left unconnected.

Pin Descriptions

NAME	48-QFN PIN#	TYPE	DESCRIPTION
MODEM OR SERIAL I/O INTERFACE (EIA-232/RS-232 Voltage Levels)			
TXDA	33	O	UART Channel A Transmit Data. The TX signal will be LOW (< 1.5V) during reset or idle (no data).
RXDA	27	I	UART Channel A Receive Data. The RX data input must idle LOW (< 1.5V). This input has an internal pull-down resistor and can be left unconnected when not used.
RTSA	24	O	UART Channel A Request-to-Send or general purpose outputs. These outputs must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1] and IER[6].
CTSA	48	I	UART Channel A Clear-to-Send or general purpose inputs. It can be used for auto CTS flow control, see EFR[7], MSR[4] and IER[7]. This input has an internal pull-down resistor and can be left unconnected when not used.
TXDB	22	O	UART Channel B Transmit Data. The TX signal will be LOW (< 1.5V) during reset or idle (no data).
RXDB	25	I	UART Channel B Receive Data. RXDB will be the input signal to the internal UART when RXBSEL is LOW. If RXB is used, then RXBSEL should be HIGH. The RX data input must idle LOW (< 1.5V). This input has an internal pull-down resistor and can be left unconnected when not used.
RTSB	3	O	UART Channel B Request-to-Send or general purpose outputs. These outputs must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1] and IER[6].
CTSB	2	I	UARTChannel B Clear-to-Send or general purpose inputs. It can be used for auto CTS flow control, see EFR[7], MSR[4] and IER[7]. This input has an internal pull-down resistor and can be left unconnected when not used.
SERIAL I/O INTERFACE (CMOS/TTL Voltage Levels)			
TXB	9	O	UART Channel B Transmit data. This is the TXB output signal from the UART. This pin can be used to communicate with an external Infrared or RS-422 transceiver if TXDB is unused.
RXB	8	I	UART Channel B Receive data. This is the RXB input signal to the UART. If RXDB is not used (RXBSEL is HIGH), then this pin can be used to communicate with an external Infrared or RS-422 transceiver. If RXDB is used (RXBSEL is LOW), this pin should be left open.
ANCILLARY SIGNALS (CMOS/TTL Voltage Levels)			
XTAL1	13	I	Crystal or external clock input. This input is not 5V tolerant.
XTAL2	14	O	Crystal or buffered clock output. This output may be use to drive a clock buffer which can drive other device(s).
PwrSave	12	I	Power-Save (active high). This feature isolates the L212's data bus interface from the host preventing other bus activities that cause higher power drain during sleep mode. See Sleep Mode with Auto Wake-up and Power-Save Feature section for details.
ACP	20	I	Autosleep for Charge Pump (active HIGH). When this pin is HIGH, the charge pump is shut off if the L212 is already in partial sleep mode, i.e. the crystal oscillator is stopped. **See "Section 2.18, Sleep Modes and Power-Save Feature with Wake-Up Interrupt" on page 19.**

Pin Descriptions

NAME	48-QFN PIN#	TYPE	DESCRIPTION
I/M#	23	I	Intel or Motorola Bus Select. When I/M# pin is HIGH, 16 or Intel Mode, the device will operate in the Intel bus type of interface. When I/M# pin is LOW, 68 or Motorola mode, the device will operate in the Motorola bus type of interface.
RESET (RESET#)	35	I	When I/M# pin is HIGH for Intel bus interface, this input becomes RESET (active high). When I/M# pin is LOW for Motorola bus interface, this input becomes RESET# (active low). A 40 ns minimum active pulse on this pin will reset the internal registers and all outputs of the UART. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (see Table 16).
C2P C2N	36 34	-	Charge pump capacitors. As shown in Figure 1, a 0.1 uF capacitor should be placed between these 2 pins.
C1P C1N	39 38	-	Charge pump capacitors. As shown in Figure 1, a 0.1 uF capacitor should be placed between these 2 pins.
VREFP	40	Pwr	+5.0V generated by the charge pump.
VREFN	21	Pwr	-5.0V generated by the charge pump.
R_EN	19	I	When the supply voltage is < 3.6V, connect R_EN to VCC. When the supply voltage is > 3.6V, connect R_EN to GND.
C3	42	I	When the supply voltage is 3.3 V, C3A and C3B should be connected to VCC. When the supply voltage is 5 V, C3A should be connected to C3B with a 1 uF capacitor to GND.
RXBSEL	7	I	When RXBSEL is HIGH, RXB is the input to the receiver of the UART. When RXBSEL is LOW, RXDB is the input to the receiver of the UART.
FAST	15	I	When FAST is HIGH, the maximum serial data rate is 1 Mbps. When FAST is LOW, the maximum serial data rate is 250 Kbps.
VCC	37, 41	Pwr	3.3V to 5.5V power supply. All CMOS/TTL input pins, except XTAL1, are 5V tolerant.
GND	1, 17, 26	Pwr	Power supply common, ground.
-	PAD	Pwr	The center pad on the backside of the 48-QFN package is metallic and is not electrically connected to anything inside the device. It must be soldered on to the PCB and may be optionally connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.

NOTE: *Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain. For CMOS/TTL Voltage levels, 'LOW' indicates a voltage in the range 0V to VIL and 'HIGH" indicates a voltage in the range VIH to VCC. For RS-232 Voltage levels, 'LOW' is any voltage < 1.5V and 'HIGH' is any voltage > 3V.*

1.0 PRODUCT DESCRIPTION

The XR19L212 consists of a two-channel UART and RS-232 transceivers. It operates from a single +3V to 5.5V supply with data rates up to 1Mbps, while meeting all EIA RS-232F specifications. Its feature set is fully compatible to the industry standard 16C550. Unlike the 16C550, most of the modem signals are not CMOS/TTL level, but conform to EIA/TIA 232 or RS-232 voltage levels. The only two signals that are CMOS/TTL level are the TXB and RXB signals. They can be used with an external IR or RS-422 transceiver when their corresponding RS-232 signals, TXDB and RXDB, are not used. The configuration register set is 16550 UART compatible for control, status and data transfer. Also, the L212 has 64-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, transmit and receive FIFO trigger levels, and a programmable fractional baud rate generator with a prescaler of divide by 1 or 4. Additionally, the L212 includes the ACP pin which the user can shut down the charge pump for the RS-232 drivers. In the UART portion, the Power-Save feature isolates the databus interface to further reduce power consumption in the Sleep mode. The L212 is fabricated using an advanced CMOS process.

Enhanced Features

The L212 UART provides a solution that supports 64 bytes of transmit and receive FIFO. Increased performance is realized in the L212 by the transmit and receive FIFOs, FIFO trigger level controls and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the L212 provides the ACP and Power-Save modes that drastically reduces the power consumption when the device is not used. The combination of the above greatly reduces the CPU’s bandwidth requirement, increases performance, and reduces power consumption.

Intel or Motorola Data Bus Interface

The L212 provides a host interface that supports Intel or Motorola microprocessor (CPU) data bus interface. The Intel bus compatible interface allows direct interconnect to Intel compatible type of CPUs using IOR#, IOW# and CS# inputs for data bus operation. The Motorola bus compatible interface instead uses the R/W# and CS# signals for data bus transactions. See pin description section for details on all the control signals. The Intel and Motorola bus interface selection is made through the pin, I/M#.

Data Rate

The L212 is capable of operation up to 1 Mbps data rate. The UART section can operate at much higher speeds, but the speed of the RS-232 transceiver is limited to 1 Mbps. The device can operate either with a crystal on pins XTAL1 and XTAL2, or external clock source on XTAL1 pin.

Internal Enhanced Register Sets

The L212 UART has a set of enhanced registers providing control and monitoring functions. Interrupt enable/disable and status, FIFO enable/disable, selectable TX and RX FIFO trigger levels, automatic hardware/software flow control enable/disable, programmable baud rates, modem interface controls and status, sleep mode and infrared mode are all standard features. Following a power on reset or an external reset (and operating in 16 or Intel Mode), the registers defaults to the reset condition and is compatible with the 16C550.

RS-232 Interface

The L212 includes RS-232 drivers/receivers for the modem interface. This feature eliminates the need for an external RS-232 transceiver. The charge pump provides output voltages of +5V and -5V for its drivers over the 3.3V to 5.5V VCC supply voltage. The serial outputs TXD and RTS swing between -5V (inactive) and 5V (active) RS-232 voltage levels. The serial inputs RXD and CTS are RS-232 receivers and can take any voltage swing from -15V to +15V. The receivers are always active, even in Full Sleep and Power-Save modes. The RS-232 drivers guarantee a data rate of 1 Mbps even when fully loaded with 3Kohm in parallel with 1000pF load.

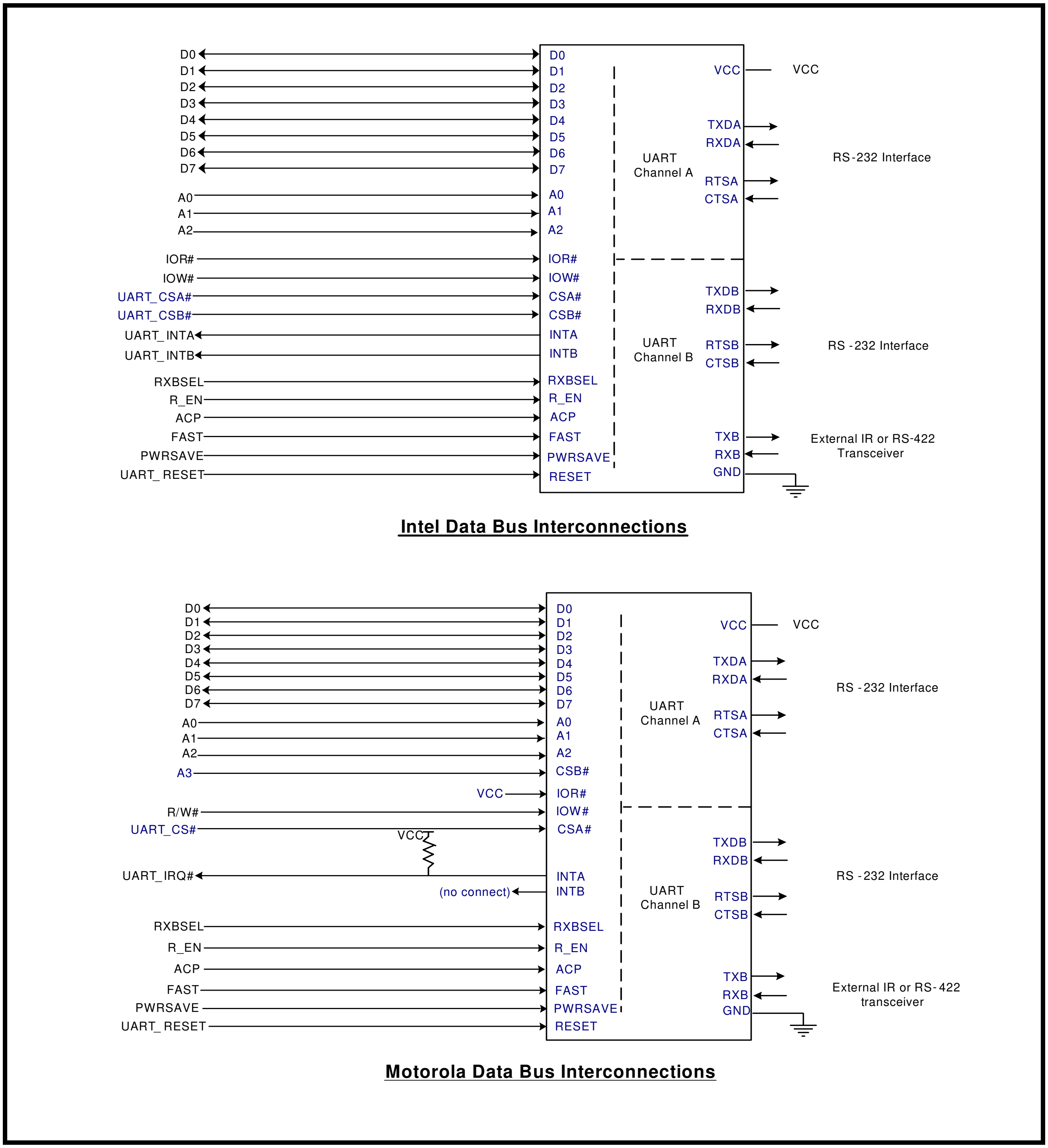
All RS-232 drivers and receivers are protected to ±15kV using the Human Body Model ground combination, ±8kV using IEC 61000-4-2 Contact Discharge, and ±15kV using IEC 61000-4-2 Air-Gap Discharge. For more information, send an e-mail to uarttechsupport@exar.com.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The L212 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# or R/W# inputs. A typical data bus interconnection for Intel and Motorola mode is shown in **Figure 3**.

FIGURE 3. XR19L212 TYPICAL INTEL/MOTOROLA DATA BUS INTERCONNECTIONS



2.2 5-Volt Tolerant Inputs

The CMOS/TTL level inputs of the L212 can accept up to 5V inputs when operating at 3.3V. Note that the XTAL1 pin is not 5V tolerant when an external clock supply is used.

2.3 Device Hardware Reset

The RESET or RESET# input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 16). An active pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Device Identification and Revision

The XR19L212 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x01 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 Channel A and B Selection

The XR19L212 provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. During Intel Bus Mode (I/M# pin connected to VCC), a LOW on chip select pins, CSA# or CSB#, allows the user to select UART channel A or B to configure, send transmit data and/or unload receive data to/from the UART. Selecting both UARTs can be useful during power up initialization to write to the same internal registers, but do not attempt to read from both UARTs simultaneously. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A AND B SELECT IN 16 MODE

CSA#	CSB#	FUNCTION
1	1	UART de-selected
0	1	Channel A selected
1	0	Channel B selected
0	0	Channel A and B selected

During Motorola Bus Mode (I/M# pin connected to GND), the package interface pins are configured for connection with Motorola and other popular microprocessor bus types. In this mode the XR19L212 decodes an additional address, A3, to select one of the UART ports. The A3 address decode function is used only when in the Motorola Bus Mode. See Table 2.

TABLE 2: CHANNEL A AND B SELECT IN 68 MODE

CS#	A3	FUNCTION
1	N/A	UART de-selected
0	0	Channel A selected
0	1	Channel B selected

2.6 Channel A and B Internal Registers

Each UART channel in the L212 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550 and dual ST16C2550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and an user accessible Scratchpad register (SPR).

Beyond the general 16C550 features and capabilities, the L212 offers enhanced feature registers such as EFR, Xon/Xoff 1, Xon/Xoff 2, FCTR, TRG, EMSR and FC that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, FIFO trigger level control and FIFO level counters. All the register functions are discussed in full detail later in **"Section 3.0, UART Internal Registers" on page 22**.

2.7 DMA Mode

The DMA Mode (a legacy term) refers to data block transfer operation. The DMA mode affects the state of the RXRDY# and TXRDY# output pins available in the original 16C550. These pins are not available in the XR19L212. The DMA Enable bit (FCR bit-3) does not have any function in this device and can be a '0' or a '1'.

2.8 INT (IRQ#) Output

The interrupt output changes according to the operating mode and enhanced features setup. **Table 3** and **Table 4** below summarize the operating behavior for the transmitter and receiver in the Intel and Motorola modes. Also see Figures **19** through **22**.

TABLE 3: INT (IRQ#) PIN OPERATION FOR TRANSMITTER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (I/M# = 1)	0 = one byte in THR 1 = THR empty	0 = FIFO above trigger level 1 = FIFO below trigger level or FIFO empty
IRQ# Pin (I/M# = 0)	1 = one byte in THR 0 = THR empty	1 = FIFO above trigger level 0 = FIFO below trigger level or FIFO empty

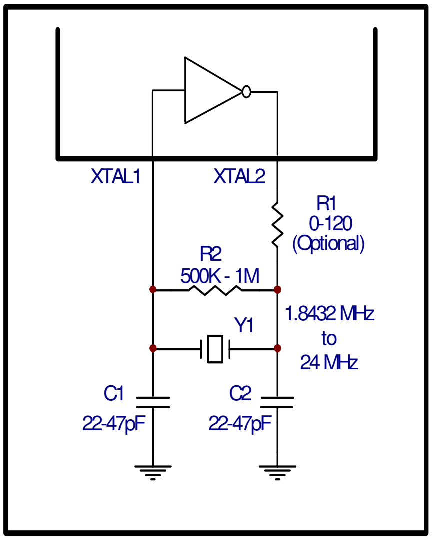
TABLE 4: INT (IRQ#) PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INT Pin (I/M# = 1)	0 = no data 1 = 1 byte	0 = FIFO below trigger level 1 = FIFO above trigger level
IRQ# Pin (I/M# = 0)	1 = no data 0 = 1 byte	1 = FIFO below trigger level 0 = FIFO above trigger level

2.9 Crystal or External Clock Input

The L212 includes an on-chip oscillator (XTAL1 and XTAL2) to generate a clock when a crystal is connected between the XTAL1 and XTAL2 pins of the device. Alternatively, an external clock can be supplied through the XTAL1 pin. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock input and XTAL2 pin is the bufferred output which can be used as a clock signal for other devices in the system. Please note that the input XTAL1 is not 5V tolerant and therefore, the maximum voltage at the pin should be 3.3V when an external clock is supplied. For programming details, see "Programmable Baud Rate Generator."

FIGURE 4. TYPICAL CRYSTAL CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins. When VCC = 5V, the on-chip oscillator can operate with a crystal whose frequency is not greater than 24 MHz. On the other hand, the L212 can accept an external clock of up to 64 MHz at XTAL1 pin also. Although the L212 can accept an external clock of up to 50MHz, the maximum data rate supported by the RS-232 drivers is 1Mbps. For further reading on the oscillator circuit please see the Application Note DAN108 on the EXAR web site at **http://www.exar.com.**

2.10 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (216 - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon reset. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the dvisior. Only the four lower bits of the DLD are implemented and they are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. **Table 5** shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in **Table 5**. At 8X sampling rate, these data rates would double. Also, when using 8X sampling mode, please note that the bit-time will have a jitter (+/- 1/16) whenever the DLD is non-zero and is an odd number. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), with 16X mode **EMSR[7] = 1**
Required Divisor (decimal) = (XTAL1 clock frequency / prescaler / (serial data rate x 8), with 8X mode **EMSR[7] = 0**

The closest divisor that is obtainable in the L212 can be calculated using the following formula:

ROUND((Required Divisor - TRUNC(Required Divisor))*16)/16 + TRUNC(Required Divisor), where

DLM = TRUNC(Required Divisor) >> 8
DLL = TRUNC(Required Divisor) & 0xFF
DLD = ROUND((Required Divisor-TRUNC(Required Divisor))*16)

In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value ’A’ by ’B’ number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 5. BAUD RATE GENERATOR

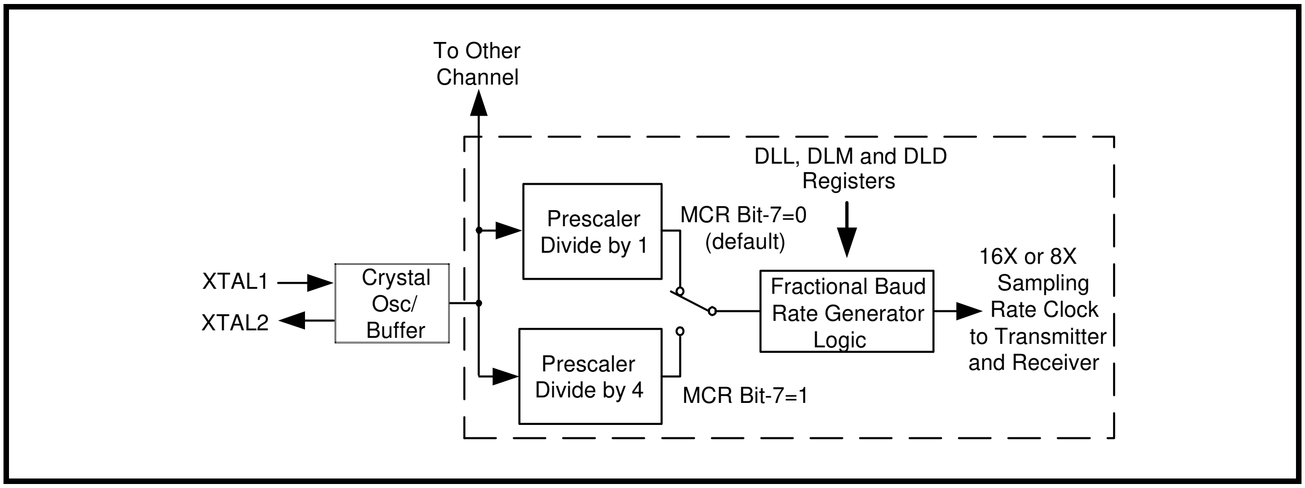
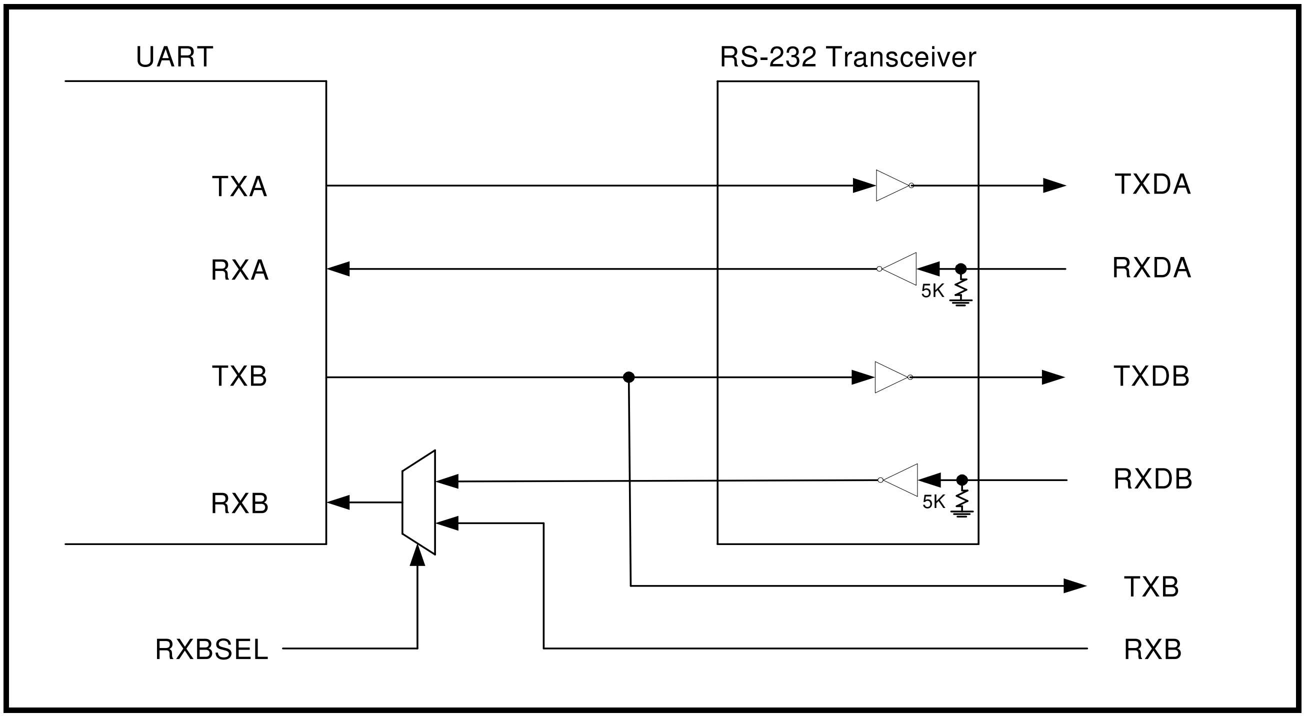


TABLE 5: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	Divisor for 16x Clock (Decimal)	Divisor Obtainable in L212	DLM Program Value (HEX)	DLL Program Value (HEX)	DLD Program Value (HEX)	Data Error Rate (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0
300000	5	5	0	5	0	0
400000	3.75	3 12/16	0	3	C	0
460800	3.2552	3 4/16	0	3	4	0.16
500000	3	3	0	3	0	0
750000	2	2	0	2	0	0
921600	1.6276	1 10/16	0	1	A	0.16
1000000	1.5	1 8/16	0	1	8	0

FIGURE 6. XR19L212 TRANSMITTER AND RECEIVER



2.11 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X internal clock. A bit time is 16 (8) clock periods (see EMSR bit-7). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

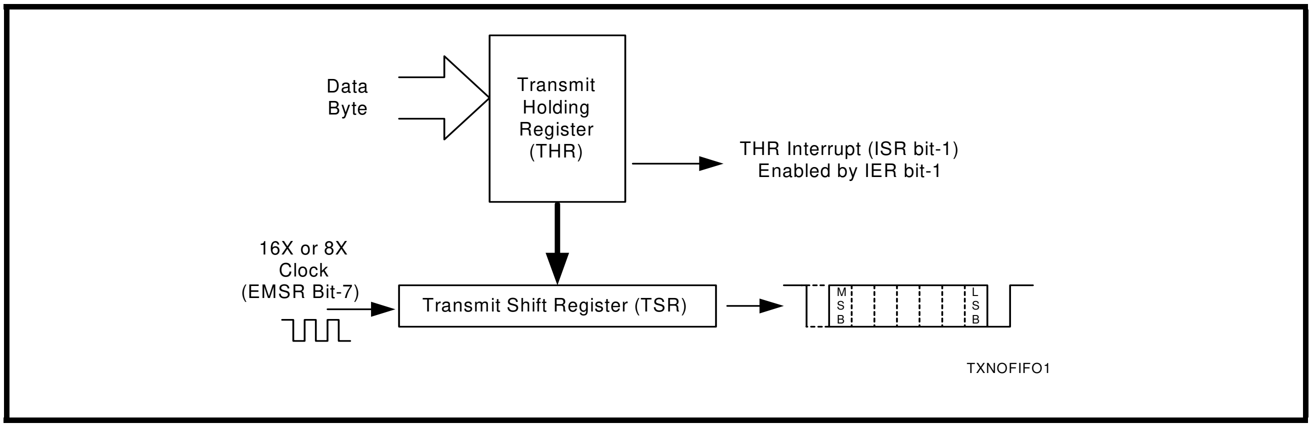
2.11.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.11.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

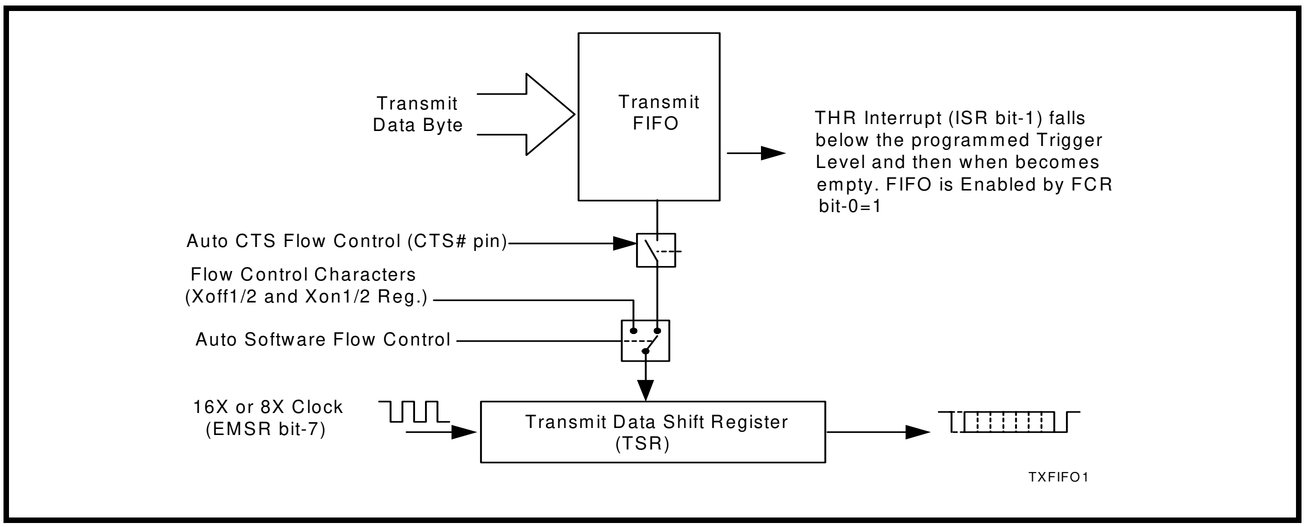
FIGURE 7. TRANSMITTER OPERATION IN NON-FIFO MODE



2.11.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The Transmitter Empty Flag (LSR bit-6) is set when both the TSR and the FIFO become empty.

FIGURE 8. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.12 RECEIVER

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X clock (EMSR bit-7) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X clock rate. After 8 clocks (or 4 if 8X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.12.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

2.12.2 Selectable Input to RX of Channel B

There is an input (RXBSEL) that selects whether the signal going to the RXB input of the UART will be the signal from the RS-232 transceiver or not. If RXBSEL is LOW, then the signal to the RXB input is the RXDB signal from the RS-232 transceiver. When RXDB is used, the RXB input should be left floating. The signal received at the UART can be probed at the RXB pin. If RXBSEL is HIGH, then the RXDB pin is tri-stated and RXB can be used with an external Infrared transceiver or RS-422 transceiver. If RXB is selected but is unused, RXB should be connected to VCC. See Figure 6 for a detailed drawing.

FIGURE 9. RECEIVER OPERATION IN NON-FIFO MODE

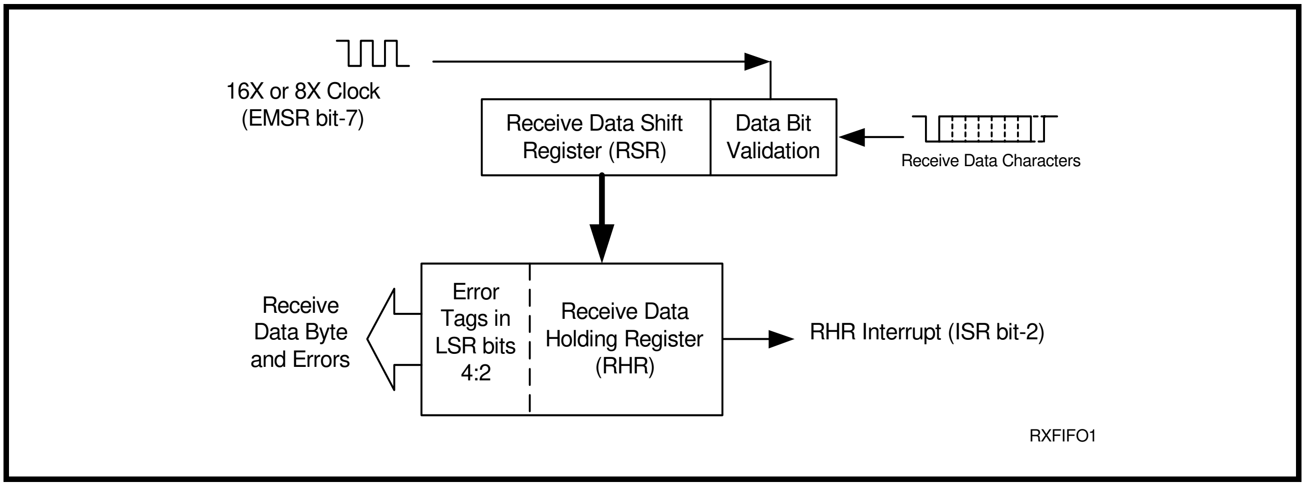
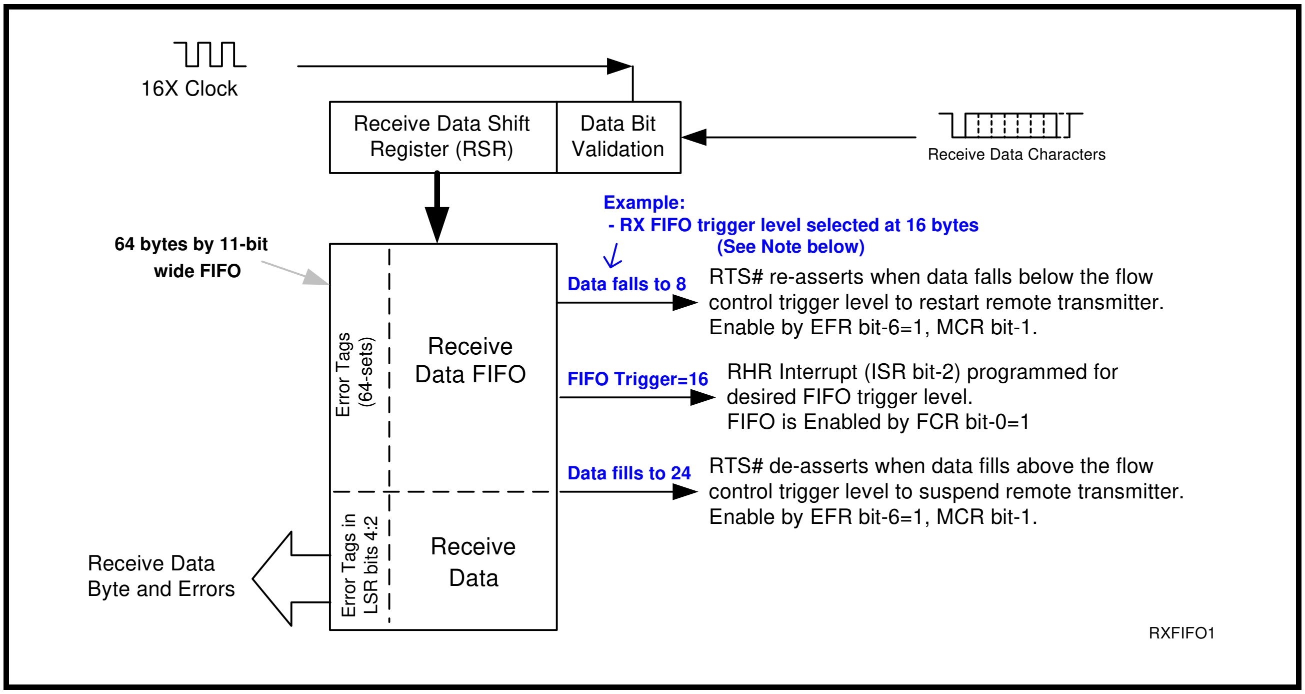


FIGURE 10. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: *Table-B selected as Trigger Table for* **Figure 10** *(***Table 14***).*

2.13 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control feature is enabled to fit specific application requirement (see **Figure 11**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.14 Auto RTS Hysteresis

The L212 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the XR16C850, ST16C650A and ST16C550 family of UARTs. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS pin will not be de-asserted until the receive FIFO reaches the upper limit of the hysteresis level. The RTS pin will be re-asserted after the RX FIFO is unloaded to the lower limit of the hysteresis level. Under the above described conditions, the L212 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS output pin is asserted. **Table 13** shows the complete details for the Auto RTS Hysteresis levels. Please note that this table is for programmable trigger levels only (Table D). The hysteresis values for Tables A-C are the next higher and next lower trigger levels in the corresponding table.

2.15 Auto CTS Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 11**):

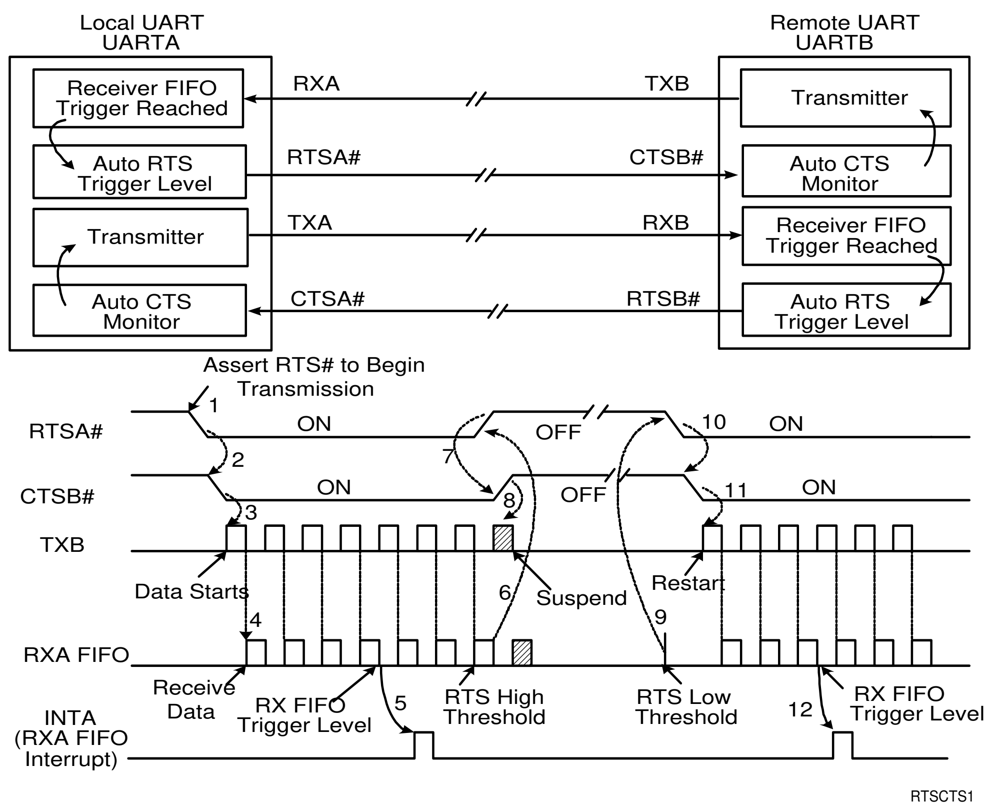
- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS pin is de-asserted: ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS input is re-asserted, indicating more data may be sent.

FIGURE 11. AUTO RTS AND CTS FLOW CONTROL OPERATION

The signals shown in this figure are the signals at the UART and not at the RS-232 transceiver.



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.16 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (**See Table 15**), the L212 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the L212 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the L212 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the L212 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (**See Table 15**) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the L212 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the L212 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The L212 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the L212 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS Hysteresis value in **Table 13**. **Table 6** below explains this when Trigger Table-B (See **Table 14**) is selected.

TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

* *After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 8-bit word length, no parity and 1 stop bit setting.*

2.17 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The L212 compares each incoming receive character with the programmed Xoff-2 data. If a match exists, the received data will be transferred to the RX FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 define the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

2.18 Sleep Modes and Power-Save Feature with Wake-Up Interrupt

There are three levels of power management integrated in the L212. The device is low power with low operational and standby supply currents. In the Partial Sleep mode, the internal oscillator of the UART or charge pump of the RS-232 transceiver is turned off to reduce the power consumption. In the Full Sleep mode, both the oscillator and the charge pump are turned off. The Power-save mode provides additional power saving by isolating the UART address, data and control signals during Sleep mode to minimize the power consumption.

2.18.1 Partial Sleep Mode

There are two different partial sleep modes. In the first mode, the UART is in sleep mode and the charge pump is active. In the other mode, the UART is still active but the charge pump is turned off.

2.18.1.1 UART in sleep mode, RS-232 transceiver active

If the ACP pin is LOW, then the charge pump for the RS-232 transceiver will always be active. But the UART portion in the L212 can still enter sleep mode if all of these conditions are satisfied:

- no interrupts pending (ISR bit-0 = 1)
- the 16-bit divisor programmed in DLM and DLL registers is a non-zero value
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RXD input pin is idling LOW

The L212 stops its crystal oscillator to conserve power in this mode. The user can check the XTAL2 pin for no clock output as an indication that the device has entered the partial sleep mode.

The UART portion in the L212 resumes normal operation or active mode by any of the following:

- a receive data start bit transition on the RXD input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: i.e., any of the MSR bits 0-3 shows a '1'

If the sleep mode is enabled and the L212 is awakened by one of the conditions described above, an interrupt is issued by the L212 to signal to the CPU that it is awake. The lower nibble of the interrupt source register (ISR) will read a value of 0x1 for this interrupt and reading the ISR clears this interrupt. Since the same value (0x1) is also used to indicate no pending interrupt, users should exercise caution while using the sleep mode. The UART portion in the L212 will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the UART portion of the L212 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The UART portion of the L212 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

2.18.1.2 UART active, charge pump of RS-232 transceiver shut down

If the ACP pin is HIGH and the UART portion of the L212 is not in sleep mode, then the charge pump will automatically shut down to conserve power if the following conditions are true:

- no activity on the TXD output signal
- modem input signals (RX, CTS) are LOW
- modem inputs have been idle for approximately 30 seconds

When these conditions are satisfied, the L212 shuts down the charge pump and tri-states the RS-232 drivers to conserve power. In this mode, the RS-232 receivers are fully active and the internal registers of the L212 can be accessed. The time for the charge pump to resume normal operation after exiting the sleep mode is typically 45µs. It will wake up by any of the following:

- a receive data start bit transition on the RXD input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a LOW to HIGH transition on any of the modem or general purpose serial inputs

Because the receivers are fully active when the charge pump is turned off, any data received will be transferred to/from the UART without any issues.

2.18.2 Full Sleep Mode

In full sleep mode, the L212 shuts down the charge pump and the internal oscillator. The L212 enters the full sleep mode if the following conditions are satisfied:

- the UART portion of the L212 is already in sleep mode (no output on XTAL2)
- the ACP (Autosleep for Charge Pump) pin is HIGH

When these conditions are satisfied, both the UART and the charge pump will be in the sleep mode. In this mode, the RS-232 receivers are fully active and the internal registers of the L212 can be accessed. The L212 exits the full sleep mode if either the ACP pin becomes LOW or the internal oscillator starts up. The time for the charge pump to resume normal operation after exiting the full sleep mode is typically 45µs.

2.18.3 Power-Save Feature

This mode is in addition to the sleep mode and in this mode, the core logic of the L212 is isolated from the CPU interface. If the address lines, data bus lines, IOW#, IOR# and CS# remain steady when the L212 is in full sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 41. However, if the input lines are floating or are toggling while the L212 is in sleep mode, the current can be up to 100 times more. If not using the Power-Save feature, an external buffer would be required to keep the address and data bus lines from toggling or floating to achieve the low current. But if the Power-Save feature is enabled (PwrSave pin connected to VCC), this will eliminate the need for an external buffer by internally isolating the address, data and control signals from other bus activities that could cause wasteful power drain (see Figure 1). The L212 enters Power-Save mode when this pin is connected to VCC, and the UART portion of the L212 is already in sleep mode.

Since Power-Save mode isolates the address, data and control signals, **the device will wake-up only by**:

- a receive data start bit transition, or
- a change of logic state on any of the modem or general purpose serial inputs: i.e., any of the MSR bits 0-3 shows a '1'

The L212 will return to the Power-Save mode automatically after a read to the MSR (to reset the modem inputs) and all interrupting conditions have been serviced and cleared. The L212 will stay in the Power-Save mode of operation until it is disabled by setting IER bit-4 to a logic 0 and/or the Power-Save pin is connected to GND.

If the L212 is awakened by any one of the above conditions, it issues an interrupt as soon as the oscillator circuit is up and running and the device is ready to transmit/receive. This interrupt has the same encoding (bit-0 of ISR register = 1) as "no interrupt pending" and will clear when the ISR register is read. This will show up in the ISR register only if no other interrupts are enabled.

2.19 Infrared Mode (UART Channel B Only)

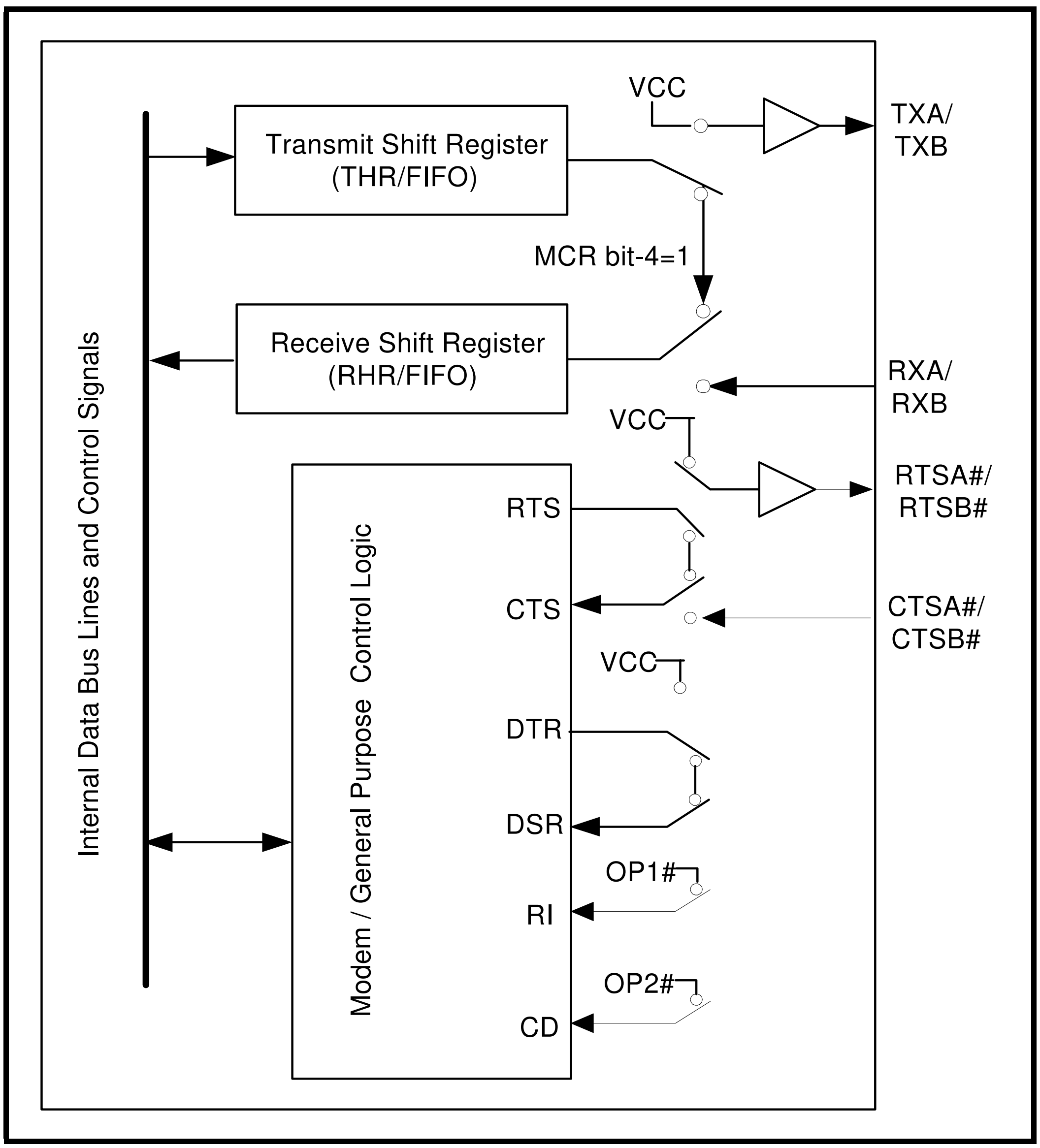
The L212 includes an infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 12 below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. When the infrared feature is enabled, the transmit data output, TXB, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see Figure 12.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RXB pin. Each time it senses a light pulse, it returns a HIGH to the data bit stream. However, this is not true with some infrared modules on the market which indicate a LOW by a light pulse. So the L212 has a provision to invert the input polarity to accommodate this. In this case user can enable FCTR bit-2 to invert the input signal.

The Infrared Mode can only be used with channel B of the L212 using the TXB output and the RXB input pins..

FIGURE 12. INTERNAL LOOP BACK



3.0 UART INTERNAL REGISTERS

The L212 has a set of configuration registers selected by address lines A0, A1 and A2 with CS# asserted. The complete register set is shown on Table 7 and Table 8.

TABLE 7: UART INTERNAL REGISTERS

ADDRESSES A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
	16C550 COMPATIBLE REGISTERS		
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor MSB	Read/Write	
0 1 0	DLD - Divisor Fractional	Read/Write	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR ≠ 0xBF
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register	Read-only	
1 1 0	MSR - Modem Status Register	Read-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	LCR ≠ 0xBF, FCTR[6] = 0
1 1 1	FLVL - RX/TX FIFO Level Counter Register	Read-only	LCR ≠ 0xBF, FCTR[6] = 1
1 1 1	EMSR - Enhanced Mode Select Register	Write-only	
	ENHANCED REGISTERS		
0 0 0	TRG - RX/TX FIFO Trigger Level Register FC - RX/TX FIFO Level Counter Register	Write-only Read-only	LCR = 0xBF
0 0 1	FCTR - Feature Control Register	Read/Write	
0 1 0	EFR - Enhanced Function Register	Read/Write	
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	

.

TABLE 8: INTERNAL REGISTER DESCRIPTIONS. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR ≠ 0xBF
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Mode ENable	0/ XonAny	Internal Lopback Enable	OP2#/INT Output Enable	Rsrvd (OP1#)	RTS# Output Control	Output Control	LCR ≠ 0xBF
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Overrun Error	RX Data Ready	
1 1 0	MSR	RD	Input	Input	Input	CTS# Input	Reserved	Reserved	Reserved	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR ≠ 0xBF FCTR[6]=0
1 1 1	EMSR	WR	16X Sampling Rate Mode	LSR Error Interrupt. Imd/Dly#	Auto RTS Hyst. bit-3	Auto RTS Hyst. bit-2	Rsrvd	Rsrvd	Rx/Tx FIFO Count	Rx/Tx FIFO Count	LCR ≠ 0xBF FCTR[6]=1
1 1 1	FLVL	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 8: INTERNAL REGISTER DESCRIPTIONS. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 1 0	DLD	RD/WR	0	0	0	0	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF EFR[4] = 1
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR≠0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	1	0	1	0	
Enhanced Registers											
0 0 0	TRG	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
0 0 0	FC	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	FCTR	RD/WR	RX/TX Mode	SCPAD Swap	Trig Table Bit-1	Trig Table Bit-0	Rsrvd	RX IR Input Inv.	Auto RTS Hyst Bit-1	Auto RTS Hyst Bit-0	
0 1 0	EFR	RD/WR	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5], DLD	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

SEE "RECEIVER" ON PAGE 14.

4.2 Transmit Holding Register (THR) - Write-Only

SEE "TRANSMITTER" ON PAGE 13.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR19L212 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO (default). Instead, LSR bits 2-4 can be programmed to generate an interrupt immediately, by setting EMSR bit-6 to a logic 1.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.