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GENERAL DESCRIPTION

The XR20V2172[1] (V2172) is a high performance two channel universal asynchronous receiver and transmitter (UART) with 64 byte TX and RX FIFOs, a selectable I^{2}C/SPI slave interface and RS232 transceiver. The V2172 operates from 3.3 to 5.5 volts. The enhanced features in the V2172 include a programmable fractional baud rate generator, an 8X and 4X sampling rate that allows for a maximum baud rate of 1 Mbps at 3.3V. The standard features include 16 selectable TX and RX FIFO trigger levels, automatic hardware (RTS/CTS) and software (Xon/Xoff) flow control, and a complete modem interface. Onboard registers provide the user with operational status and data error flags. An internal loopback capability allows system diagnostics. The V2172 is available in the 64-pin QFN.

NOTE: *1 Covered by U.S. Patent #5,649,122*

APPLICATIONS

- Portable Appliances
- Battery-Operated Devices
- Cellular Data Devices
- Factory Automation and Process Controls

FEATURES

- Selectable I^{2}C/SPI Interface
- SPI clock frequency up to 18 MHz
- Meets true EIA/TIA-232-F Standards from +3.3V to +5.5V operation
- Data rate up to 1 Mbps
- 45us sleep mode exit (charge pump to full power)
- ESD protection for RS-232 I/O pins at
  - +/-15kV - Human Body Model
  - +/-15kV - IEC 61000-4-2, Air-Gap Discharge
  - +/- 8kV - IEC 61000-4-2, Contact Discharge
- Full-featured UART
  - Fractional Baud Rate Generator
  - Transmit and Receive FIFOs of 64 bytes
  - 16 Selectable TX and RX FIFO Trigger Levels
  - Automatic Hardware (RTS/CTS) Flow Control
  - Automatic Software (Xon/Xoff) Flow Control
  - Halt and Resume Transmission Control
  - Automatic sleep mode
  - General Purpose I/Os
  - Full modem interface
- 64-QFN packages

FIGURE 1. XR20V2172 BLOCK DIAGRAM

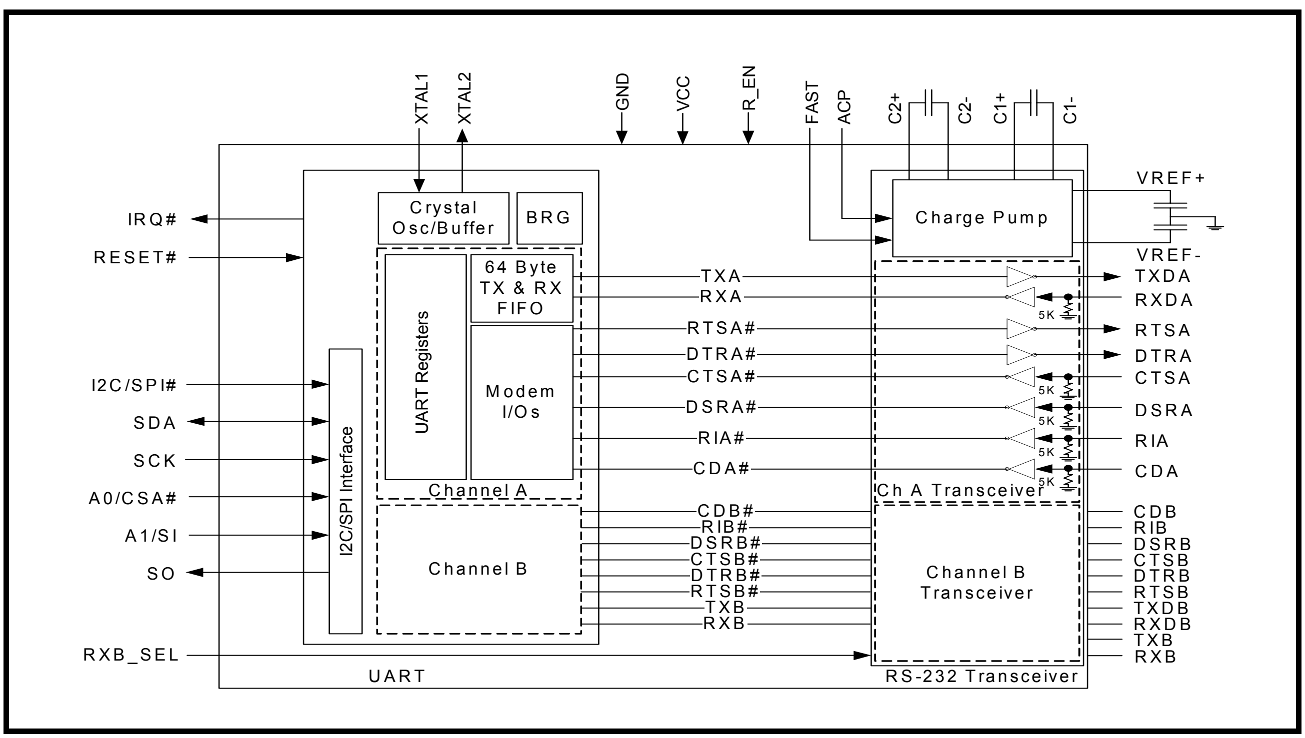
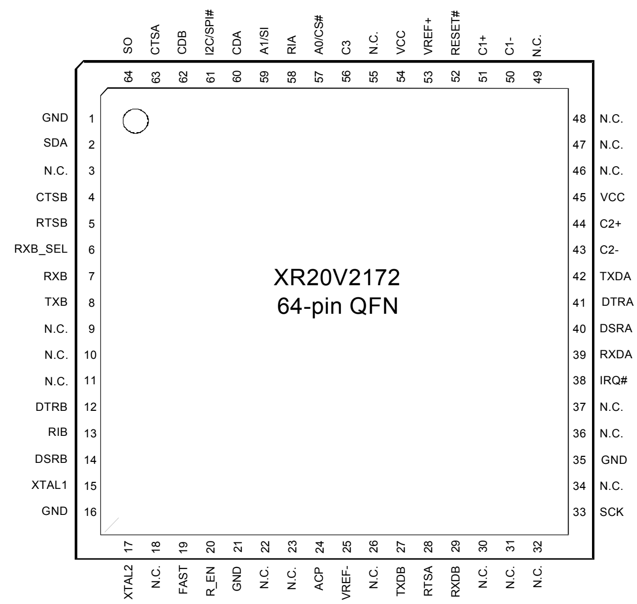


FIGURE 2. PIN OUT ASSIGNMENT



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR20V2172IL64-F	64-pin QFN	-40°C to +85°C	Active
XR20V2172IL64TR-F	64-pin QFN	-40°C to +85°C	Active

NOTE: **TR = Tape and Reel, F = Green / RoHS**

PIN DESCRIPTIONS

Pin Description

NAME	64-QFN PIN #	TYPE	DESCRIPTION
I2C (SPI) INTERFACE			
I^2C/SPI#	61	I/O	I^2C-bus or SPI interface select. I^2C-bus interface is selected if this pin is HIGH. SPI interface is selected if this pin is LOW. This pin is not 5V tolerant.
SDA	2	I/O	I^2C-bus data input/output (open-drain). If SPI configuration is selected, then this pin is undefined and must be connected to VCC. This pin is not 5V tolerant.
SCK	33	I	I^2C-bus or SPI serial input clock. When the I^2C-bus interface is selected, the serial clock idles HIGH. When the SPI interface is selected, the serial clock idles LOW. This pin is not 5V tolerant.
A0/ CS#	57	I	I^2C-bus device address select A0 or SPI chip select. If I^2C-bus configuration is selected, this pin along with the A1 pin allows user to change the device's base address. If SPI configuration is selected, this pin is the SPI chip select pin (Schmitt-trigger, active LOW). This pin is not 5V tolerant.
A1/ SI	59	I	I^2C-bus device address select A1 or SPI data input pin. If I^2C-bus onfiguration is selected, this pin along with A0 pin allows user to change the device's base address. If SPI configuration is selected, this pin is the SPI data input pin. This pin is not 5V tolerant.
SO	64	O	SPI data output pin. If SPI configuration is selected then this pin is a three-stateable output pin. If I^2C-bus configuration is selected, this pin is undefined and must be left unconnected.
IRQ#	38	OD	Interrupt output (open-drain, active LOW).
RESET#	52	I	Reset (active LOW) - A longer than 40 ns LOW pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be idle and the receiver input will be ignored. This pin is not 5V tolerant.
SERIAL I/O INTERFACE (CMOS/TTL Voltage Levels)			
RXB	7	I	UART Channel B Receive Data. This pin can be used to communicate with external IR or RS-232 transceiver. This pin is not 5V tolerant.
TXB	8	O	UART Channel B Transmit Data. This pin can be used to communicate with external IR or RS-232 transceiver.
MODEM OR SERIAL I/O INTERFACE (EIA-232/RS-232 Voltage Levels)			
RXDA RXDB	39 29	I	UART Receive Data. UART receive data input must idle LOW (< 1.5V). This input has an internal pull-down resistor and can be left unconnected when not used.
TXDA TXDB	42 27	O	UART Transmit Data. The TX signal will be LOW (< 1.5V) during reset or idle (no data).
RTSA RTSB	28 5	O	UART Request-to-Send. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1] and IER[6].
CTSA CTSB	63 4	I	UART Clear-to-Send. It can be used for auto CTS flow control, see EFR[7], MSR[4] and IER[7]. This input has an internal pull-down resistor and can be left unconnected when not used.

Pin Description

Name	64-QFN Pin #	Type	Description
DTRA DTRB	41 12	O	UART Data-Terminal-Ready. See MCR[0].
DSRA DSRB	40 14	I	UART Data-Set-Ready. This input has an internal pull-down resistor and can be left unconnected when not used. See MSR[5].
CDA CDB	60 62	I	UART Carrier-Detect. This input has an internal pull-down resistor and can be left unconnected when not used. See MSR[7].
RIA RIB	58 13	I	UART Ring-Indicator. This input has an internal pull-down resistor and can be left unconnected when not used. See MSR[6].
Ancillary signals (CMOS/TTL Voltage Levels)			
XTAL1	15	I	Crystal or external clock input. This pin is not 5V tolerant.
XTAL2	17	O	Crystal or buffered clock output.
ACP	24	I	Autosleep for Charge Pump (active HIGH). When this pin is HIGH, the charge pump is shut off if the V2172 is already in partial sleep mode, i.e. the crystal oscillator is stopped. This pin is 5V tolerant.
FAST	19	I	When FAST is HIGH, the maximum serial data rate is 1 Mbps. When FAST is LOW, the maximum serial data rate is 250 Kbps. This pin is 5V tolerant.
R_EN	20	I	When the supply voltage is < 3.6V, connect R_EN to VCC. When the supply voltage is > 3.6V, connect R_EN to GND. This pin is 5V tolerant.
RXB_SEL	6	I	When RXB_SEL is HIGH, RXB is the receive data input. When RXB_SEL is LOW, RXDB is the receive data input. This pin is 5V tolerant.
C2+ C2-	44 43	-	Charge pump capacitors. As shown in **Figure 1**, a 0.1 uF capacitor should be placed between these 2 pins.
C1+ C1-	51 50	-	Charge pump capacitors. As shown in **Figure 1**, a 0.1 uF capacitor should be placed between these 2 pins.
C3	56	-	When the supply voltage is 3.3 V, C3 should be connected to VCC. When the supply voltage is 5 V, C3 should be connected to a 1 uF capacitor to GND.
VREF-	25	Pwr	-5.0V generated by the charge pump.
VREF+	53	Pwr	+5.0V generated by the charge pump.
GND	1, 16, 21, 35	Pwr	Power supply common, ground.
VCC	45, 54	Pwr	3.3 to 5.5V power supply.

Pin Description

NAME	64-QFN PIN #	TYPE	DESCRIPTION
-	PAD	Pwr	The center pad on the backside of the QFN packages is metallic and is not electrically connected to anything inside the device. It must be soldered on to the PCB and may be optionally connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.
NC	3, 9, 10, 11, 18, 22, 23, 26, 30, 31, 32, 34, 36, 37, 46, 47, 48, 49, 55	-	No Connection.

NOTE: **Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.** *For CMOS/TTL Voltage levels, 'LOW' indicates a voltage in the range 0V to VIL and 'HIGH" indicates a voltage in the range VIH to VCC. For RS-232 input voltage levels, 'LOW' is any voltage < -3V and 'HIGH' is any voltage > 3V. For RS-232 output voltage levels, 'LOW' is any voltage < -5V and 'HIGH' is any voltage > 5V.*

1.0 PRODUCT DESCRIPTION

The XR20V2172 (V2172) integrates a selectable I^2C/SPI bus interface with an enhanced two channel Universal Asynchronous Receiver and Transmitter (UART) and an RS-232 Transceiver. The configuration register set is 16550 UART compatible for control, status and data transfer. Additionally, each channel of the V2172 has 64-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, programmable fractional baud rate generator with a prescaler of divide by 1 or 4, data rate up to 1 Mbps, while meeting all EIA RS-232F specifications. Additionally, the V2172 includes the ACP pin with which the user can shut down the charge pump for the RS-232 drivers when the V2172 is already in sleep mode. The XR20V2172 is a 3.3 to 5.5V device. The V2172 is fabricated with an advanced CMOS process.

Enhanced Features

The V2172 UART provides a solution that supports 64 bytes of transmit and receive FIFO memory, instead of 16 bytes in the industry standard 16C550. The V2172 is designed to work with low supply voltage and high performance data communication systems, that require fast data processing time. Increased performance is realized in the V2172 by the larger transmit and receive FIFOs, FIFO trigger level control and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the 16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2 Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 64 byte FIFO in the V2172, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU’s bandwidth requirement, increases performance, and reduces power consumption. Finally, since the V2172 includes an RS-232 transceiver and a full-modem interface, it can be connected to an RS-232 serial cable directly.

Data Rate

The V2172 is capable of operation up to 1 Mbps data rate using the 16X, 8X or 4X internal sampling clock rate. The UART section can operate at much higher speeds, but the speed of the RS-232 transceiver is limited to 1Mbps beyond which the V2172 cannot comply with the EIA/TIA-232 electrical characteristics. The device can operate either with a crystal on pins XTAL1 and XTAL2, or external clock source on XTAL1 pin.

RS-232 Interface

The V2172 includes RS-232 drivers/receivers for the modem interface. This feature eliminates the need for an external RS-232 transceiver. The charge pump provides output voltages of +5V and -5V for its drivers over the 3.3V to 3.63V power supply voltage range. The serial outputs TXD swing between -5V (inactive) and +5V (active) RS-232 voltage levels. The serial inputs RXD are RS-232 receivers and can take any voltage swing from -15V to +15V. The receivers are always active, even in Sleep mode. The RS-232 drivers guarantee a data rate of 1 Mbps even when fully loaded with 3Kohm in parallel with 1000pF load.

All RS-232 drivers and receivers are protected to ±15kV using the Human Body Model ground combination, ±8kV using IEC 61000-4-2 Contact Discharge, and ±15kV using IEC 61000-4-2 Air-Gap Discharge. For more information, send an e-mail to uarttechsupport@exar.com.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The V2172 can operate with either an I^{2}C-bus interface or an SPI interface. The CPU interface is selected via the I2C/SPI# input pin.

2.1.1 I^{2}C-bus Interface

The I^{2}C-bus interface is compliant with the Standard-mode and Fast-mode I^{2}C-bus specifications. The I^{2}C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the Standard-mode, the serial clock and serial data can go up to 100 kbps and in the Fast-mode, the serial clock and serial data can go up to 400 kbps. The first byte sent by an I^{2}C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The V2172 responds to each write with an acknowledge (SDA driven LOW by V2172 for one clock cycle when SCL is HIGH). If the TX FIFO is full, the V2172 will respond with a negative acknowledge (SDA driven HIGH by V2172 for one clock cycle when SCL is HIGH) when the CPU tries to write to the TX FIFO. The last byte sent by an I^{2}C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See Figures 3 - 5 below. For complete details, see the I^{2}C-bus specifications.

FIGURE 3. I^{2}C START AND STOP CONDITIONS

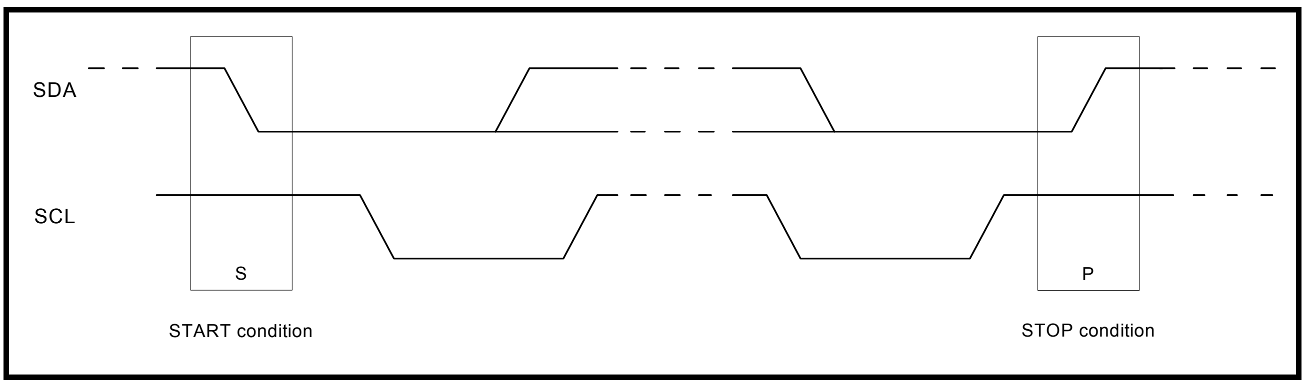


FIGURE 4. MASTER WRITES TO SLAVE (V2172)

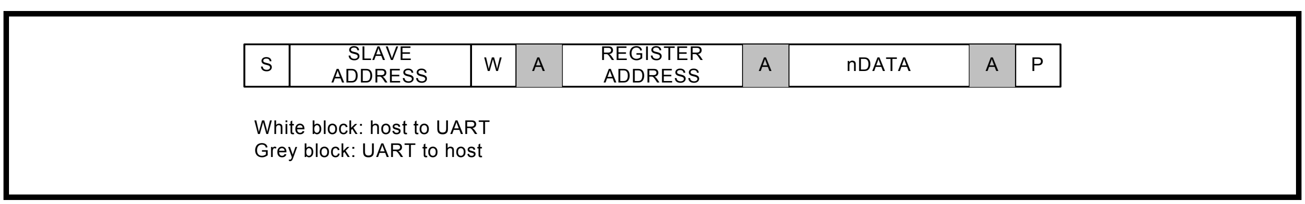
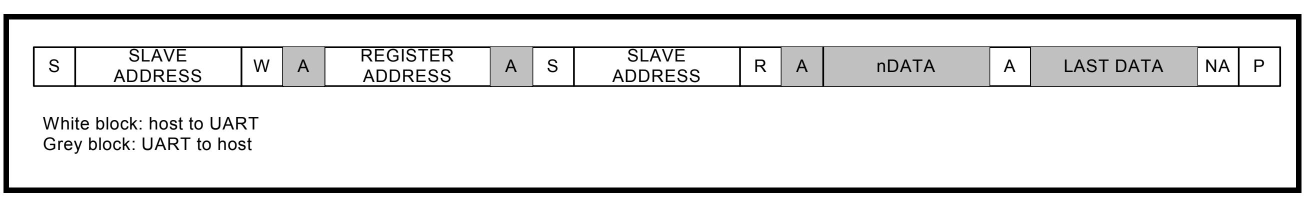


FIGURE 5. MASTER READS FROM SLAVE (V2172)



2.2 I^2C-bus Addressing

There could be many devices on the I^2C-bus. To distinguish itself from the other devices on the I^2C-bus, there are eight possible slave addresses that can be selected for the V2172 using the A1 and A0 address lines. Table 1 below shows the different addresses that can be selected. Note that there are two different ways to select each I^2C address.

TABLE 1: XR20V2172 I^2C ADDRESS MAP

A1	A0	I^2C ADDRESS
VCC	VCC	0x60 (0110 000X)
VCC	GND	0x62 (0110 001X)
VCC	SCL	0x64 (0110 010X)
VCC	SDA	0x66 (0110 011X)
GND	VCC	0x68 (0110 100X)
GND	GND	0x6A (0110 101X)
GND	SCL	0x6C (0110 110X)
GND	SDA	0x6E (0110 111X)
SCL	VCC	0x60 (0110 000X)
SCL	GND	0x62 (0110 001X)
SCL	SCL	0x64 (0110 010X)
SCL	SDA	0x66 (0110 011X)
SDA	VCC	0x68 (0110 100X)
SDA	GND	0x6A (0110 101X)
SDA	SCL	0x6C (0110 110X)
SDA	SDA	0x6E (0110 111X)

An I^2C sub-address is sent by the I^2C master following the slave address. The sub-address contains the UART register address being accessed. A read or write transaction is determined by bit-0 of the slave address. If bit-0 is’0’, then it is a write transaction. If bit-0 is ’1’, then it is a read transaction. Table 2 below lists the functions of the bits in the I^2C sub-address.

TABLE 2: I^2C SUB-ADDRESS

BIT	FUNCTION
7	Reserved
6:3	UART Internal Register Address A3:A0
2:1	UART Channel Select ’00’ = UART Channel A ’01’ = UART Channel B
0	Reserved

After the last read or write transaction, the I^2C-bus master will set the SCL signal back to its idle state (HIGH).

2.2.1 SPI Bus Interface

The SPI interface consists of four lines: serial clock (SCL), chip select (CS#), slave output (SO) and slave input (SI). The serial clock, slave output and slave input can be as fast as 18 MHz at 3.3V. To access the device in the SPI mode, the CS# signal for the V2172 is asserted by the SPI master, then the SPI master starts toggling the SCL signal with the appropriate transaction information. The first byte sent by the SPI master includes whether it is a read or write transaction and the UART register being accessed. See **Table 3** below.

TABLE 3: SPI FIRST BYTE FORMAT

BIT	FUNCTION
7	Read/Write# Logic 1 = Read Logic 0 = Write
6:3	UART Internal Register Address A3:A0
2:1	UART Channel Select '00' = UART Channel A '01' = UART Channel B
0	Reserved

After the last read or write transaction, the SPI master will set the SCL signal back to its idle state (LOW).

2.3 Device Reset

The RESET# input resets the internal registers and the serial interface outputs in the UART to its default state (see **Table 16**). An active low pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Internal Registers

The V2172 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to the industry standard ST16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM/DLD), and a user accessible Scratchpad Register (SPR).

Beyond the general 16C550 features and capabilities, the V2172 offers enhanced feature registers (EFR, Xon/Xoff 1, Xon/Xoff 2, TCR, TLR, TXLVL, RXLVL, IODir, IOState, IOIntEna, IOControl, EFCR and DLD) that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, TX and RX FIFO level counters, and programmable FIFO trigger level control. All the register functions are discussed in full detail later in **"Section 3.0, UART Internal Registers" on page 21**.

2.5 IRQ# Output

The IRQ# interrupt output changes according to the operating mode and enhanced features setup. **Table 4 and 5** summarize the operating behavior for the transmitter and receiver.

TABLE 4: IRQ# PIN OPERATION FOR TRANSMITTER

	Auto RS485 Mode	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
IRQ# Pin	NO	HIGH = a byte in THR LOW = THR empty	HIGH = FIFO above trigger level LOW = FIFO below trigger level or FIFO empty
IRQ# Pin	YES	HIGH = a byte in THR LOW = transmitter empty	HIGH = FIFO above trigger level LOW = FIFO below trigger level or transmitter empty

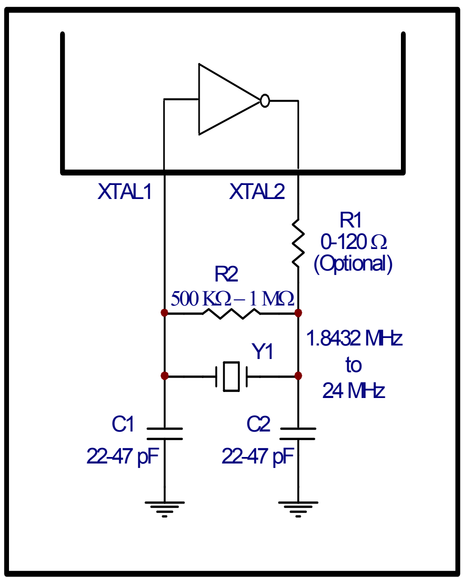
TABLE 5: IRQ# PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
IRQ# Pin	HIGH = no data LOW = 1 byte	HIGH = FIFO below trigger level LOW = FIFO above trigger level

2.6 Crystal Oscillator or External Clock Input

The V2172 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. Please note that the input XTAL1 is not 5V tolerant and so the maximum at the pin should be VCC. For programming details, see "**"Section 2.7, Programmable Baud Rate Generator with Fractional Divisor" on page 10**."

FIGURE 6. TYPICAL OSCILLATOR CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100 ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see **Figure 6**). The programmable Baud Rate Generator is capable of operating with a crystal oscillator frequency of up to 24 MHz. Although the V2172 can accept an external clock of up to 64MHz, the maximum data rate supported by the RS-232 drivers is 250Kbps. For further reading on the oscillator circuit please see the Application Note DAN108 on the EXAR web site at **http://www.exar.com.**

2.7 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X, 8X or 4X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to the value of ’1’ (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon power-up. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the dvisior. The four lower bits of the DLD are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. Table 6 shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in Table 6. At 8X sampling rate, these data rates would double and at 4X sampling rate, these data rates would quadruple. Also, when using 8X sampling mode, the bit time will have a jitter of ± 1/16 whenever the DLD is non-zero and is an odd number. When using 4X sampling mode, the bit time will have a jitter of ± 1/8 whenever DLD is non-zero, odd and not a multiple of 4. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal)=(XTAL1 clock frequency / prescaler) /(serial data rate x 16), with 16X mode, **DLD[5:4]=’00’**
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 8), with 8X mode, **DLD[5:4] = ’01’**
Required Divisor (decimal)= (XTAL1 clock frequency / prescaler / (serial data rate x 4), with 4X mode, **DLD[5:4] = ’10’**

The closest divisor that is obtainable in the V2172 can be calculated using the following formula:

ROUND((Required Divisor - TRUNC(Required Divisor))*16)/16 + TRUNC(Required Divisor), where
DLM = TRUNC(Required Divisor) >> 8 DLL = TRUNC(Required Divisor) & 0xFF DLD = ROUND((Required Divisor-TRUNC(Required Divisor))*16)

In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value ’A’ by ’B’ number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 7. BAUD RATE GENERATOR

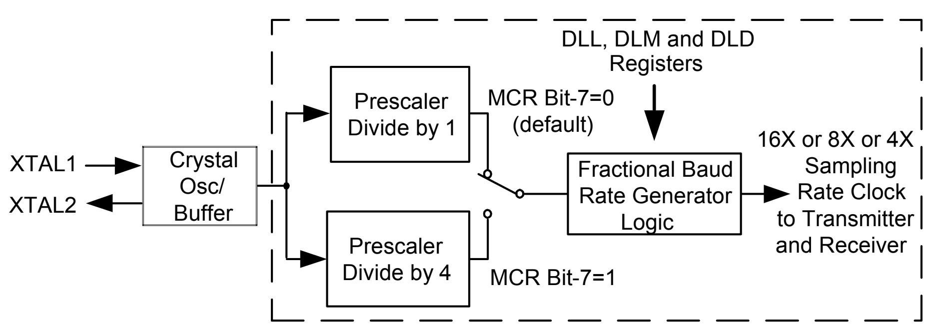


TABLE 6: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	DIVISOR FOR 16x Clock (Decimal)	DIVISOR OBTAINABLE IN V2172	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DLD PROGRAM VALUE (HEX)	DATA ERROR RATE (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0

2.8 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X/4X internal clock. A bit time is 16 (8 if 8X or 4 if 4X) clock periods (see DLD[5:4]). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR[6:5]).

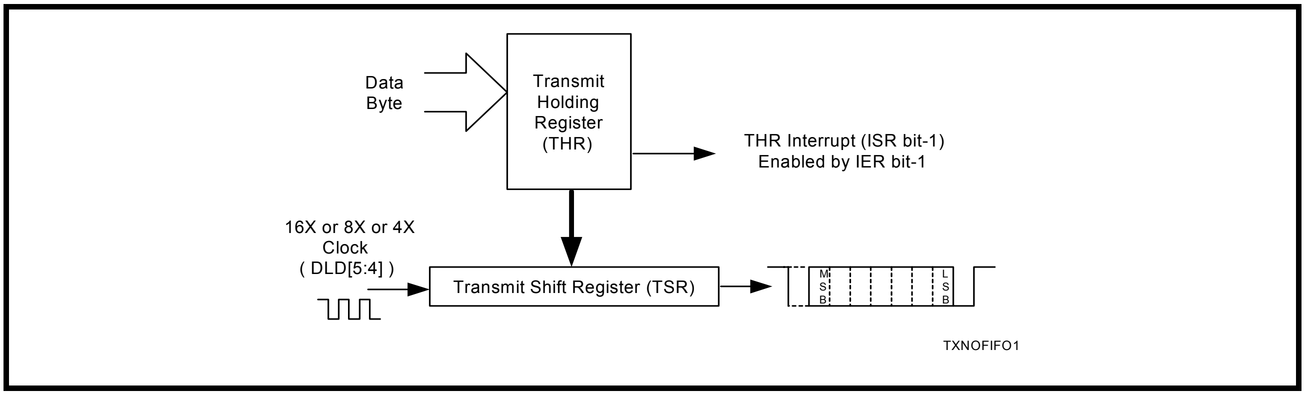
2.8.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.8.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

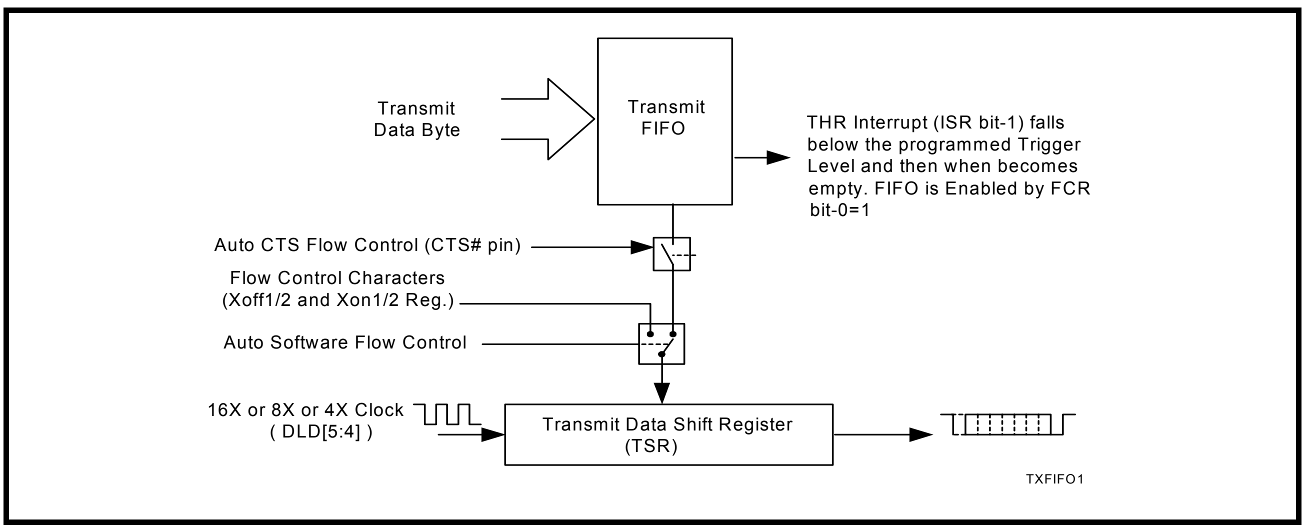
FIGURE 8. TRANSMITTER OPERATION IN NON-FIFO MODE



2.8.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 9. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.9 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X/4X clock (DLD [5:4]) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X/4X clock rate. After 8 clocks (or 4 if 8X or 2 if 4X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.9.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 10. RECEIVER OPERATION IN NON-FIFO MODE

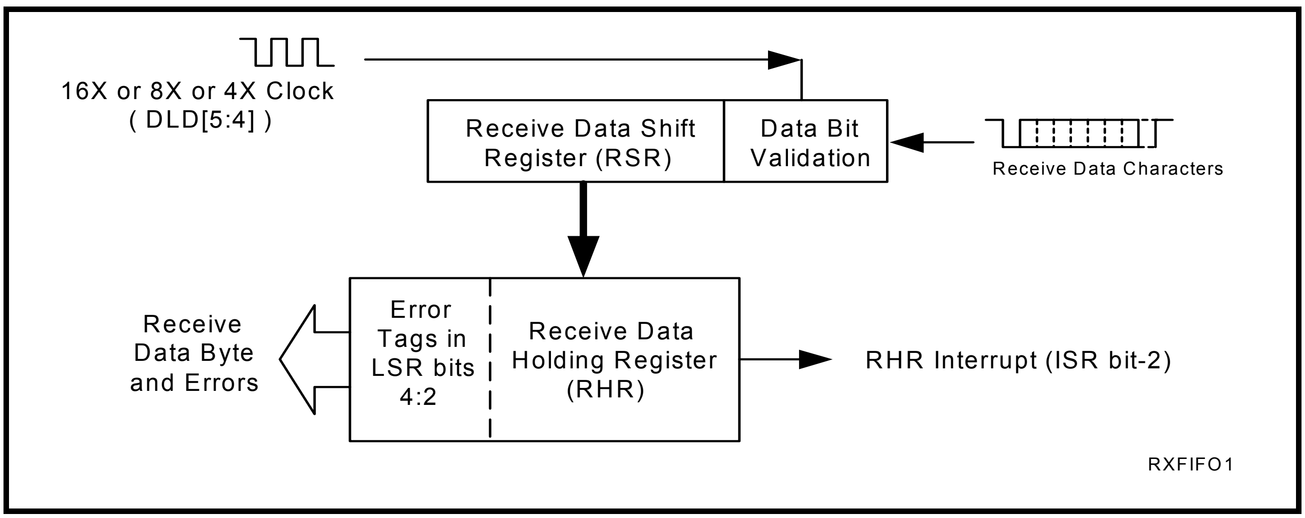
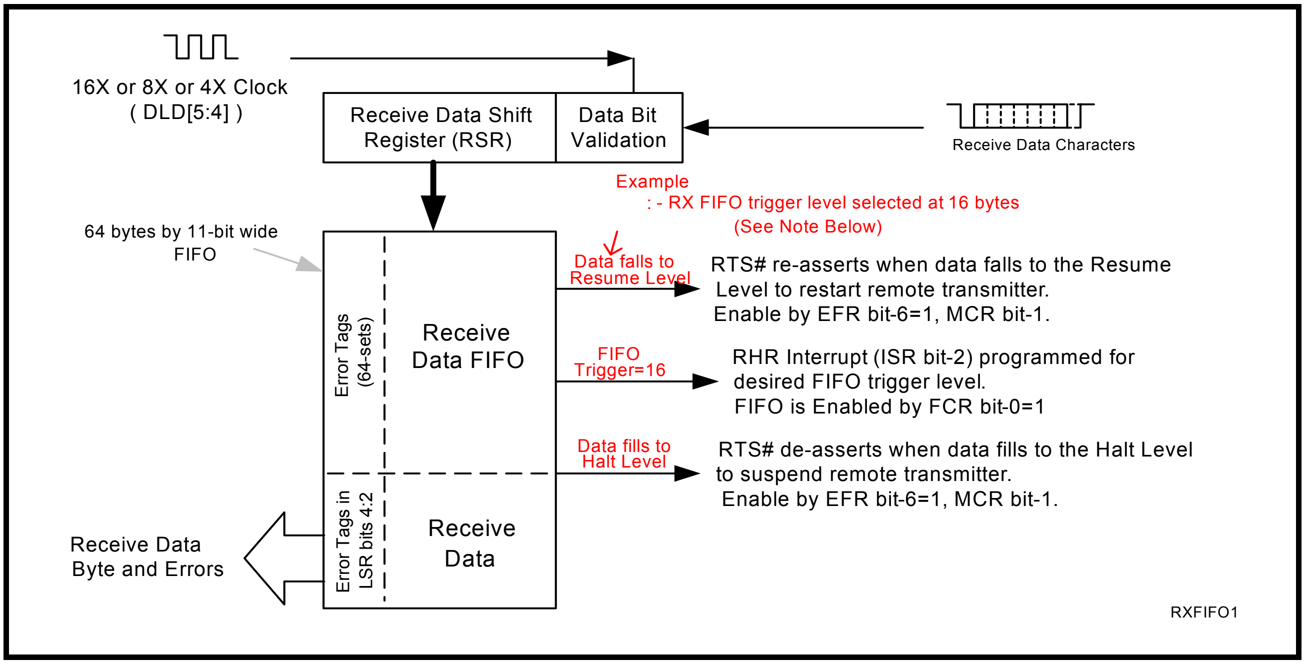


FIGURE 11. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.10 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see **Figure 12**):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.11 Auto RTS Halt and Resume

The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches the Halt Level (TCR[3:0]). The RTS# pin will return LOW after the RX FIFO is unloaded to the Resume Level (TCR[7:4]). Under these conditions, the V2172 will continue to accept data if the remote UART continues to transmit data. It is the responsibility of the user to ensure that the Halt Level is greater than the Resume Level. If interrupts are used, it is recommended that Halt Level > RX Trigger Level > Resume Level. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On).

2.12 Auto CTS Flow Control

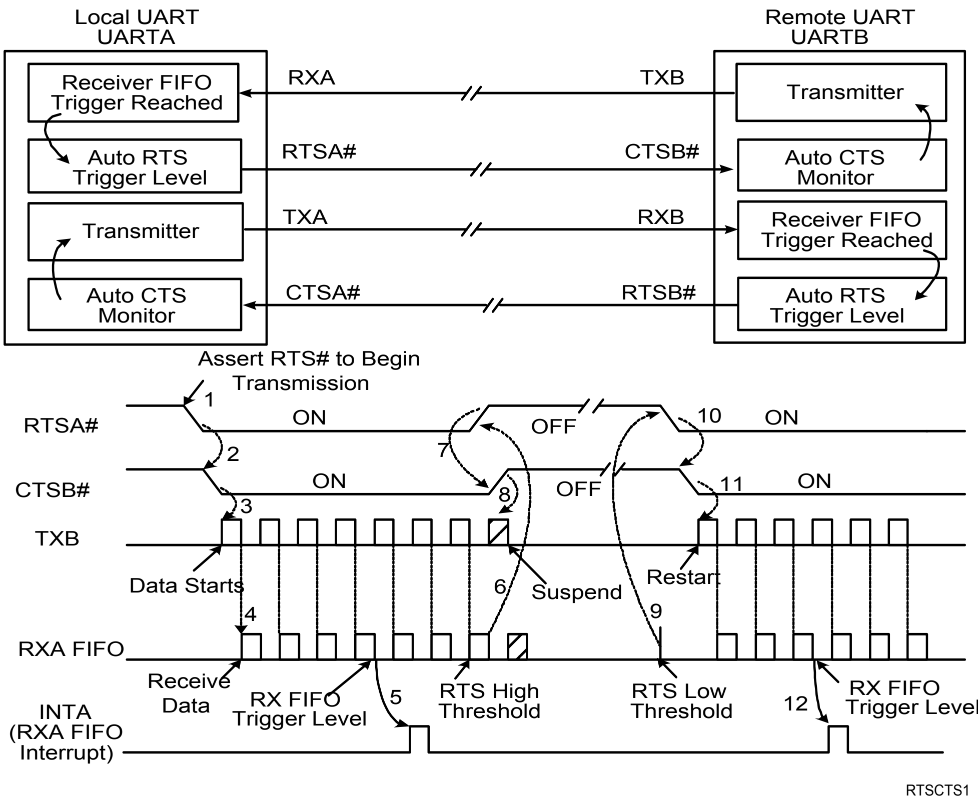
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see **Figure 12**):

- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 12. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.13 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (**See Table 15**), the V2172 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the V2172 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the V2172 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the V2172 will resume operation and clear the flags (ISR bit-4).

Upon power-up, the contents of the Xon/Xoff 8-bit flow control registers to 0x00. The user can write any Xon/Xoff value desired for software flow control. These registers are not reset by a hardware or software reset. Different conditions can be set to detect Xon/Xoff characters (**See Table 15**) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the V2172 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the V2172 automatically sends the Xoff-1,2 via the serial TX output to the remote modem when the RX FIFO reaches the Halt Level (TCR[3:0]). To clear this condition, the V2172 will transmit the programmed Xon-1,2 characters as soon as RX FIFO falls down to the Resume Level.

2.14 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The V2172 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison.

2.15 Sleep Mode with Auto Wake-Up

The V2172 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used. In the Partial Sleep mode, the internal oscillator of the UART or charge pump of the RS-232 transceiver is turned off to reduce the power consumption. In the Full Sleep mode, both the oscillator and the charge pump are turned off.

2.15.1 Partial Sleep Mode

There are two different partial sleep modes. In the first mode, the UART is in sleep mode and the charge pump is active. In the other mode, the UART is still active but the charge pump is turned off.

2.15.1.1 UART in sleep mode, RS-232 transceiver active

If the ACP pin is LOW, then the charge pump for the RS-232 transceiver will always be active. But the UART portion in the V2172 can still enter sleep mode if all of these conditions are satisfied for both channels:

- no interrupts pending (ISR bit-0 = 1)
- the 16-bit divisor programmed in DLM and DLL registers is a non-zero value
- sleep mode is enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RXD input pin is idling LOW

The V2172 UART portion stops its crystal oscillator to conserve power in this mode. The user can check the XTAL2 pin for no clock output as an indication that the device has entered the partial sleep mode.

The UART portion in the V2172 resumes normal operation or active mode by any of the following:

- a receive data start bit transition on the RXD input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the UART portion of V2172 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the UART portion of V2172 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending. The UART portion of V2172 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

2.15.1.2 UART active, charge pump of RS-232 transceiver shut down

If the ACP pin is HIGH and the UART portion of the V2172 is not in sleep mode, then the charge pump will automatically shut down to conserve power if the following conditions are true:

- no activity on the TXD output signal
- modem input signals (RX) are LOW
- modem inputs have been idle for approximately 30 seconds

When these conditions are satisfied, the V2172 shuts down the charge pump and tri-states the RS-232 drivers to conserve power. In this mode, the RS-232 receivers are fully active and the internal registers of the V2172 can be accessed. The time for the charge pump to resume normal operation after exiting the sleep mode is typically 45µs. It will wake up by any of the following:

- a receive data start bit transition on the RXD input (LOW to HIGH)
- a data byte is loaded to the transmitter, THR or FIFO
- a LOW to HIGH transition on any of the modem or general purpose serial inputs

Because the receivers are fully active when the charge pump is turned off, any data received will be transferred to/from the UART without any issues.

2.15.2 Full Sleep Mode

In full sleep mode, the V2172 shuts down the charge pump and the internal oscillator. The V2172 enters the full sleep mode if the following conditions are satisfied:

- the UART portion of the V2172 is already in sleep mode (no output on XTAL2)
- the ACP (Autosleep for Charge Pump) pin is HIGH

When these conditions are satisfied, both the UART and the charge pump will be in the sleep mode. In this mode, the RS-232 receivers are fully active and the internal registers of the V2172 can be accessed. The V2172 exits the full sleep mode if either the ACP pin becomes LOW or the internal oscillator starts up. The time for the charge pump to resume normal operation after exiting the full sleep mode is typically 45µs.

If the serial clock, serial data, and modem input lines remain steady when the V2172 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 39.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate. Also, it is important to keep RX input idling HIGH or “marking” condition during sleep mode to avoid receiving a “break” condition upon the restart. This may occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the designer can use a 47k-100k ohm pull-up resistor on the RX input pin.

2.16 Infrared Mode (UART Channel B Only)

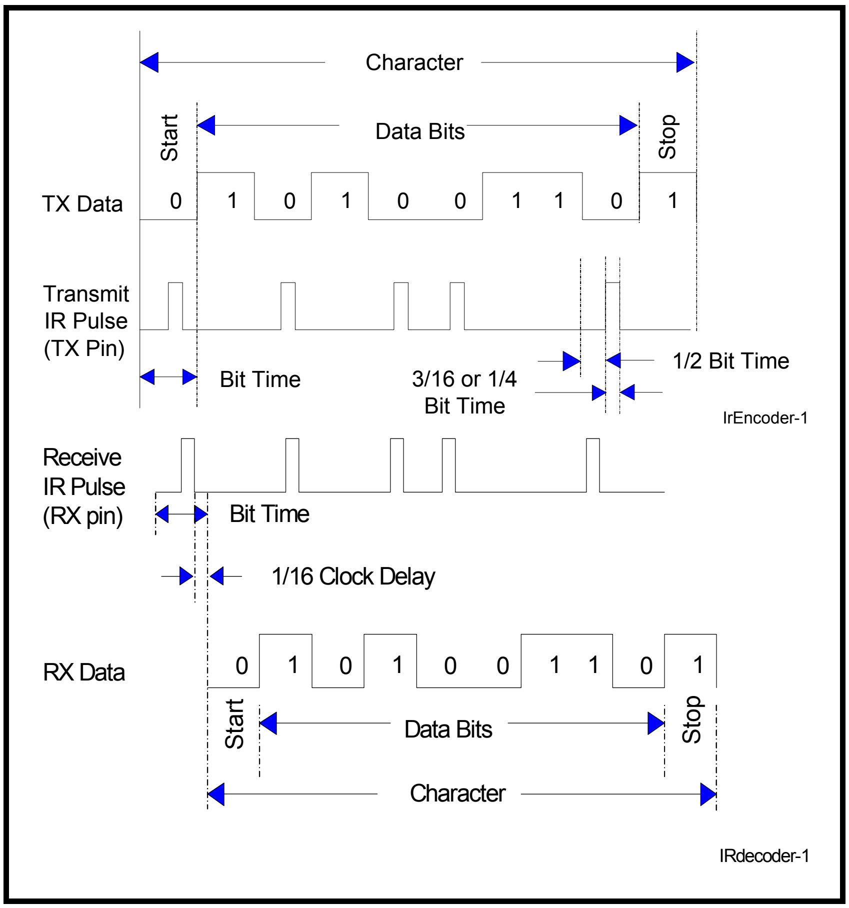
The L402 includes an infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0 and 1.1. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream with a data rate up to 115.2 Kbps. For the IrDA 1.1 standard, the infrared encoder sends out a 1/4 of a bit time wide HIGH-pulse for each "0" bit in the transmit data stream with a data rate up to 1.152 Mbps. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 13** below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. With this bit enabled, the infrared encoder and decoder is compatible to the IrDA 1.0 standard. For the infrared encoder and decoder to be compatible to the IrDA 1.1 standard, EFCR bit-7 will also need to be set to a ’1’. When the infrared feature is enabled, the transmit data output, TX, idles LOW. Likewise, the RX input also idles LOW, see **Figure 13**.

The wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream.

The Infrared Mode can only be used with channel B of the L402 using the TXB output and the RXB input pins.

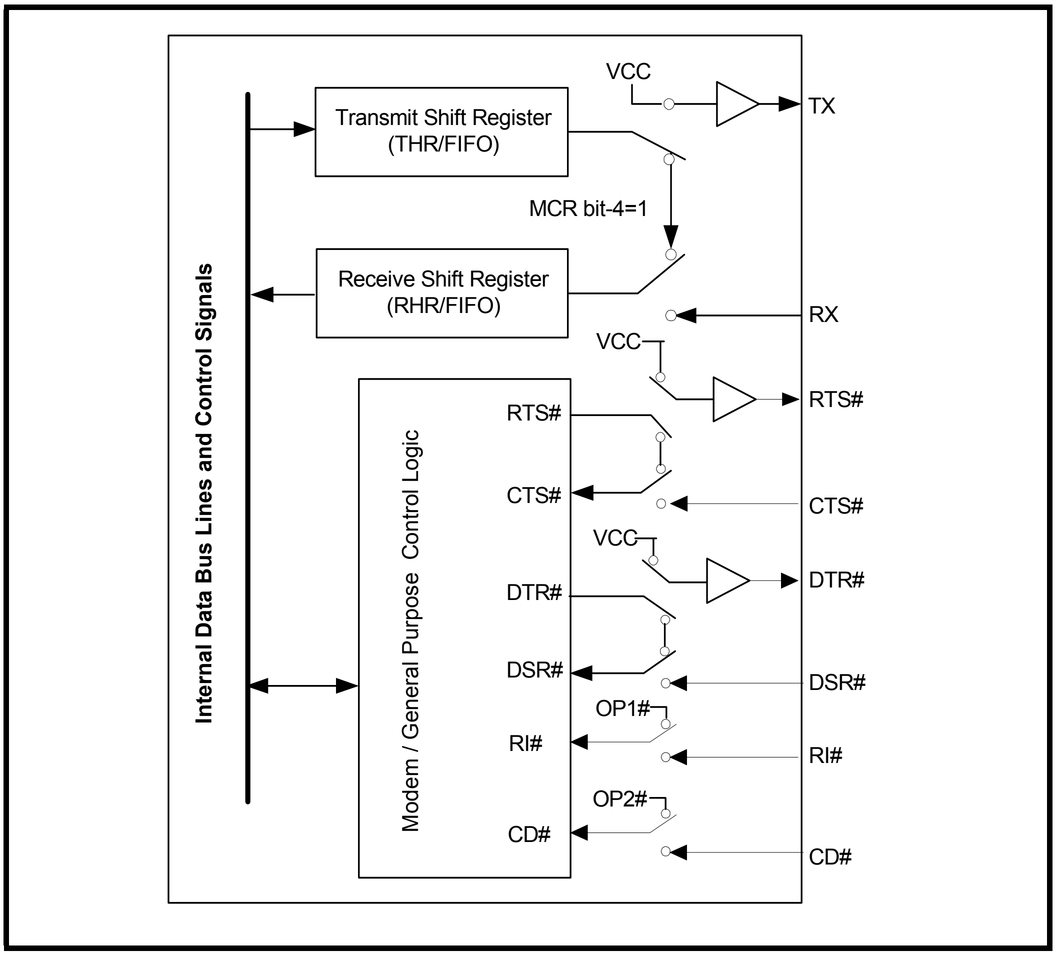
FIGURE 13. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.17 Internal Loopback

The V2172 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 14 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held while the CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input pin must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal. Also, auto RTS/CTS flow control is not supported during internal loopback.

FIGURE 14. INTERNAL LOOP BACK



3.0 UART INTERNAL REGISTERS

The complete register set is shown below in Table 7 and Table 8.

TABLE 7: UART INTERNAL REGISTER ADDRESSES

ADDRESS	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0X00	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0X00	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0X01	DLM - Divisor MSB	Read/Write	
0X02	DLD - Divisor Fractional	Read/Write	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1
0X01	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0X02	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0X03	LCR - Line Control Register	Read/Write	
0X04	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
0X05	LSR - Line Status Register	Read-only	
0X06	MSR - Modem Status Register	Read-only	See Table 12
0X07	SPR - Scratch Pad Register	Read/Write	See Table 13
0X06	TCR - Transmission Control Register	Read/Write	See Table 12
0X07	TLR - Trigger Level Register	Read/Write	See Table 13
0X08	TXLVL - Transmit FIFO Level	Read-only	LCR[7] = 0
0x09	RXLVL - Receive FIFO Level	Read-only	
0x0A	IODir - GPIO Direction Control Register	Read/Write	
0x0B	IOState - GPIO State Register	Read/Write	
0x0C	IOIntEna - GPIO Interrupt Enable Register	Read/Write	
0x0D	Reserved	-	
0x0E	IOControl - GPIO Control Register	Read/Write	
0x0F	EFCR - Extra Features Control Register	Read/Write	
0x02	EFR - Enhanced Function Register	Read/Write	LCR = 0xBF
0x04	Xon-1 - Xon Character 1	Read/Write	
0x05	Xon-2 - Xon Character 2	Read/Write	
0x06	Xoff-1 - Xoff Character 1	Read/Write	
0x07	Xoff-2 - Xoff Character 2	Read/Write	

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDR	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0x00	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0x00	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x01	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0x02	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0x02	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	0	TXFIFO Reset	RX FIFO Reset	FIFOs Enable	
0x03	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
0x04	MCR	RD/WR	0/ Clock Pres-caler Select	0/ Enable IR Mode (Ch B Only)	0/ XonAny	Internal Lopback Enable	OP2#	0/ Enable TCR and TLR	RTS# Output Control	DTR# Output Control	LCR≠0xBF
0x05	LSR	RD	RXFIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
0x06	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	See Table 12
0x07	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	See Table 13
0x06	TCR	RD/WR	Resume Bit-3	Resume Bit-2	Resume Bit-1	Resume Bit-0	Halt Bit-3	Halt Bit-2	Halt Bit-1	Halt Bit-0	See Table 12
0x07	TLR	RD/WR	RX Trig Bit-3	RX Trig Bit-2	RX Trig Bit-1	RX Trig Bit-0	TX Trig Bit-3	TX Trig Bit-2	TX Trig Bit-1	TX Trig Bit-0	See Table 13
0x08	TXLVL	RD/WR	0	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x09	RXLVL	RD/WR	0	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDR	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
0x0A	IODir	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0B	IOState	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0C	IOIntEna	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x0D	reserved	-	0	0	0	0	0	0	0	0	
0x0E	IOControl	RD/WR	0	0	0	0	UART SW Reset	GPIO or Modem IO Ch B	GPIO or Modem IO Ch A	IOLatch	
0x0F	EFCR	RD/WR	Fast IR Mode (Ch B Only)	0	0	0	0	TX Disable	RX Disable	0	
Baud Rate Generator Divisor											
0x00	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR≠0xBF
0x01	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x02	DLD	RD/WR	Bit-7	Bit-6	4X Mode	8X Mode	Frac-tional Divisor Bit-3	Frac-tional Divisor Bit-2	Frac-tional Divisor Bit-1	Frac-tional Divisor Bit-0	LCR[7]=1 LCR≠0xBF EFR[4]=1
Enhanced Registers											
0x02	EFR	RD/WR	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5], DLD	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	LCR=0xBF
0x04	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x05	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x06	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0x07	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

SEE"RECEIVER" ON PAGE 14.

4.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 12.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR20V2172 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when spaces in the FIFO is above the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3, 4 or 7 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bit-7 is set if any character in the RX FIFO has a parity or framing error, or is a break character. LSR[4:2] always show the error status for the received character available for reading from the RX FIFO. If IER[2] = 1, an LSR interrupt will be generated as long as LSR[7] = 1, ie. the RX FIFO contains at lease one character with an error.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from low to high.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from low to high.

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 9, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3, 4 and 7.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- GPIO is when any of the GPIO inputs toggle.
- Receive Xoff/Special character is by detection of a Xoff or Special character.
- CTS# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS flow control.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by reading all characters with errors out of the RX FIFO.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- GPIO interrupt is cleared by reading the IOState register.
- Xoff interrupt is cleared when Xon character(s) is received.