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GENERAL DESCRIPTION

The XR28V384 (V384) is a quad Universal Asynchronous Receiver and Transmitter (UART) for the Intel Low Pin Count (LPC) bus interface. This device can replace or supplement a Super I/O device to add additional serial ports to the system.

The V384 UARTs support any 16-bit I/O address supported by the system. The register set is based on the industry standard 16550 UART, so the V384 operates with the standard serial port drivers without requiring a custom driver to be installed.

The 128 byte Transmit and Receive FIFOs reduce CPU overhead and minimize the chance of buffer overflow and data loss. In addition to the 16550 UART registers, there are also Configuration register set where enhanced features such as the 9-bit (multidrop) mode, IrDA mode and the Watchdog Timer can be enabled.

The V384 is available in a 48-pin TQFP package.

APPLICATIONS

- Industrial and Embedded PCs
- Factory Automation and Process Controls
- Network Routers
- System Board Designs

FEATURES

- **128 Byte Transmit and Receive FIFO**
- Compliant to LPC 1.1 Specifications
- **-40°C to +85°C Industrial Temp Operation**
- Watchdog Timer with WDTOUT# signal
- 4 Independent UART channels
  - Programmable I/O mapped base addresses
  - Data rates up to 3 Mbps
  - Selectable RX FIFO interrupt trigger levels
  - **Auto RS-485 Half-Duplex Control mode**
  - Programmable character lengths (5, 6, 7, 8) with even, odd, or no parity
  - IrDA mode and separate IRTXA# and IRRXA# pins for the first UART channel
  - 9-bit (Multidrop) mode
- External 24MHz/48MHz clock
- **Single 3.3V Supply Voltage (±10%)**
- 5V tolerant inputs
- **48-TQFP package (7mm x 7mm)**

FIGURE 1. XR28V384 BLOCK DIAGRAM

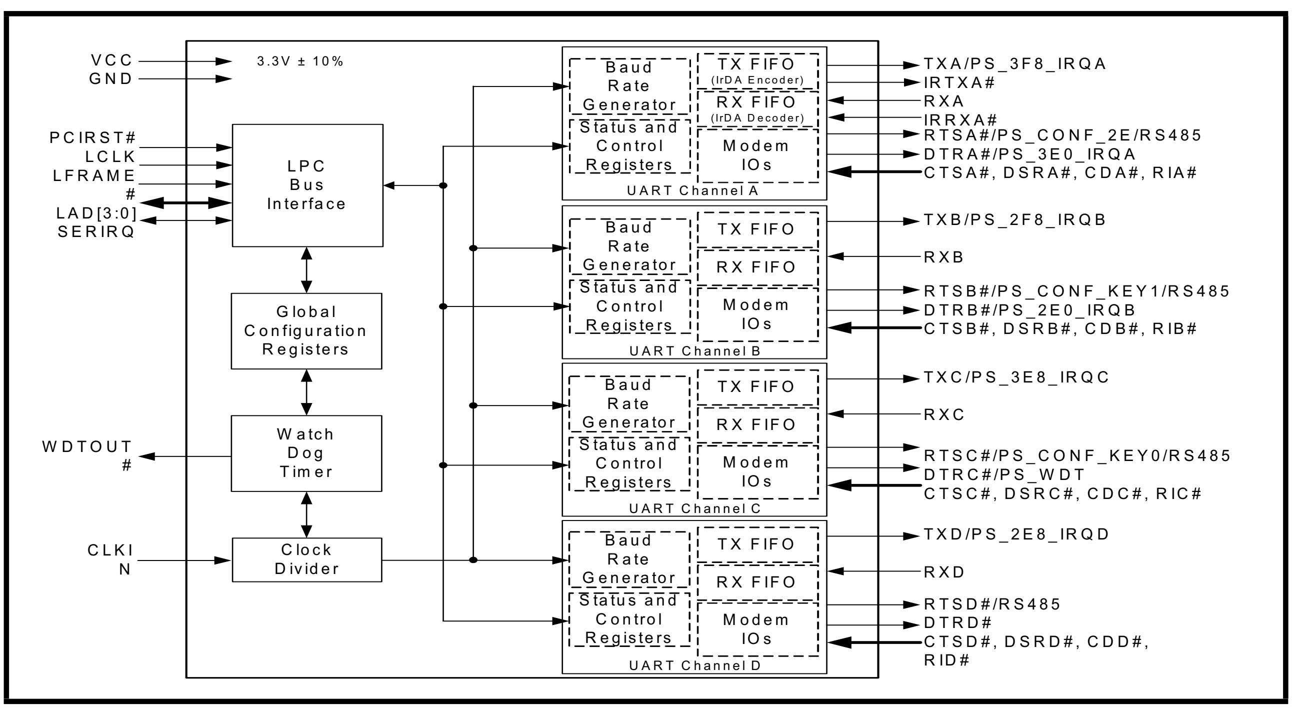
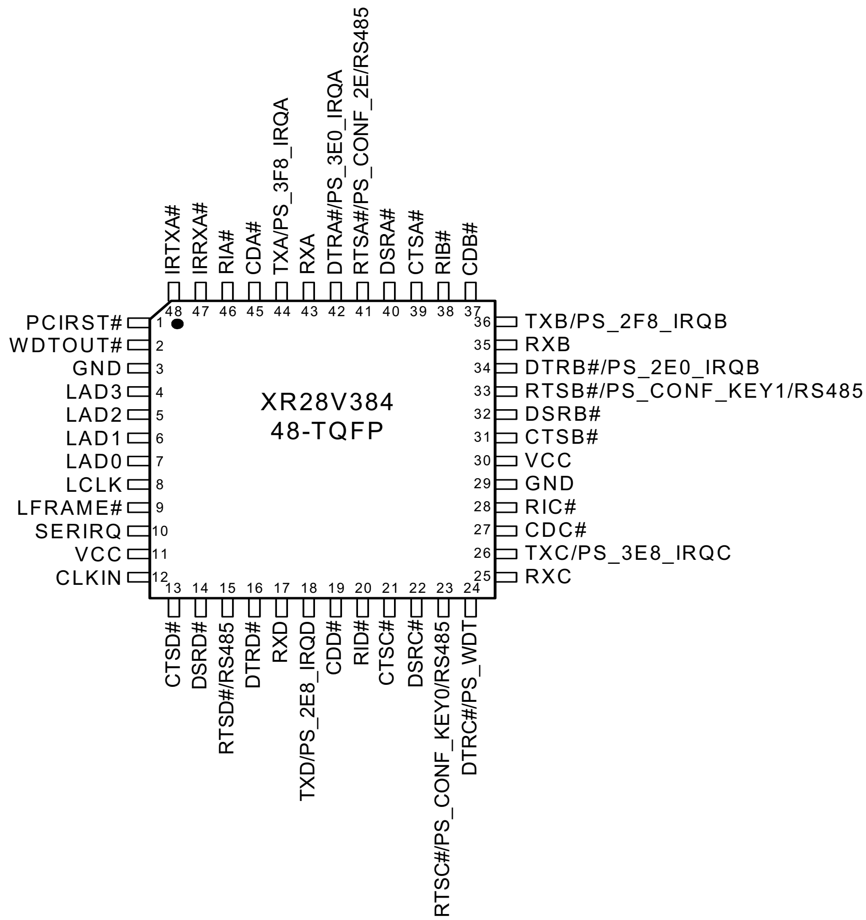


FIGURE 2. PIN OUT ASSIGNMENT



Ordering Information

PART NUMBER	**PACKAGE**	**OPERATING TEMPERATURE RANGE**	**DEVICE STATUS**
XR28V384IM48-F	48-Lead TQFP	-40°C to +85°C	Active
XR28V384IM48TR-F	48-Lead TQFP	-40°C to +85°C	Active

NOTE: **TR = Tape and Reel, F = Green / RoHS**

PIN DESCRIPTIONS

Pin Description

NAME	48-TQFP PIN#	TYPE	DESCRIPTION
LPC BUS INTERFACE			
PCIRST#	1	I	Active low Reset signal.
LAD3 LAD2 LAD1 LAD0	4 5 6 7	I/O	Multiplexed address / data bus [3:0]. See 'Section 1.2, LPC Bus Interface'.
LCLK	8	I	LPC clock input up to 33.3MHz.
LFRAME#	9	I	Active low LPC Frame signal indicates start of a new cycle or termination of a broken cycle.
SERIRQ	10	I/O	Bi-directional pin for sending interrupts. By default this pin is tri-stated when idle. Interrupts can be active high or low. See 'Section 1.2.1, Serial IRQ' and See 'Section 2.2.1.3, Interrupt Enable Register (IER) - Read/Write' for more information regarding interrupts.
UART I/O INTERFACE			
CTSD#	13	I	UART Channel D Clear-to-Send (active low) or general purpose input. This input should be connected to VCC or GND when not used.
DSRD#	14	I	UART Channel D Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RTSD#/RS485	15	O	UART Channel D Request-to-Send (active low) or general purpose output or Automatic RS485 Half Duplex control pin. See 'Section 1.4.4, Auto RS-485 Half-Duplex Control'.
DTRD#	16	O	UART Channel D Data-Terminal-Ready (active low) or general purpose output.
RXD	17	I	UART Channel D Receive Data. Normal receive data input must idle at logic 1 condition. This input should be connected to VCC or GND when not used.
TXD / PS_2E8_IRQD	18	O	UART Channel D Transmit Data. The TXD signal will be a logic 1 during reset or idle (no data). If it is not used, leave it unconnected. This pin has an internal pull-up resistor and is sampled upon power-up or reset. This will determine the default register settings for UART channel D. The registers can later be modified by the software. See Table 1 'UART Power On Configuration'.
CDD#	19	I	UART Channel D Carrier-Detect (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RID#	20	I	UART Channel D Ring-Indicator (active low) or general purpose input. This input should be connected to VCC or GND when not used.
CTSC#	21	I	UART Channel C Clear-to-Send (active low) or general purpose input. This input should be connected to VCC or GND when not used.
DSRC#	22	I	UART Channel C Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC or GND when not used.

Pin Description

NAME	48-TQFP PIN#	TYPE	DESCRIPTION
RTSC# / PS_CONF_KEY0/ RS485	23	O	UART Channel C Request-to-Send (active low) or general purpose output or Automatic RS485 Half-Duplex control pin. See 'Section 1.4.4, Auto RS-485 Half-Duplex Control'. This pin has an internal pull-up resistor and is sampled upon power-up or reset. See Table 1 'UART Power On Configuration'.
DTRC# / PS_WDT	24	O	UART Channel C Data-Terminal-Ready (active low) or general purpose output. This pin has an internal pull-up resistor and is sampled upon power-up or reset. The registers can later be modified by the software. See Table 1 'UART Power On Configuration'.
RXC	25	I	UART Channel C Receive data. Normal receive data input must idle at logic 1 condition. This input should be connected to VCC or GND when not used.
TXC / PS_3E8_IRQC	26	O	UART Channel C Transmit Data. The TXC signal will be a logic 1 during reset or idle (no data). If it is not used, leave it unconnected. This pin has an internal pull-up resistor and is sampled upon power-up or reset. This will determine the default register settings for UART channel C. The registers can later be modified by the software. See Table 1 'UART Power On Configuration'.
CDC#	27	I	UART Channel C Carrier-Detect (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RIC#	28	I	UART Channel C Ring-Indicator (active low) or general purpose input. This input should be connected to VCC or GND when not used.
CTSB#	31	I	UART Channel B Clear-to-Send (active low) or general purpose input. This input should be connected to VCC or GND when not used.
DSRB#	32	I	UART Channel B Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RTSB# / PS_CONF_KEY1/ RS485	33	O	UART Channel B Request-to-Send (active low) or general purpose output or automatic RS485 Half-Duplex control pin. See 'Section 1.4.4, Auto RS-485 Half-Duplex Control'. This pin has an internal pull-up resistor and is sampled upon power-up or reset See Table 1 'UART Power On Configuration'.
DTRB# / PS_2E0_IRQB	34	O	UART Channel B Data-Terminal-Ready (active low) or general purpose output. This pin has an internal pull-up resistor and is sampled upon power-up or reset. This will determine the default register settings for UART channel B. The registers can later be modified by the software. See Table 1 'UART Power On Configuration'.
RXB	35	I	UART Channel B Receive data. Normal receive data input must idle at logic 1 condition. This input should be connected to VCC or GND when not used.
TXB / PS_2F8_IRQB	36	O	UART Channel B Transmit Data. The TXB signal will be a logic 1 during reset or idle (no data). If it is not used, leave it unconnected. This pin has an internal pull-up resistor and is sampled upon power-up or reset. This will determine the default register settings for UART Channel B. The registers can later be modified by the software. See Table 1 'UART Power On Configuration'.
CDB#	37	I	UART Channel B Carrier-Detect (active low) or general purpose input. This input should be connected to VCC or GND when not used.

Pin Description

NAME	48-TQFP PIN#	TYPE	DESCRIPTION
RIB#	38	I	UART Channel B Ring-Indicator (active low) or general purpose input. This input should be connected to VCC or GND when not used.
CTSA#	39	I	UART Channel A Clear-to-Send (active low) or general purpose input. This input should be connected to VCC or GND when not used.
DSRA#	40	I	UART Channel A Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RTSA# / PS_CONF_2E/ RS485	41	O	UART Channel A Request-to-Send (active low) or general purpose output. This pin has an internal pull-up resistor and is sampled upon power-up or reset. The registers can later be modified by the software. **See Table 1 'UART Power On Configuration'**.
DTRA# / PS_3E0_IRQA	42	O	UART Channel A Data-Terminal-Ready (active low) or general purpose output. This pin has an internal pull-up resistor and is sampled upon power-up or reset. This will determine the default register settings for UART Channel A. The registers can later be modified by the software. **See Table 1 'UART Power On Configuration'**.
RXA	43	I	UART Channel A Receive data.The receive data input must idle at logic 1 condition. This input should be connected to VCC or GND when not used.
TXA / PS_3F8_IRQA	44	O	UART Channel A Transmit Data. The TXA signal will be a logic 1 during reset or idle (no data). If it is not used, leave it unconnected. This pin has an internal pull-up resistor and is sampled upon power-up or reset. This will determine the default register settings for UART Channel A. The registers can later be modified by the software. **See Table 1 'UART Power On Configuration'**.
CDA#	45	I	UART Channel A Carrier-Detect (active low) or general purpose input. This input should be connected to VCC or GND when not used.
RIA#	46	I	UART Channel A Ring-Indicator (active low) or general purpose input. This input should be connected to VCC or GND when not used.
IRRXA#	47	I	Infrared Receiver input. The infrared receive data input idles at logic 0. This input should be connected to GND when not used.
IRTXA#	48	O	Infrared Transmitter output. The IRTXA# signal will be a logic 0 during reset or idle (no data).
ANCILLARY SIGNALS			
CLKIN	12	I	Clock input 24 MHz or 48 MHz.
WDTOUT#	2	O	Active low watchdog timer output. This pin is open drain and needs a pull-up resistor if it is used. The registers can later be modified by the software. **See Table 1 'UART Power On Configuration'**.
POWER SIGNALS			
VCC	11, 30	Pwr	3.3V ± 10% power supply.
GND	3, 29	Pwr	Power supply common, ground.

Pin type: I=Input, O=Output, I/O= Input/output, Pwr=Power supply.

1.0 FUNCTIONAL DESCRIPTIONS

1.1 Power on Strapping Options

At power-on, strapping options for each pin listed in Table 1 result in the register values based upon the pin state selected. These register values can also be modified by the software.

1.1.1 UART/Watchdog Timer Options

The V384 provides seven pins for power on hardware strapping options to select the settings of the UART channels and Watchdog Timer.

TABLE 1: UART POWER ON CONFIGURATION

PIN NUMBER	PIN NAME	PIN STATE	REGISTER VALUES				COMMENT
			ENABLE (0x30)	BASE ADDRESS HIGH REGISTER (0x60)	BASE ADDRESS LOW REGISTER (0x61)	IRQSEL (0x70)	
18	TXD / PS_2E8_IRQD	1	0x1	0x2	0xE8	0x9	
		0	0x0	0x0	0x0	0x0	
26	TXC / PS_3E8_IRQC	1	0x1	0x3	0xE8	0x5	
		0	0x0	0x0	0x0	0x0	
34	DTRB# / PS_2E0_IRQB	1	0x1	0x2	0xE0	0x4	When both pins are high, the base address will be 0x2F8.
		0	0x0	0x0	0x0	0x0	
36	TXB / PS_2F8_IRQB	1	0x1	0x2	0xF8	0x4	
		0	0x0	0x0	0x0	0x0	
42	DTRA# / PS_3E0_IRQA	1	0x1	0x3	0xE0	0x3	When both pins are high, the base address will be 0x3F8.
		0	0x0	0x0	0x0	0x0	
44	TXA / PS_3F8_IRQA	1	0x1	0x3	0xF8	0x3	
		0	0x0	0x0	0x0	0x0	
24	DTRC# / PS_WDT	1	0x1	0x4	0x42	0x0	
		0	0x0	0x0	0x0	0x0	

After power-on, the Enable, Base Address High & Low, IRQSEL registers can be modified by the software.

1.1.2 Configuration Port and Key Selection Options

1.1.2.1 Configuration Port Selection Option

The configuration registers are programmed by the index port and the data port. The port address is determined by the strap pin RTSA#/PS_CONF_2E/RS485. If an external pull-down resistor is not installed, the default value of the RTSA#/PS_CONF_2E/RS485 pin is ’1’ when the system powers on. Therefore, the default index port address is 0x2E and the data port address is 0x2F.

TABLE 2: CONFIGURATION PORT SELECTION

RTSA#/PS_CONF_2E/RS485 (PIN 41)	INDEX PORT ADDRESS	DATA PORT ADDRESS
0	0x4E	0x4F
1 (default)	0x2E	0x2F

1.1.2.2 Configuration Entry Key Options

In order to enable the configuration register access mode, the entry key needs to be written consecutively twice to the index port. The entry key is generated by the power on setting pins RTSB#/PS_CONF_KEY1/RS485 and RTSC#/PS_CONF_KEY0/RS485.

TABLE 3: CONFIGURATION ENTRY KEY

RTSB#/PS_CONF_KEY1/RS485 (PIN 33)	RTSC#/PS_CONF_KEY0/RS485 (PIN 23)	ENTRY KEY
0	0	0x77
0	1	0xA0
1	0	0x87
1	1	0x67 (Default)

In order to disable the configuration register access mode, 0xAA must be written to the index port.

1.1.2.3 Example

1.1.2.3.1 Index port address 0x2E & Data port address 0x2F (default)

```
write (0x2E, 0x67);
write (0x2E, 0x67);      //write entry key (0x67) twice to configuration port
                         //Enable access to the configuration registers
write (0x2E, 0x20);      //Select the DEV_ID_M register
read (0x2F);             //Read the DEV_ID_M register
write (0x2E, 0x21);      //Select the DEV_ID_L register
read (0x2F);             //Read the DEV_ID_L register
write (0x2E, 0x25);      //Select the Clock Select Register
write (0x2F, 0x1);       //Select the input clock frequency 48 MHz
write (0x2E, 0x7);       //Select the LDN register
write (0x2F, 0x1);       //Select the UART Channel B
write (0x2E, 0xF6);      //Select the FIFO Mode Select Register of UART Channel B
write (0x2F, 0x3);       //Set the FIFO size 128 bytes,
                         //RX trigger level 1, 4, 8, 14 and no delay for THR empty interrupt
write (0x2E, 0x30);
write (0x2F, 0x1);       //Enable the UART Channel B
write (0x2E, 0xAA);      //Disable access to configuration registers
```

1.1.2.3.2 Index port address 0x4E & Data port address 0x4F

```
write (0x4E, 0x67);
write (0x4E, 0x67);     //write entry key (0x67) twice to configuration port
                        //Enable access to the configuration registers
write (0x4E, 0x23);     //Select the VID_M register
read (0x4F);            //Read the VID_M register
write (0x4E, 0x24);     //Select the VID_L register
read (0x4F);            //Read the VID_L register
write (0x4E, 0x25);     //Select the Clock Select Register
write (0x4F, 0x0);      //Select the input clock frequency 24 MHz
write (0x4E, 0x7);      //Select the LDN register
write (0x4F, 0x0);      //Select the UART Channel A
write (0x4E, 0x60);
write (0x4F, 0x3);      //Set the UART Channel A base address high byte as 0x3
write (0x4E, 0x61);
write (0x4F, 0xF8);     //Set the UART Channel A base address low byte as 0xF8
write (0x4E, 0xF6);     //Select the FIFO Mode Select Register of UART Channel A
write (0x4F, 0x0);      //Set the FIFO size 16 bytes,
                        //RX trigger level 1, 4, 8, 14 and no delay for THR empty interrupt
write (0x4E, 0x30);
write (0x4F, 0x1);      //Enable the UART Channel A
write (0x4E, 0xAA);     //Disable access to the configuration registers
```

1.2 LPC Bus Interface

The LPC bus interface has a 4-bit multiplexed address/data bus, 1 reset signal, 1 clock and 1 control signal. It also has one interrupt signal. The V384 implements the following signals of the LPC bus.

- LFRAME# is used by the host to start or stop transfers.
- LCLK is a clock used for synchronization.
- PCIRST# is an active low reset signal.
- LAD[3:0] signal lines communicate device address, control (read, write, wait and transfer type), and data information over the LPC bus between a host and a peripheral.
- Interrupt requests are issued through SERIRQ.

1.2.1 Serial IRQ

The V384 supports a serial IRQ scheme specified in specification for Serialized IRQ support for PCI system Rev6.0 which allows SERIRQ pin to be shared with multiple devices. The SERIRQ signal is tri-stated when idle. The SERIRQ is divided into 3 types of time slots known as Frames: Start frame, IRQ frame, and Stop frame. The SERIRQ uses LCLK for timing. There are two modes of operation for SERIRQ signal: Quiet mode and Continuous mode. These two modes are discussed in further detail in **'Section 1.2.1.1, Start Frame'**.

1.2.1.1 Start Frame

The Start frame indicates begining of the SERIRQ cycle. During this frame the SERIRQ is driven LOW for 4-8 clock cycles. It can be initiated by the host or V384 depending on the mode of operation.

In the Continuous mode, only the host controller initiates the Start frame to update the SERIRQ line information. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal defaults to the Continuous mode for the host controller to initiate the first Start frame.

In the Quiet mode, the Start frame is initiated by the device/host. The V384 drives the SERIRQ signal active low for one clock to initiate a Start Frame, and then tri-states it immediately. The host controller will then take over driving SERIRQ signal low in the next clock and will continue driving the SERIRQ low for 3 to 7 clock periods. This makes the total number of clocks low for 4 to 8 clock periods. After these clocks, the host controller will drive the SERIRQ high for one clock and then tri-states it.

A Start Frame may not be initiated while SERIRQ is active. The SERIRQ is active between Start and Stop frames while it is idle between Stop and Start frames.

1.2.1.2 IRQ Frame

Once the start frame has been initiated, all the peripherals must start counting frames based on the rising edge of the clock (LCLK). Each IRQ Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase, the peripheral drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ will be left tri-stated. During the Recovery phase, the peripheral device drives the SERIRQ high. During the Turn-around phase, the peripheral device leaves the SERIRQ tri-stated. The V384 supports IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, and IRQ11.

TABLE 4: SERIRQ SAMPLING PERIODS

IRQ/DATA FRAME	SIGNAL SAMPLED	NUMBER OF CLOCKS PAST START
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

1.2.1.3 Stop Frame

After all IRQ/Data Frames have been completed, the host controller will terminate SERIRQ by a Stop frame. Only the host controller can initiate the Stop frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the next SERIRQ cycle will be the Quiet mode whereas if it is low for 3 clocks, the next SERIRQ cycle will be the Continuous mode.

1.3 Watchdog Timer (WDT)

The WDT is typically used in a system to initiate any of the several types of corrective action, including processor reset, power cycling, fail-safe activation etc. The Watchdog timer of V384 is an 8 bit counter controlled by six registers. **See "Section 2.1.2.2, Watchdog Timer Registers (LDN = 0x08)" on page 26.** WDTOUT# idles HIGH and will transition LOW when a time out occurs. The V384 provides three time intervals: 10 ms, 1s and 1 minute allowing for timeouts ranging from approximately 2.5 seconds to more than 4 hours. **See 'Section 2.1.2.2.4, WDT Timer Status and Control Register - Read/Write'** to set up time interval.

1.4 UART

1.4.1 External Clock Input (CLKIN)

Along with LCLK, the V384 also needs an external clock for UART data communication. It can support any clock up to 48MHz. The 24MHz and 48MHz are the standard clock frequencies supported by the V384. **See 'Section 2.1.1.5, Clock Select Register - Read/Write'**.

1.4.1.1 Programmable Baud Rate Generator

Each UART has its own Baud Rate Generator (BRG) with a prescaler. The prescaler is controlled by Bit[1:0] of **Enhanced Multifunction Register - Read/Write.**

Table 5 shows the standard data rates available with a 24 MHz external clock at 16X sampling rate and internal clock frequency set to 1.8462 MHz. The divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (Internal clock frequency) / (serial data rate x 16)

TABLE 5: TYPICAL DATA RATES WITH A 1.8462MHZ INTERNAL CLOCK

BAUD Rate (BPS)	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	ACTUAL BAUD RATE	DATA RATE ERROR (%)
150	768	300	03	00	150.24	0.2
300	384	180	01	80	300.48	0.2
600	192	C0	00	C0	600.96	0.2
1200	96	60	00	60	1201.92	0.2
2400	48	30	00	30	2403.85	0.2
4800	24	18	00	18	4807.69	0.2
9600	12	0C	00	0C	9615.39	0.2
19200	6	06	00	06	19230.77	0.2
38400	3	03	00	03	38461.54	0.2
57600	2	02	00	02	57692.31	0.2
115200	1	01	00	01	115384.6	0.2

Table 8 lists the different internal clock settings.

1.4.2 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and up to 128 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the internal sampling clock. The transmitter sends the start bit followed by the number of data bits, inserts the proper parity bit if enabled, and adds the stop bit(s). The status of the THR and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

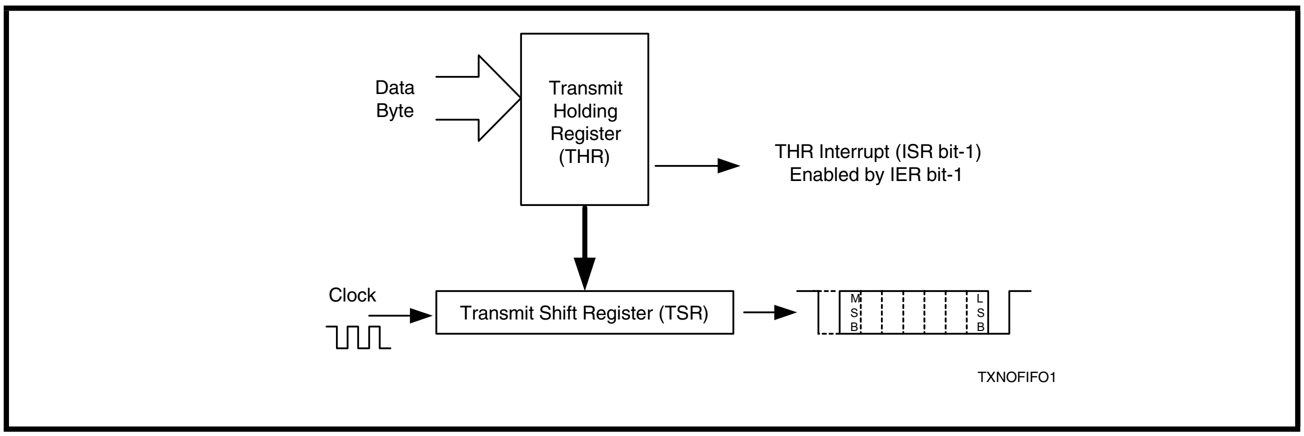
1.4.2.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start bit, data bits, parity bit and stop bit(s). The least significant bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of up to 128 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

1.4.2.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

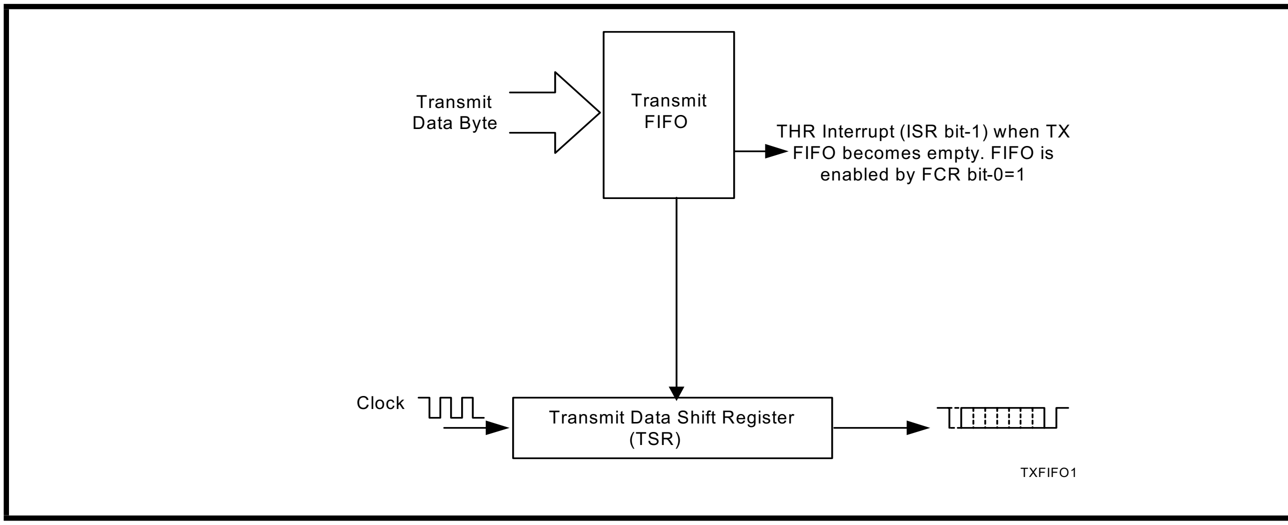
FIGURE 3. TRANSMITTER OPERATION IN NON-FIFO MODE



1.4.2.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 128 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the FIFO becomes empty. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 4. TRANSMITTER OPERATION IN FIFO MODE



1.4.3 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and up to 128 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the internal sampling clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0. See Figure 5.

1.4.3.1 *Receive Holding Register (RHR) - Read-Only*

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of up to 128 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 5. RECEIVER OPERATION IN NON-FIFO MODE

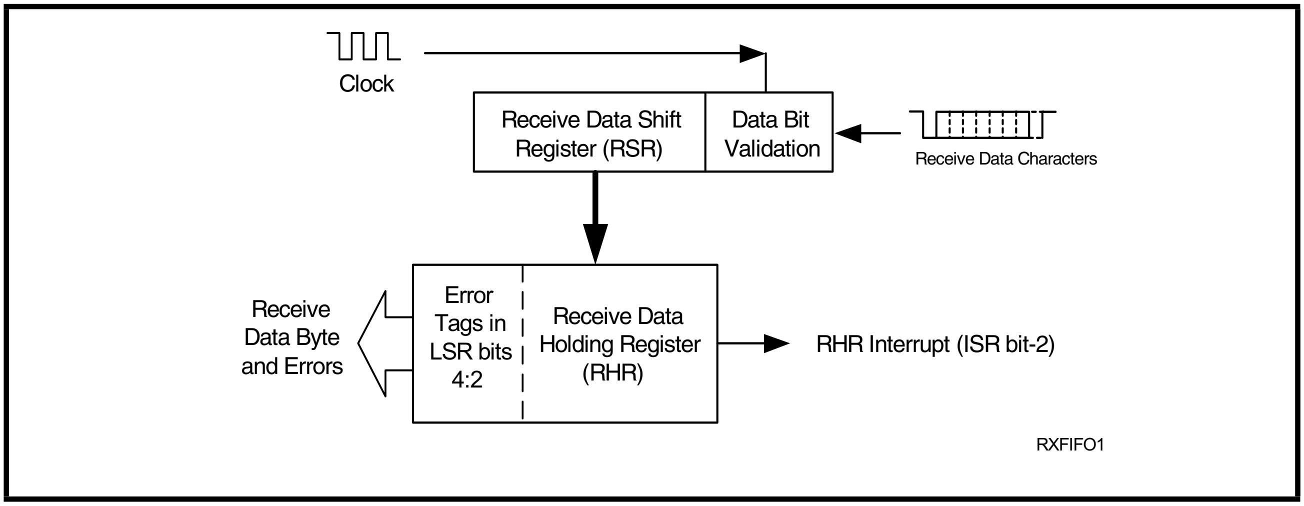
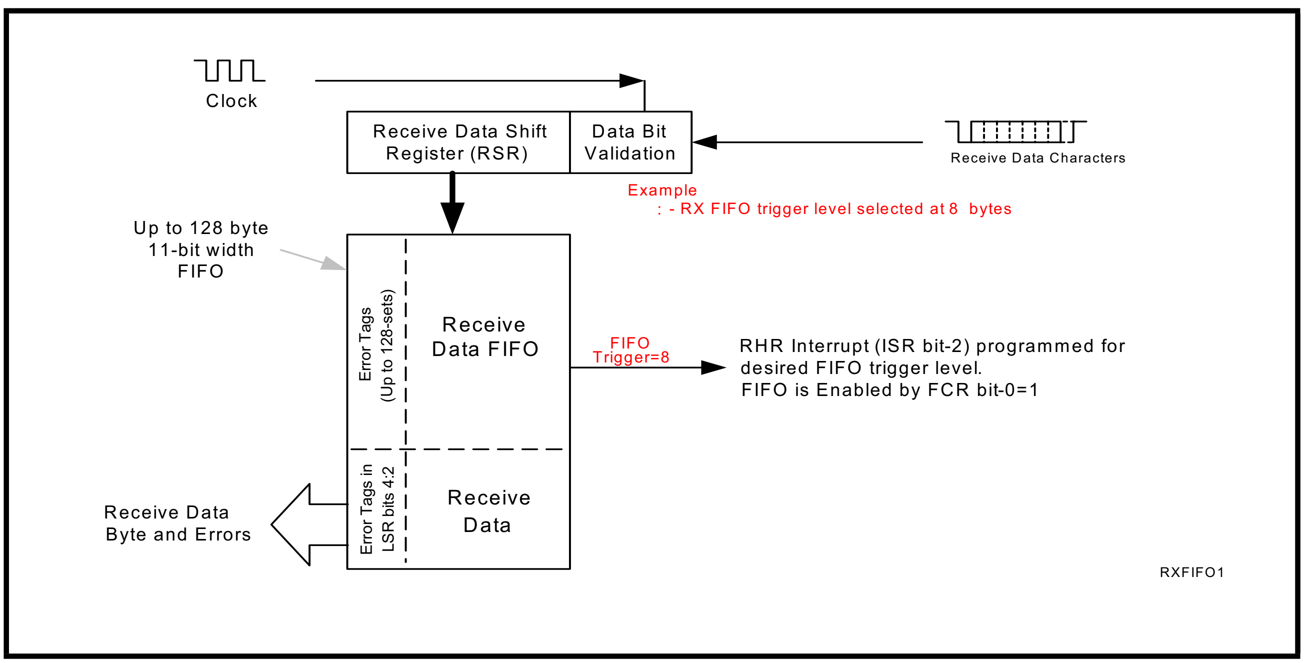


FIGURE 6. RECEIVER OPERATION IN FIFO MODE



1.4.4 Auto RS-485 Half-Duplex Control

The Auto RS-485 Half-Duplex Control feature changes the behavior of the RTS#/RS485 pin when enabled by **Enhanced Multifunction Register - Read/Write** bit-4. If enabled, by default, it de-asserts RTS#/RS485 ouput following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit data packet, it only has to load data bytes to the transmit FIFO. The transmitter automatically asserts RTS#/RS485 output prior to sending the data. The polarity of RTS#/RS485 signal can be modified by bit-5 of Enhanced Multifunction register.

1.4.5 Normal Multidrop (9-bit) Mode

Normal multidrop mode is enabled when bit-7 of Enhanced Multifunction register in the UART Device Configuration Registers is set to '1'. In the multidrop (9-bit) mode, the parity bit becomes the address/data bit.

If a data byte is received (9th bit is '0'), it will be loaded into the RX FIFO and the parity error bit will be '0'. If an address byte is received (9th bit is '1'), it will be loaded into the RX FIFO and the parity error bit will be '1'. When the address byte has been received, the software will need to examine the byte: If the address matches its slave address, the receiver will receive the subsequent data; If the address does not match its slave address, then the receiver will discard the data.

1.4.5.1 Auto Address Detection

Auto Address Detection mode is enabled when bit-6 of Enhanced Multifunction register (0xF0) in UART device configuration registers set is set to '1'. The desired slave address will need to be written into the 9-bit mode slave address register (0xF4) in the UART device configuration registers set. If the received byte is an address byte that does not match the programmed character in the 9-bit mode slave address register, the receiver will discard these data. Upon receiving an address byte that matches the 9-bit mode slave address register character, the receiver will automatically push the address byte into the RX FIFO and set the parity error bit in the LSR register. The receiver also generates an LSR interrupt if enabled. The receiver will then receive the subsequent data. If another address byte is received and does not match the programmed 9-bit mode slave address register value, then the receiver will ignore the data that follows.

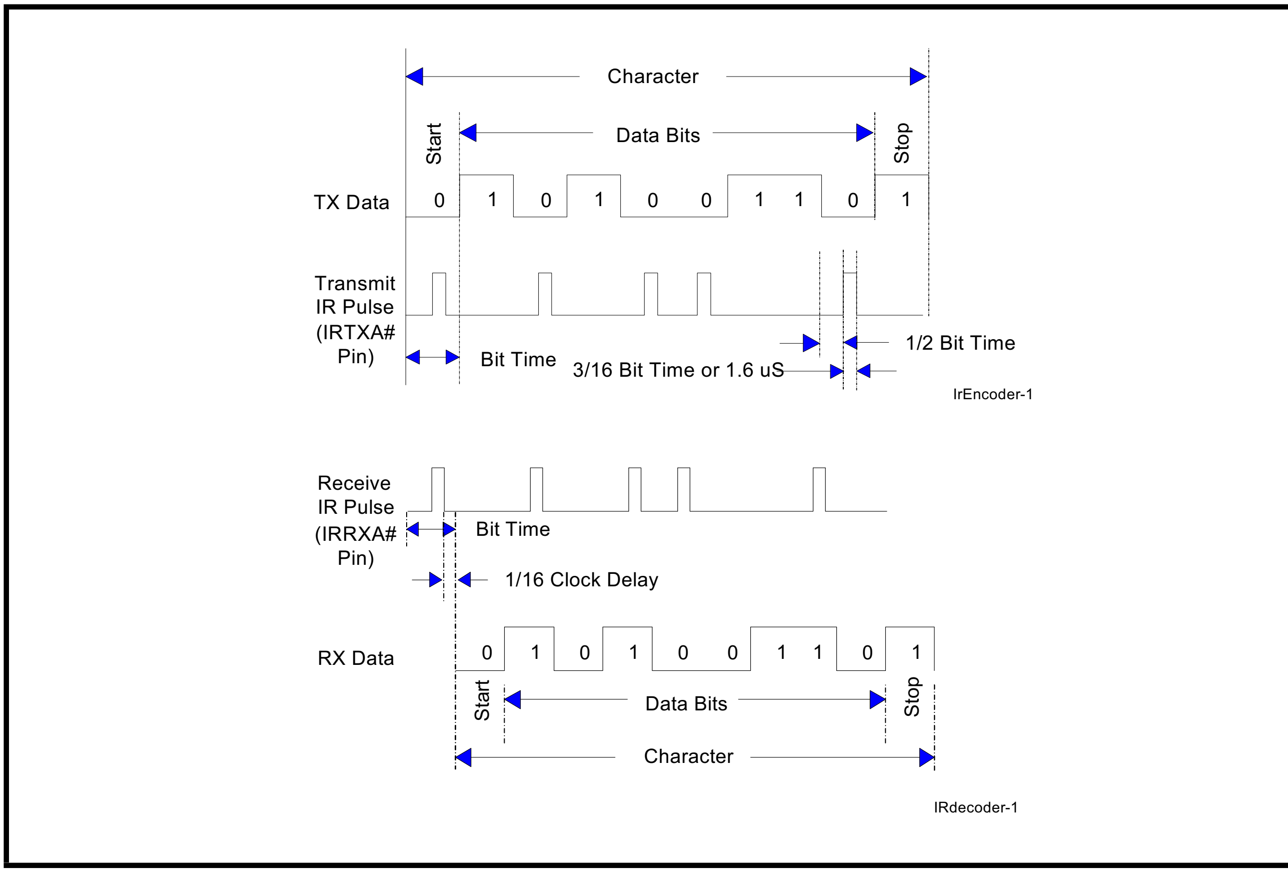
1.4.6 Infrared Mode

The V384 UART Channel A includes the infrared encoder and decoder compatible to IrDA (Infrared Data Association) version 1.0. The infrared encoder sends out a 3/16 of a bit wide or 1.6 uS HIGH pulse for each "0" bit in the transmit data stream with a data rate up to 115.2 kbps. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 7.

The infrared encoder and decoder are enabled by setting Infrared Mode Control Register - Read/Write bit-4 to a '1'. The IRRXA# input assumes an idle level of logic zero after a reset and power up, see Figure 7. The IRRXA# input will assume an idle level of logic HIGH if bit-0 of the Infrared Mode Control Register - Read/Write is set to '1'. The IRTXA# is idle at LOW by default. The IRTXA# will be idle at HIGH if bit-1 of the Infrared Mode Control Register - Read/Write is set to '1'.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the IRRXA# pin. Each time it senses a light pulse, it returns a logic 0 to the data bit stream.

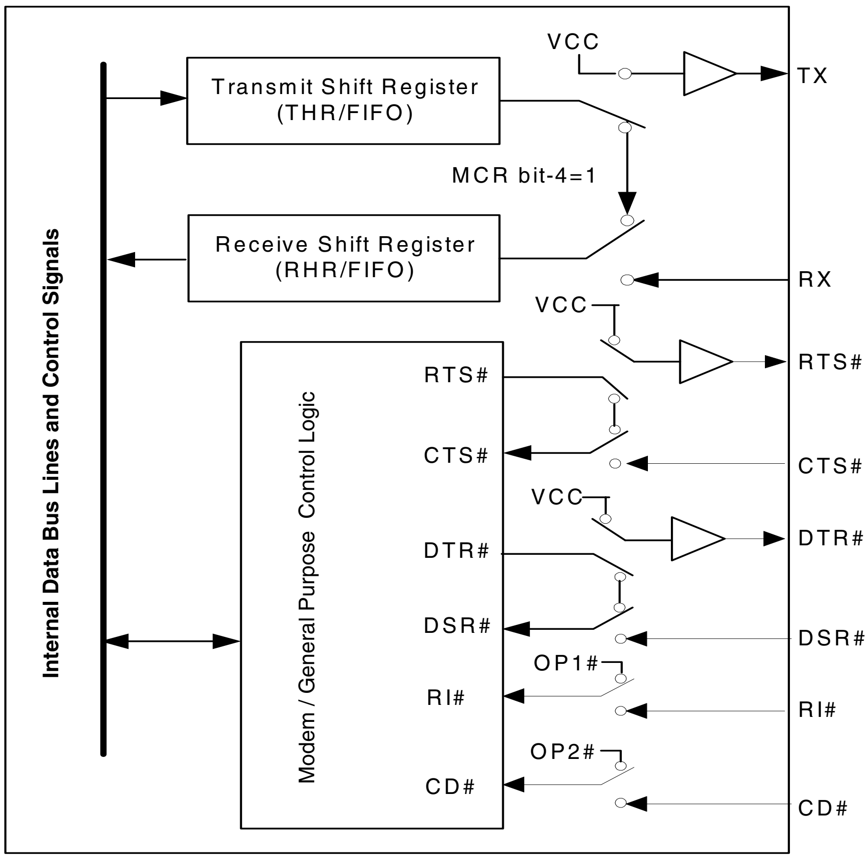
FIGURE 7. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



1.4.7 Internal Loopback

The V384 provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. Figure 8 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held HIGH or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false "break" signal.

FIGURE 8. INTERNAL LOOPBACK



1.5 Serial Transceiver Interface

The V384 is typically used with RS-232, RS-485 and IR transceivers. The following figure shows typical connections from the UART to the different transceivers. For more information on RS-232 and RS-485/422 transceivers, go to www.exar.com or send an e-mail to uarttechsupport@exar.com.

FIGURE 9. XR28V384 TYPICAL SERIAL INTERFACE CONNECTIONS

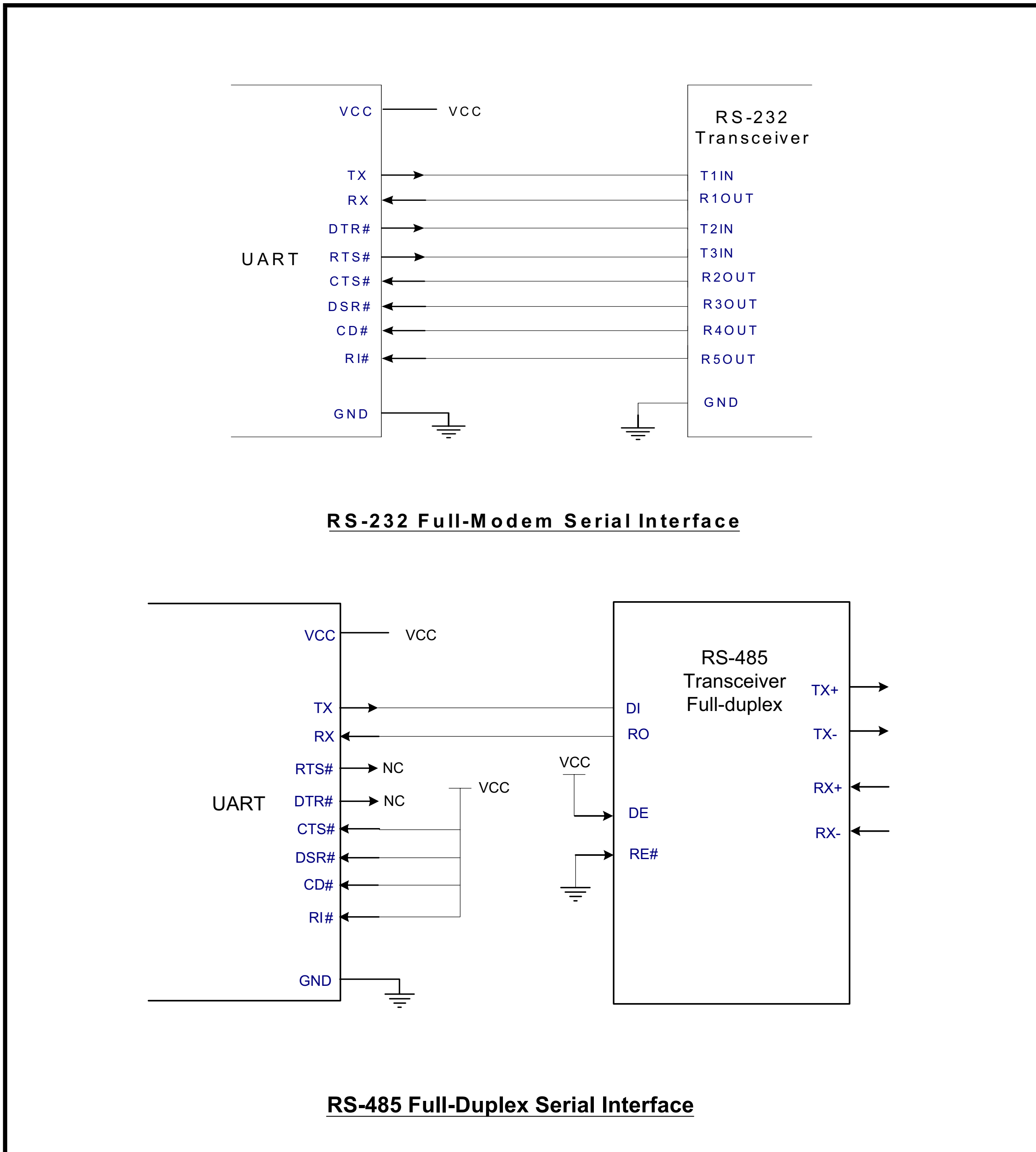
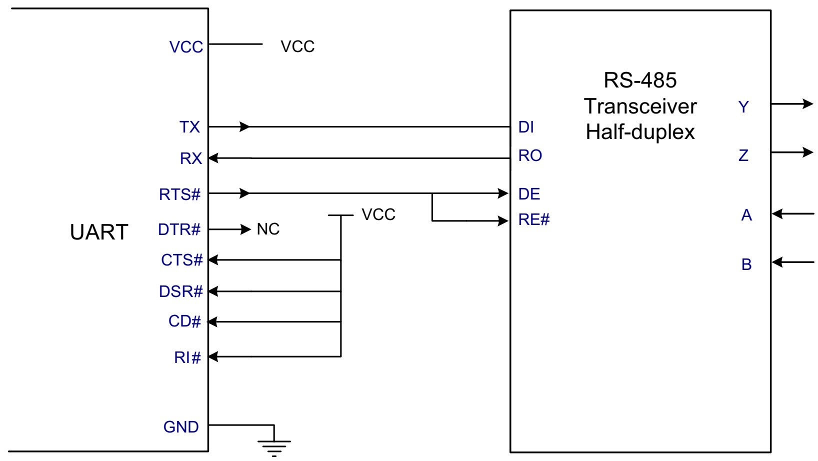
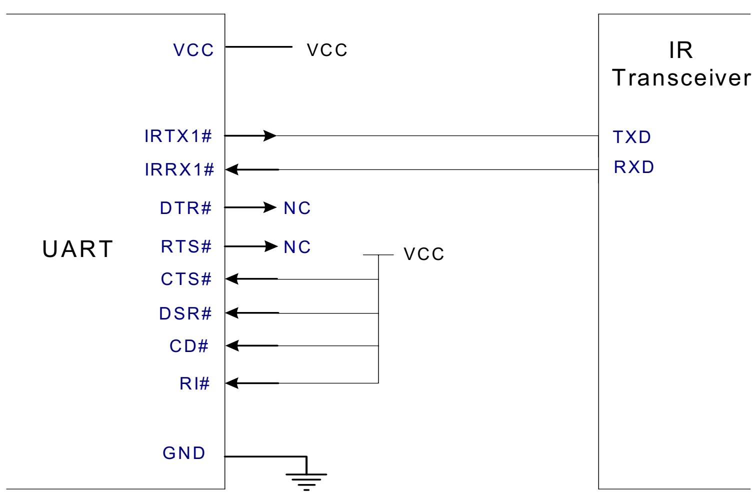


FIGURE 10. XR28V384 TYPICAL SERIAL INTERFACE CONNECTIONS



RS-485 Half-Duplex Serial Interface



Infrared Connection

1.6 Device Reset

The PCIRST# input resets the internal registers and the serial interface outputs to their default states. The PCIRST# assertion for general system reset may occur at any time and may be asynchronous to LCLK.

2.0 REGISTER DETAILS

The Register map of V384 is primarily divided into two sections:

- Configuration Register set
- UART internal Register set

2.1 Configuration Register

There are two different sets of configuration registers: the Global Control Register set and the Device Configuration Register set. The Global Control Registers can be used to perform software reset, select clock input frequency, configure watchdog timer, configuration port selection and read Vendor ID and Device ID. The Device Configuration Registers configure all 4 UARTs to enable the UART channel, base address, IRQ channel, internal clock frequency, IR control, 9-bit mode slave address and FIFO mode. The watchdog timer can also be configured in the Device Configuration Registers set including enable the watchdog timer, configure base address, IRQ channel, timer count number and monitor the timer status.

- **Global Control Registers**

The Global Control Register set is the set of registers that are shared among all the devices of V384. Table 6 describes the list of all the Global Control Registers.

TABLE 6: LPC BUS GLOBAL CONTROL REGISTERS

ADDRESS [A7:A0]	REGISTER	READ/WRITE COMMENT	RESET STATE
0x02	Software Reset Register	Read/Write	Bits [7:0] = 0x00
0x07	Logic Device Number Register (LDN)	Read/Write	Bits [7:0] = 0x00
0x20	Device ID MSB Register (DEV_ID_M)	Read-only	Bits [7:0] = 0x03
0x21	Device ID LSB Register (DEV_ID_L)	Read-only	Bits [7:0] = 0x84
0x23	Vendor ID MSB Register (VID_M)	Read-only	Bits [7:0] = 0x13
0x24	Vendor ID LSB Register (VID_L)	Read-only	Bits [7:0] = 0xA8
0x25	Clock Select Register (CLKSEL)	Read/Write	Bits [7:0] = 0x00
0x26	Watchdog Timer Control Register (WDT)	Read/Write	Bits [7:0] = 0x00
0x27	Port Select Register	Read/Write	Bits [7:0] = 0x00

- **Device Configuration Registers**

The Device Configuration Register set is specific to each device of the V384. The V384 has two types of devices: 1) UART 2) Watchdog Timer. It has 4 UART devices and 1 Watchdog timer. All the UARTs have similar register set except UARTA. UARTA has an additional register to control IR function.

The Device Configuration register set can be accessed through indirect addressing described in **'Section 1.1.2.3, Example'** . **Table 7** lists the Device Configuration registers.

TABLE 7: DEVICE CONFIGURATION REGISTERS

	ADDRESS [A7:A0]	REGISTER	READ/WRITE	RESET STATE	COMMENT
UARTA (LDN=0x00)	0x30	UART Enable Register (ENABLE)	Read/Write	See Table 1 'UART Power On Configuration'	
	0x60	Base Address High Register	Read/Write		
	0x61	Base Address Low Register	Read/Write		
	0x70	IRQ Channel Select Register	Read/Write		
	0xF0	Enhanced Multifunction Register	Read/Write	0x00	
	0xF1	IR Control Register	Read/Write	0x44	
	0xF4	9-bit Mode Slave Address Register	Read/Write	0x00	
	0xF5	9-bit Mode Slave Address Mask Register	Read/Write	0x00	
	0xF6	FIFO Mode Select Register	Read/Write	0x00	
UARTB (LDN=0x01) UARTC (LDN=0x02) UARTD (LDN=0x03)	0x30	UART Enable Register (ENABLE)	Read/Write	See Table 1 'UART Power On Configuration'	
	0x60	Base Address High Register	Read/Write		
	0x61	Base Address Low Register	Read/Write		
	0x70	IRQ Channel Select Register	Read/Write		
	0xF0	Enhanced Multifunction Register	Read/Write	0x00	
	0xF4	9-bit Mode Slave Address Register	Read/Write	0x00	
	0xF5	9-bit Mode Slave Address Mask Register	Read/Write	0x00	
	0xF6	FIFO Mode Select Register	Read/Write	0x00	
WDT (LDN=0x08)	0x30	Watchdog Enable Register	Read/Write	0x01	See Table 1 'UART Power On Configuration'
	0x60	Base Address High Register	Read/Write	0x04	
	0x61	Base Address Low Register	Read/Write	0x42	
	0x70	IRQ Channel Select Register	Read/Write	0x00	
	0xF0	Timer Status and Control Register	Read/Write	0x02	
	0xF1	Timer Count Number Register	Read/Write	0x0A	

2.1.1 Global Control Registers

2.1.1.1 Software Reset Register

Software Reset resets the Device Configuration registers to their factory defaults. Strapping pins from **Table 1** are not sampled during a software reset.

Bit [0]: Software reset

- Logic 0 = Disable software reset (default).
- Logic 1 = Enable software reset. After the software reset, this bit will turn to ’0’ automatically.

Bits [7:1]: Reserved

2.1.1.2 Logic Device Number Register - Read/Write

This register selects device configuration register set among the 4 channel UARTs and the watchdog timer.

Bits [7:0]: Select different device configuration register set.

- 0x00 = Select UART A device configuration register (default).
- 0x01 = Select UART B device configuration register.
- 0x02 = Select UART C device configuration register.
- 0x03 = Select UART D device configuration register.
- 0x08 = Select Watchdog Timer device configuration register.

2.1.1.3 Device ID MSB/LSB Register - Read only

***DEV_ID_M* (0x20):** This register provides upper byte device ID for XR28V384. The default value is 0x03.

DEV_ID_L (0x21): This register provides lower byte device ID for XR28V384. The default value is 0x84.

2.1.1.4 Vendor ID MSB/LSB Register - Read only

VID_M (0x23): This register value provides upper byte of Exar’s Vendor ID. The default value is 0x13.

VID_L (0x24): This register value provides lower byte of Exar’s Vendor ID. The default value is 0xA8.

2.1.1.5 Clock Select Register - Read/Write

This register selects the clock frequency.

Bit [0]: Clock select

- Logic 0 = The CLKIN is 24 MHz (default).
- Logic 1 = The CLKIN is 48 MHz.

Bits [7:1]: Reserved

2.1.1.6 Watchdog Timer Control Register - Read/Write

This register controls the watchdog timer.

Bit [0]: Assert a low pulse from WDTOUT# pin

- Logic 0 = Watchdog timer (WDT) will assert a low pulse from WDTOUT# pin (default).
- Logic 1 = Watchdog timer (WDT) will not assert a low pulse from WDTOUT# pin, but the timeout status will be set.

Bit [1]: Restart timer

- Logic 0 = Read watchdog timer (WDT) will restart the timer (default).
- Logic 1 = Read watchdog timer (WDT) will not restart the timer.

Bits [7:2]: Reserved

2.1.1.7 Port Select Register - Read/Write

This register selects the configuration port.

Bits [1:0]: Select configuration entry key

The default value of these bits are determined by RTSB#/PS_CONF_KEY1/RS485 and RTSC/PS_CONF_KEY0/RS485. **See Table 3 'Configuration Entry Key'**.

- '00' = The entry key is 0x77.
- '01' = The entry key is 0xA0.
- '10' = The entry key is 0x87.
- '11' = The entry key is 0x67.

Bits [3:2]: Reserved

Bit [4]: Select configuration port

The default value of this bit is determined by RTSA#/PS_CONF_2E/RS485 pin. **See Table 2 'Configuration Port Selection'**.

- Logic 0 = The configuration port is 0x2E/0x2F.
- Logic 1 = The configuration port is 0x4E/0x4F.

Bits [7:5]: Reserved

2.1.2 Device Configuration Registers

In order to access Device Configuration Register set, the configuration regsiter access mode has to be enabled. The value in the LDN register determines which device's configuration register set to access.

Example: if LDN register = 0x02, modifying UART Enable Register (0x30) will modify UART Enable Register of channel C.

2.1.2.1 UART Registers

2.1.2.1.1 UART Enable Register (ENABLE) - Read/Write

This register enables/disables the UART selected in the LDN register.

Bit [0]: Enable/Disable UART

The default value of this bit is determined by the strapping options. **See Table 1 'UART Power On Configuration'**. This bit can be programmed after power up.

- Logic 0 = Disable the UART selected in LDN register.
- Logic 1 = Enable the UART selected in LDN register.

Bits [7:1]: Reserved

2.1.2.1.2 Base Address High/Low Register - Read/Write

The V384 provides programmable I/O mapped address feature. Configure the MSB/LSB of 16-bit I/O address, for the UART selected in LDN register, in this register.

Bits [7:0]: MSB of UART base address (0x60)

The default value of this register is determined by the strapping options. **See Table 1 'UART Power On Configuration'**.

Bits [7:0]: LSB of UART base address (0x61)

The default value of this register is determined by the strapping options. **See Table 1 'UART Power On Configuration'**.

2.1.2.1.3 IRQ Channel Select Register - Read/Write

The V384 supports different IRQ channels and modes. The IRQ modes and IRQ channel number for each device of V384 should be programmed in their respective IRQ Channel Selelct register. Each device of V384 can have same/different IRQ channel.

Bits [3:0]: Select the IRQ channel

The default values of these bits is determined by the strapping options **See Table 1 'UART Power On Configuration'.** They can also be configured via software after power on.

Bit [4]: Enable/Disable the IRQ Sharing mode

- Logic 0 = Disable the IRQ sharing mode (default). The IRQ channel must be different for each UART for proper behavior.
- Logic 1 = Enable the IRQ sharing mode. The IRQ channel (bits 3-0) can be different or be the same as the other UARTs.

Bits [6:5]: IRQ Sharing mode

These two bits are effective only when IRQ sharing mode is enabled (bit[4] = '1'). The SERIRQ time slot is specified by bits 3-0. An interrupt will only appear on the SERIRQ pin during that time slot if MCR[3] = '1'.

- '00' = The IRQ Sharing mode is active LOW level (default). There will be an active low pulse continuously on the SERIRQ pin until the interrupt has been cleared.
- '01' = The IRQ Sharing mode is active LOW edge. When there is an interrupt, there will be a single active low pulse on the SERIRQ pin.
- '10' = The IRQ Sharing mode is active HIGH level. There will be an active high pulse continuously on the SERIRQ pin until the interrupt has been cleared.
- '11' = Reserved.

Bit [7]: Reserved

2.1.2.1.4 Enhanced Multifunction Register - Read/Write

This register enables/disables the RS-485 mode, 9-bit mode, selects clock frequency and delay in the IR mode.

Bits [1:0]: Internal clock frequency

The V384 provides an option to select among various internal clock frequency, which is used to generate different baud values. The value of the internal clock frequency is dependent on external clock provided to the CLKIN pin and setting of **Clock Select Register - Read/Write**. Table 8 describes various possible internal clock frequencies derived from 24MHz/48MHz external clock.

TABLE 8: INTERNAL CLOCK FREQUENCY (MHZ)

BITS[1:0]	EXTERNAL CLOCK = 24MHZ		EXTERNAL CLOCK = 48MHZ	
	CLKSEL=0x0	CLKSEL=0x1	CLKSEL=0x0	CLKSEL =0x1
00	1.8462	0.9231	3.6923	1.8462
01	18	9	36	18
10	24	12	48	24
11	14	7	28	14

See 'Section 1.4.1.1, Programmable Baud Rate Generator'.

Bit [2]: IR mode TX Delay

- Logic 0 = TX transmits data immedately when changing from RX to TX (default).
- Logic 1 = TX delays 4 character time when changing from RX to TX.

Bit [3]: IR mode RX Delay

- Logic 0 = RX is enabled immediately after TX is idle (default).
- Logic 1 = RX is disabled for 4 character time after TX is idle.

Bit [4]: Enable/Disable Auto RS-485 Half-Duplex Control mode

- Logic 0 = Disable the Auto RS-485 Half-Duplex Control mode (default). The RTS#/RS485 pin can be controlled by MCR bit-1.
- Logic 1 = Enable the Auto RS-485 Half-Duplex Control mode. The RTS#/RS485 signal polarity is determined by the bit-5.

Bit [5]: Invert the RTS#/RS485 signal polarity for RS-485 Half-Duplex Control mode

- Logic 0 = RTS#/RS485 signal polarity is HIGH for transmission and LOW for reception (default).
- Logic 1 = RTS#/RS485 signal polarity is inverted (that is, LOW for transmission and HIGH for reception).

Bit [6]: Auto Address Detection

- Logic 0 = All bytes received will be loaded into RX FIFO. **See 'Section 1.4.4, Auto RS-485 Half-Duplex Control'**.
- Logic 1 = All bytes received after address byte that matches the given address or broadcast address (determined by the 9-bit mode slave address register and 9-bit mode slave address mask register) will be loaded into RX FIFO. **See 'Section 1.4.5.1, Auto Address Detection'.**

Bit [7]: Enable/Disable the 9-bit Mode

- Logic 0 = Disable the 9-bit mode (default).
- Logic 1 = Enable the 9-bit mode (multi-drop mode).

In the 9-bit mode, the parity bit becomes the address/data bit.**See 'Section 1.4.5, Normal Multidrop (9-bit) Mode'**.

2.1.2.1.5 Infrared Mode Control Register - Read/Write

The V384 supports IR mode for UART channel A only. It controls infrared mode by setting this register. See 'Section 1.4.6, Infrared Mode'.

Bit [0]: IR mode IRRXA# invert

- Logic 0 = IRRA# idles LOW. (Default)
- Logic 1 = Invert the IRRXA# for IR mode, idle at HIGH.

Bit [1]: IR mode IRTXA# invert

- Logic 0 = IRTXA# idles LOW. (Default)
- Logic 1 = Invert the IRTXA# for IR mode, idle at HIGH.

Bit [2]: IR mode Half-Duplex

- Logic 0 = Enable full duplex function for IR mode.
- Logic 1 = Enable half duplex function for IR mode (default).

Bits [4:3]: IR mode Enable

- '00' or '01' = Disable the IR function (default value is '00').
- '10' = Enable the IR function, active pulse is 1.6 us.
- '11' = Enable the IR function, active pulse is 3/16 bit time.

Bits [7:5]: Reserved

2.1.2.1.6 9-bit Mode Slave Address Register - Read/Write

This register indicates the slave address in 9-bit mode. This register along with the 9-bit mode slave address mask register will determine the given address and broadcast address in 9-bit mode. The V384 will respond to both the given address and the broadcast address.

2.1.2.1.7 9-bit Mode Slave Address Mask Register - Read/Write

This register indicates the slave address mask in 9-bit mode. This register along with the 9-bit mode slave address register will determine the given address and broadcast address in 9-bit mode. The V384 will respond to both the given address and the broadcast address.

- Given address: If bit n of the 9-bit mode slave address mask register is '0', then the corresponding bit of given address is 'do not care'.
- Broadcast address: If bit n of the ORed 9-bit mode slave address register and 9-bit mode slave address mask register is '0', then this bit n is a 'do not care' bit. The remaining bit which is '1' is compared to the received address.

TABLE 9: EXAMPLE

REGISTER	EXAMPLE 1	EXAMPLE 2	EXAMPLE 3	EXAMPLE 4
9-bit mode slave address register (0xF4)	11110100	00001111	01010101	11100111
9-bit mode slave address mask register (0xF5)	01010101	10101010	11111111	00001111
Given address	x1x1x1x0	0x0x1x1x	01010101	xxxx0111
Broadcast address	1111x1x1	1x1x1111	11111111	111x1111