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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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XR77128

Quad Output Digital PWM/PFM Universal PMIC

General Description

The XR77128 is a quad channel digital Pulse Width Modulated (PWM) step down (buck) controller. A wide 4.75V to 5.5V and 5.5V to 25V input voltage range allows for single supply operation from standard power rails.

With integrated FET gate drivers, two LDOs for standby power and a 105kHz to 1.23MHz independent channel to channel programmable constant operating frequency, the XR77128 reduces overall component count, solution footprint and optimizes conversion efficiencies. A selectable digital Pulse Frequency Mode (PFM) capable of better than 80% efficiency at light current load and low operating current allow for portable and Energy Star compliant applications. Each XR77128 channel's output voltage is individually programmable down to 0.6V with a resolution of 2.5mV, and is configurable for precise soft start and soft stop sequencing, including delay and ramp control.

The XR77128 operations are fully controlled via a SMBus-compliant I^2C interface allowing for advanced local and/or remote reconfiguration, full performance monitoring and reporting as well as fault handling.

Built-in independent output Over-Voltage, Over-Temperature, Over-Current and Under-Voltage Lockout protections insure safe operation under abnormal operating conditions.

The XR77128 is offered in a RoHS compliant, "green"/halogen free 44-pin TQFN package.

FEATURES

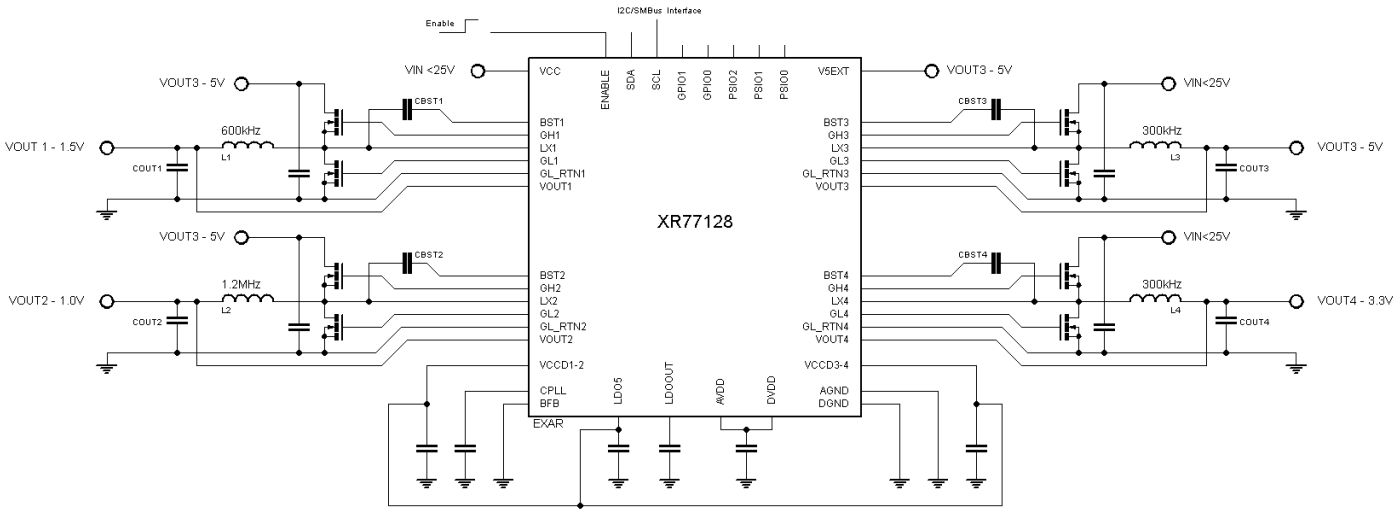
- Quad Channel Step-down Controller
  - Digital PWM 105kHz-1.23MHz Operation
  - Individual Channel Frequency Selection
  - Patented digital PFM with Ultrasonic mode
  - Patented Over Sampling Feedback
  - Programmable 5 coefficient PID control
  - Integrated MOSFET Drivers
  - Supports DrMOS devices
- 4.75V to 5.5V and 5.5V to 25V Input Voltage
- 0.6V to 5.5V Output Voltage (higher with external feedback resistors)
- SMBus Compliant I^2C Interface
- Full Power Monitoring and Reporting
- 3 x 15V Capable PSIO + 2 x GPIOs
- Full Start/Stop Sequencing Support
- Built-in Thermal, Over-Current, UVLO and Output Over-Voltage Protections
- On Board 5V and LDOOUT Standby LDOs
- On Board Non-Volatile Memory
- Supported by PowerArchitect™ 5.2 or later

APPLICATIONS

- Industrial Control Systems
- Automatic Test Equipment
- Video Surveillance Systems
- Automotive Infotainment

Ordering Information – back page

Typical Application



Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

VCCD, LDO5, LDOOUT, GLx, VOUTx.....-0.3V to 7.0V

ENABLE, V5EXT.....-0.3V to 7.0V

GPIO0/1, SCL, SDA.....6.0V

PSIO Inputs, BFB.....18V

DVDD, AVDD.....2.0V

VCC.....28V

LX#.....-1V to 28V

BSTx, GHx.....VLx + 6V

Storage Temperature.....-65°C to +150°C

Power Dissipation.....Internally Limited

Lead Temperature (Soldering, 10 sec).....300°C

ESD Rating (HBM - Human Body Model).....2kV

Operating Conditions

Input Voltage Range VCC.....5.5V to 25V

Input Voltage Range VCC = LDO5.....4.75V to 5.5V

VOUT1, 2, 3, 4.....5.5V

Junction Temperature Range.....-40°C to +125°C

JEDEC Thermal Resistance θ_{JA}.....32°C/W

Electrical Characteristics

Unless otherwise noted: T_J= 25°C, VCC = 5.5V to 25V, V5EXT open. Limits applying over the full operating temperature range are denoted by a "•"

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current							
I_{SUPPLY}	VCC Supply Current	SHUTDOWN EN = 0V, VCC = 12V			10	20	µA
		STANDBY I/Os programmed as inputs, VCC = 12V, EN = 5V			550	650	µA
		2ch PFM 2 channels on set at 5V, VOUT forced to 5.1V, no load, non-switching, ultra-sonic off, VCC = 12V, no I^2C activity			3.1		mA
		4ch PFM 4 channels on set at 5V, VOUT forced to 5.1V, no load, non-switching, ultra-sonic off, VCC = 12V, no I^2C activity			4.0		mA
		4ch PWM All channels enabled, f_{sw} = 600kHz, gate drivers unloaded, no I^2C activity			18		mA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{ENABLE}	ENABLE Turn On Threshold	VCC = 12V, Enable Rising		0.65		0.95	V
I_{LEAK}	ENABLE Pin Leakage Current	EN = 5V			3.6	10	µA
		EN = 0V		-10			µA
Input Voltage Range and Undervoltage Lockout							
VCC	VCC Range		•	5.5		25	V
		with VCC connected to LDO5	•	4.75		5.5	V
Voltage Feedback Accuracy and Output Voltage Set Point Resolution							
V_{A_VO}	VOUT Regulation Accuracy	Low Output Range 0.6 ≤ VOUT ≤ 1.6V, PWM operation		-5		5	mV
			•	-12.5		12.5	mV
		Mid Output Range 0.6 ≤ VOUT ≤ 3.2V, PWM operation		-10		10	mV
			•	-25		25	mV
		High Output Range 0.6 ≤ VOUT ≤ 5.5V, PWM operation		-20		20	mV
			•	-50		50	mV
V_{R_VO}	VOUT Regulation Range	Without external divider network	•	0.6		5.5	V
V_{NATIVE}	VOUT Native Set Point Resolution	Low Range			12.5		mV
		Mid Range			25		mV
		High Range			50		mV
V_{FINE}	VOUT Fine Set Point Resolution[1]	Low Range			2.5		mV
		Mid Range			5		mV
		High Range			10		mV
R_{IN}	VOUT Input Resistance	Low Range			120		kΩ
		Mid Range			80		kΩ
		High Range			65		kΩ
R_{IN}	VOUT Input Resistance in PFM	Low Range			10		MΩ
		Mid Range			1		MΩ
		High Range			0.67		MΩ
V_{SET_PG}	Power Good and OVP Set Point Range (from set point)	Low Range		-155		157.5	mV
		Mid Range		-310		315	mV
		High Range		-620		630	mV
V_{SET_PG}	Power Good and OVP Set Point Accuracy	Low Range		-5		5	mV
		Mid Range		-10		10	mV
		High Range		-20		20	mV
V_{SET_BF}	BFB Set Point Range			9		16	V
V_{RES_BF}	BFB Set Point Resolution				1		V
V_{A_BF}	BFB Accuracy			-0.5		0.5	V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Current and AUX ADC (Monitoring ADCs)							
V_{A_CS}	Current Sense Accuracy	Low Range (≤120mV), -60mV applied		-2.5	±1.25	2.5	mV
			•	-6.25		6.25	mV
		High Range (≤280mV), 150mV applied		-5	±2.5	5	mV
			•	-12.5		12.5	mV
INL_{CS}	Current Sense ADC INL				±0.4		LSB
DNL_{CS}	Current Sense DNL				±0.4		LSB
V_{SET_CS}	Current Limit Set Point Resolution and Current Sense ADC Resolution	Low Range (≤120mV)			1.25		mV
		High Range (≤280mV)			2.5		mV
V_{CS}	Current Sense ADC Range	Low Range (≤120mV)		-120		20	mV
		High Range (≤280mV)		-280		40	mV
V_{ADC_VO}	VOUT ADC Resolution	Low Range			15		mV
		Mid Range			30		mV
		High Range			60		mV
LSB_{ADC}	VOUT ADC Accuracy			-1		1	LSB
V_{ADC}	VCC ADC Range			4.6		25	V
V_{R_ADC}	VCC ADC Resolution				200		mV
V_{A_ADC}	VCC ADC Accuracy	VCC ≤ 20V		-1		1	LSB
T_{R_ADC}	Die Temp ADC Resolution				5		°C
T_{ADC}	Die Temp ADC Range	Output value is in Kelvin		-44		156	°C
Linear Regulators							
V_{O_LDO5}	LDO5 Output Voltage	5.5V ≤ VCC ≤ 25V 0mA < $I_{LDO5OUT}$ < 130mA, LDOOUT off	•	4.85	5.0	5.15	V
I_{CL_LDO5}	LDO5 Current Limit	LDO5 Fault Set	•	135	155	180	mA
	LDO5 UVLO	VCC Rising	•	4.6			V
	LDO5 PGOOD Hysteresis	VCC Falling			375		mV
	LDO5 Bypass Switch Resistance				1.1	1.5	Ω
	Bypass Switch Activation Threshold	V5EXT Rising, % of threshold setting	•	2.5		2.5	%
	Bypass Switch Activation Hysteresis	V5EXT Falling			150		mV
	LDOOUT Output Voltage	4.6V ≤ LDO5 ≤ 5.5V 0mA < I_{LDOOUT} < 50mA LDOOUT set to 3.3V	•	3.15	3.3	3.45	V
	LDOOUT Current Limit	LDOOUT Fault Set, LDOOUT set to 3.3V	•	50		85	mA
	Maximum total LDO loading during ENABLE start-up	ENABLE transition from logic low to high. Once LDO5 in regulation, above limits apply.				75	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PWM Generators and Oscillator							
f_{SW}	Switching Frequency Range	Steps defined in table		105		1230	kHz
	Switching Frequency Accuracy			-5		5	%
f_{CLKIN}	CLOCK IN Synchronization Frequency	When synchronizing to an external clock (Range 1)		20	25.7	31	MHz
		When synchronizing to an external clock (Range 2)		10	12.8	15.5	MHz
I^2C and GPIOs[2]							
V_{IL}	Input Pin Low Level					0.8	V
V_{IH}	Input Pin High Level			1.35			V
	Input Pin Leakage Current					1	µA
V_{OL}	Output Pin Low Level	I_{SINK} = 1mA				0.4	V
V_{OH}	Output Pin High Level	I_{SOURCE} = 1mA		2.4			V
		I_{SOURCE} = 0mA			3.3	3.6	V
	Output Pin High-Z Leakage Current (GPIO pins only)					10	µA
	Maximum Sink Current	Open Drain Mode				1	mA
	I/O Frequency					30	MHz
PSIOs[3]							
V_{IL}	Input Pin Low Level					0.8	V
V_{IH}	Input Pin High Level	PSIO0 and PSIO1		2			V
V_{IH}	Input Pin High Level	PSIO2		1.35			V
	Input Pin Leakage Current					1	µA
V_{OL}	Output Pin Low Level	I_{SINK} = 3mA				0.4	V
V_{OH}	Output Pin High Level	Open Drain. External pull-up resistor to user supply.				15	V
	Output Pin High-Z Leakage Current (PSIO pins only)					10	µA
	I/O Frequency					5	MHz
SMBus (I^2C) Interface							
V_{IL}	Input Pin Low Level	V_{IO} = 3.3V ±10%				$0.3V_{IO}$	V
V_{IH}	Input Pin High Level	V_{IO} = 3.3V ±10%		$0.7V_{IO}$			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	V_{IO} = 3.3V ±10%		0.05 V_{IO}			V
V_{OL}	Output Pin Low Level (open drain or collector)	I_{SINK} = 3mA				0.4	V
I_{LEAK}	Input Leakage Current	Input is between $0.1V_{IO}$ and $0.9V_{IO}$		-10		10	µA

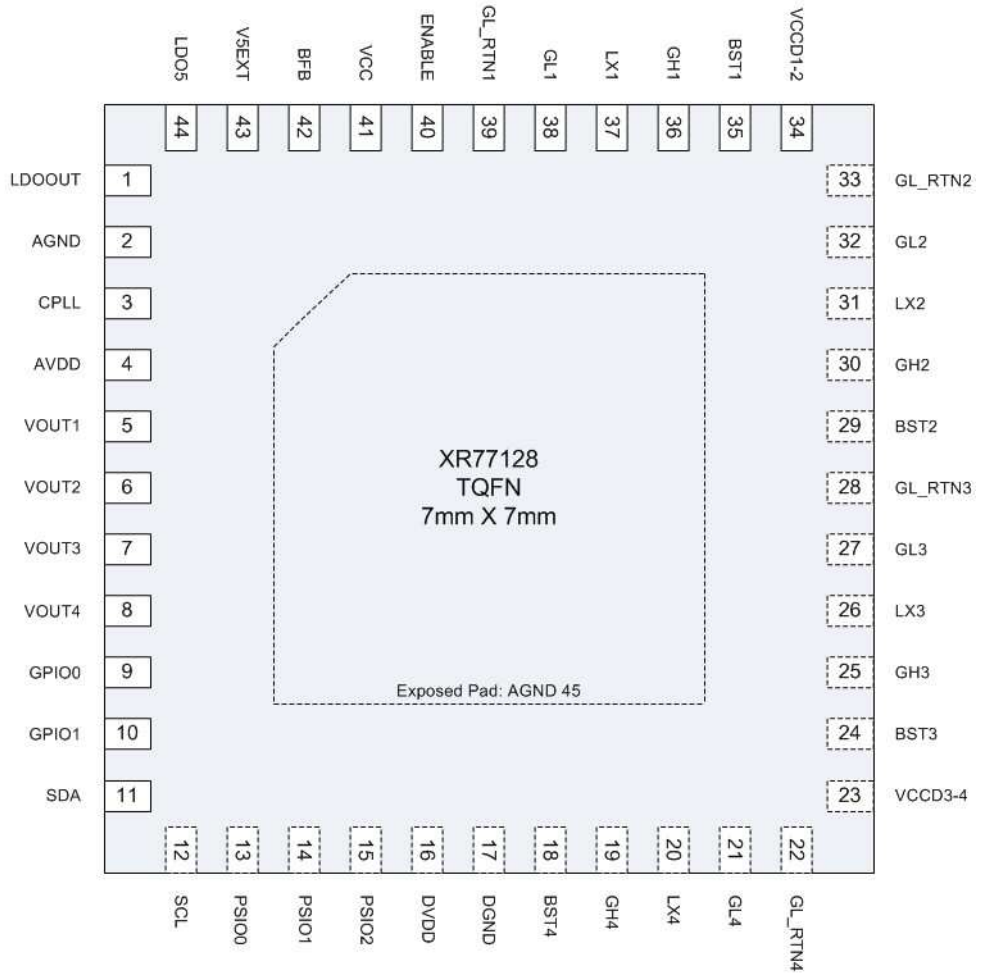
Symbol	Parameter	Conditions		Min	Typ	Max	Units
	Output Fall Time from V_{IHmin} to V_{IL-max}	With a bus capacitance (C_b) from 10pF to 400pF		20 + 0.1C_b		250	ns
	Internal Pin Capacitance					1	pF
Gate Drivers							
	GH, GL Rise Time	At 10-90% of full scale, 1nF Cload			17		ns
	GH, GL Fall Time	At 10-90% of full scale, 1nF Cload			11		ns
	GH, GL Pull-Up On-State Output Resistance				4.35	5	Ω
	GH, GL Pull-Down On-State Output Resistance				1.96	2.5	Ω
	GH, GL Pull-Down Off-Mode Resistance	VCC = VCCD = 0V			48		kΩ
	Bootstrap Diode Forward Resistance	at 10mA			8.5		Ω
	Minimum On-Time	1nF of gate capacitance			50		ns
	Minimum Off-Time	1nF of gate capacitance			125		ns
	Minimum Programmable Dead Time	Does not include dead time variation from driver output stage, T_{SW} = switching period			20		ns
	Maximum Programmable Dead Time				T_{SW}		
	Programmable Dead Time Adjustment Step	103MHz internal clock frequency			607		ps

Note 1: Fine Set Point Resolution not available in PFM

Note 2: 3.3V CMOS logic compatible, 5V tolerant

Note 3: 3.3V/5.0V CMOS logic compatible, maximum rating of 15.0V

Pin Configuration



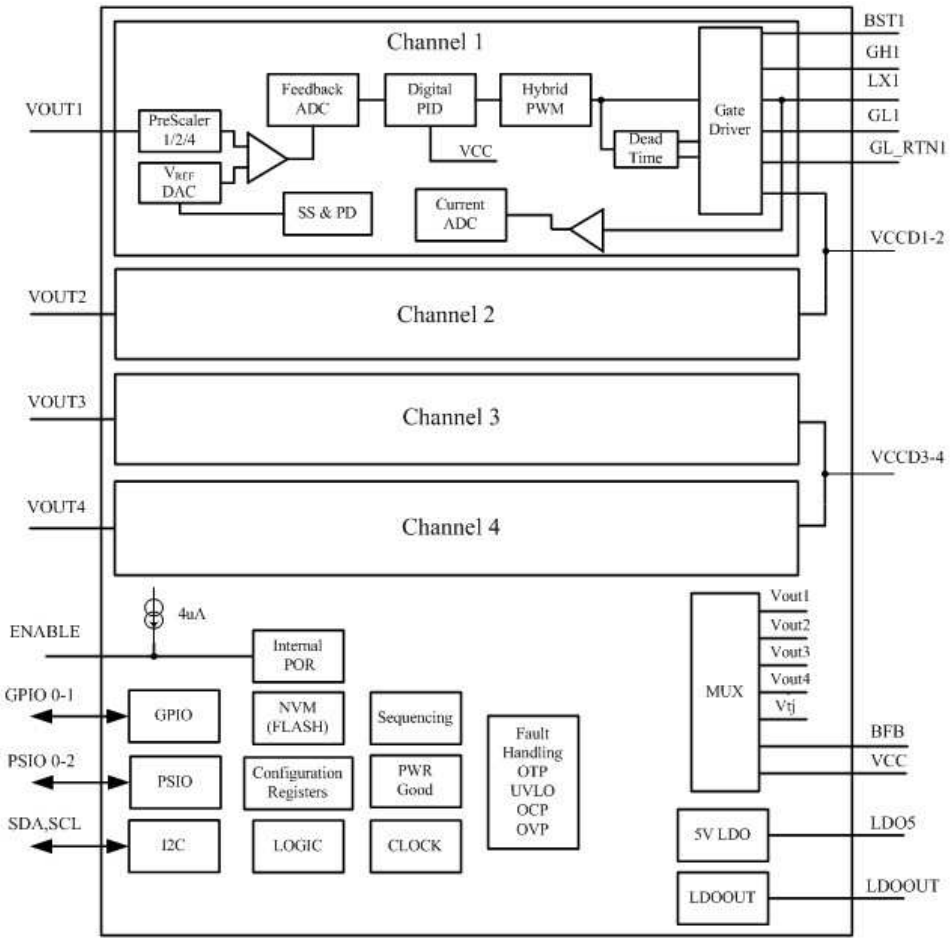
Pin Assignments

Pin No.	Pin Name	Description
1	LDOOUT	Output of the standby LDO. This is a micro power LDO that needs to be configured or commanded to turn on.
2	AGND	Analog ground pin. This is the small signal ground connection.
3	CPLL	Connect to a 2.2nF capacitor to GND.
4	AVDD	Output of the internal 1.8V LDO. A decoupling capacitor should be placed between AVDD and AGND close to the chip.
5, 6, 7, 8	VOUT1, VOUT2, VOUT3, VOUT4	Connect to the output of the corresponding power stage.The output is sampled at least once every switching cycle.
9,10	GPIO0, GPIO1	These pins can be configured as inputs or outputs to implement custom flags, power good signals, enable/disable controls and synchronization to an external clock.
11, 12	SDA, SCL	SMBus/I^2C serial interface communication pins.

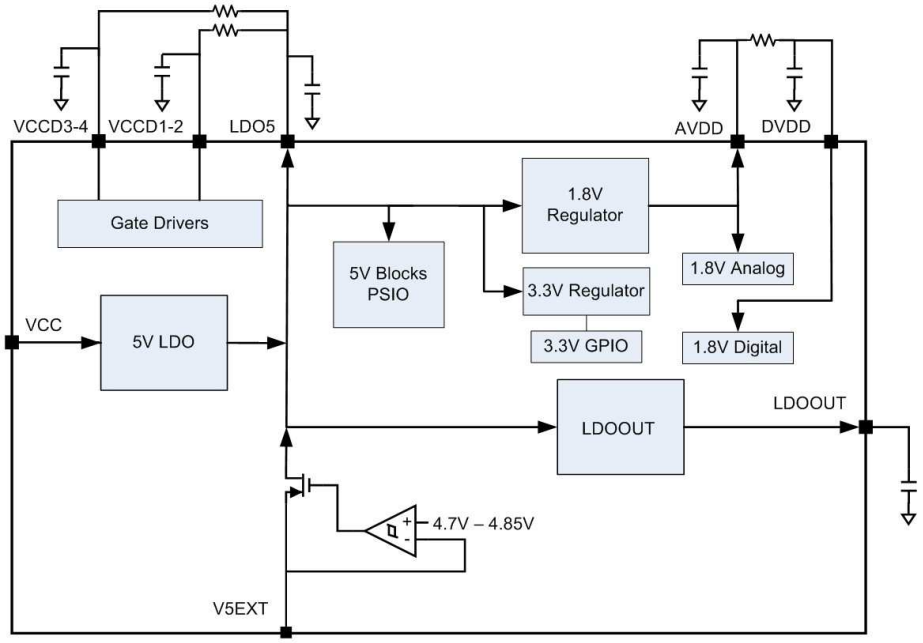
Pin No.	Pin Name	Description
13, 14, 15	PSIO0, PSIO1, PSIO2	Open drain, these pins can be used to control external power MOSFETs to switch loads on and off, shedding the load for fine grained power management. They can also be configures as standard logic outputs or inputs just as any of the GPIOs can be configured, but as open drains require an external pull-up when configured as outputs.
16	DVDD	1.8V supply input for digital circuitry. Connect pin to AVDD. Place a decoupling capacitor close to the controller IC.
17	DGND	Digital ground pin. This is the logic ground connection, and should be connected to the ground plane close to the PAD.
18, 24, 29, 35	BST4, BST3, BST2, BST1	High side driver supply pin(s). Connect BST to the external capacitor as shown in the Typical Application Circuit. The high side driver is connected between the BST pin and LX pin and delivers the BST pin voltage to the high side FET gate each cycle.
19, 25, 30, 36	GH4, GH3, GH2, GH1	Output pin of the high side gate driver. Connect directly to the gate of an external N-channel MOSFET.
20, 26, 31, 37	LX4, LX3, LX2, LX1	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFETs and the inductor. These pins are also used to measure voltage drop across bottom MOSFETs in order to provide output current information to the control engine.
21, 27, 32, 38	GL4, GL3, GL2, GL1	Output pin of the low side gate driver. Connect directly to the gate of an external N-channel MOSFET.
22, 28, 33, 39	GL_RTN4, GL_RTN3, GL_RTN2, GL_RTN1	Ground connection for the low side gate driver. This should be routed as a signal trace with GL. Connect to the source of the low side MOSFET.
23, 34	VCCD3-4, VCCD1-2	Gate Drive supply. Two independent gate drive supply pins where pin 34 supplies drivers 1 and 2 and pin 23 supplies drivers 3 and 4. One of the two pins must be connected to the LDO5 pin to enable two power rails initially. It is recommended that the other VCCD pin be connected to the output of a 5V switching rail (for improved efficiency or for driving larger external FETs), if available, otherwise this pin may also be connected to the LDO5 pin. A bypass capacitor (>1uF) to the system ground is recommended for each VCCD pin with the pin(s) connected to LDO5 with shortest possible length of etch.
40	ENABLE	If ENABLE is pulled high or allowed to float high, the chip is powered up (logic is reset, registers configuration loaded, etc.). The pin must be held low for the XR77128 to be placed into shutdown.
41	VCC	Input voltage. Place a decoupling capacitor close to the controller IC. This input is used in UVLO fault generation.
42	BFB	Input from the 15V output created by the external boost supply. When this pin goes below a pre-defined threshold, a pulse is created on the low side drive to charge this output back to the original level. If not used, this pin should be connected to GND.
43	V5EXT	External 5V that can be provided. If one of the output channels is configured for 5V, then this voltage can be fed back to this pin for reduced operating current of the chip and improved efficiency.
44	LDO5	Output of a 5V LDO. This LDO is used to power the internal Analog Blocks.
45	PAD	This is the die attach paddle, which is exposed on the bottom of the part. Connect externally to the ground plane.

Functional Block Diagram

XR77128 Block Diagram



LDO Block Diagram



Typical Performance Characteristics

Unless otherwise noted: VCC = 12V, T_A = 25°C

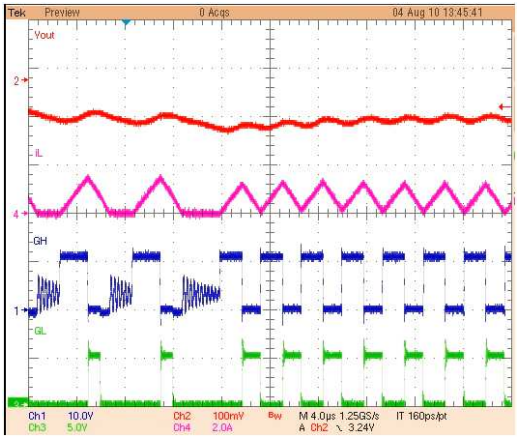


Figure 1: PFM to PWM Transition

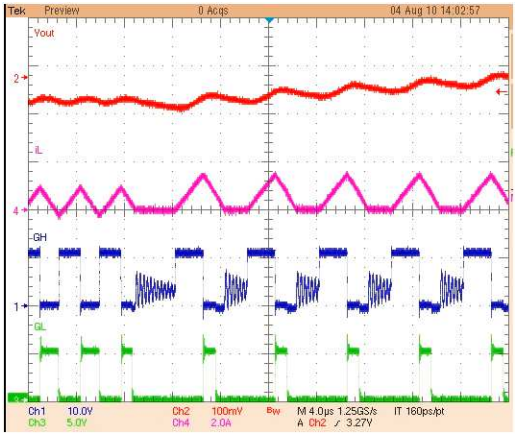


Figure 2: PWM to PFM Transition

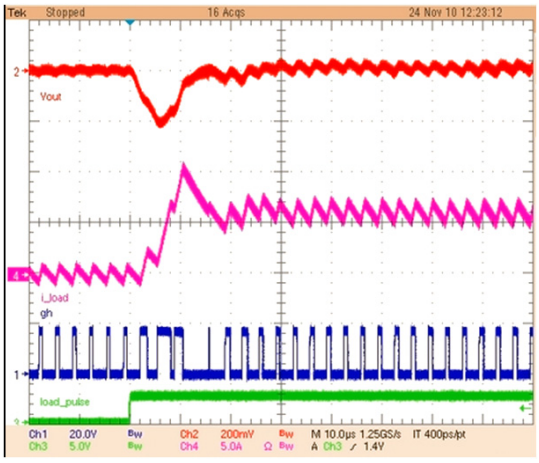


Figure 3: 0-6A Transient 300kHz PWM only

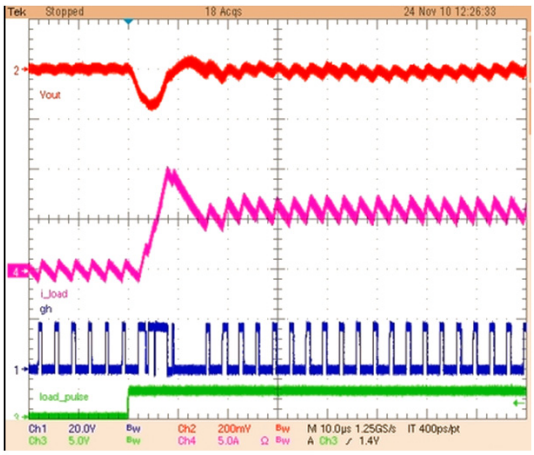


Figure 4: 0-6A Transient 300kHz with OVS +/-5%

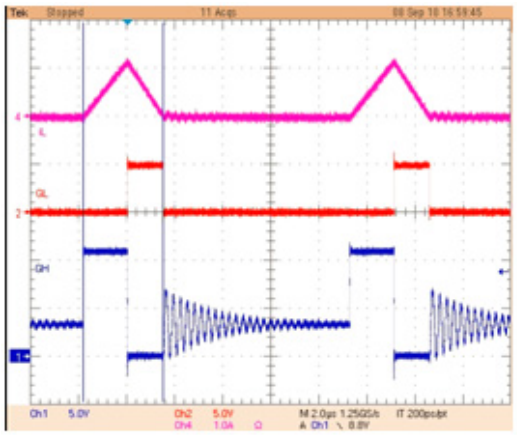


Figure 5: PFM Zero Current Accuracy

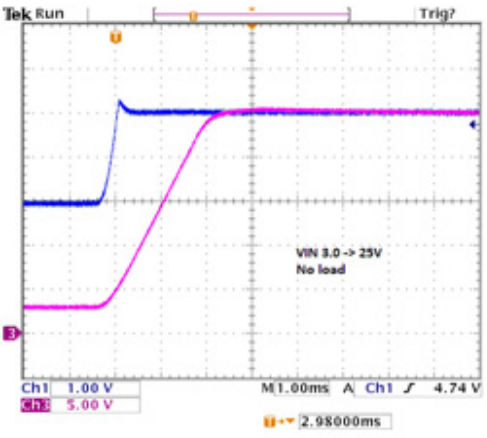


Figure 6: LDO5 Brown Out Recovery, No Load

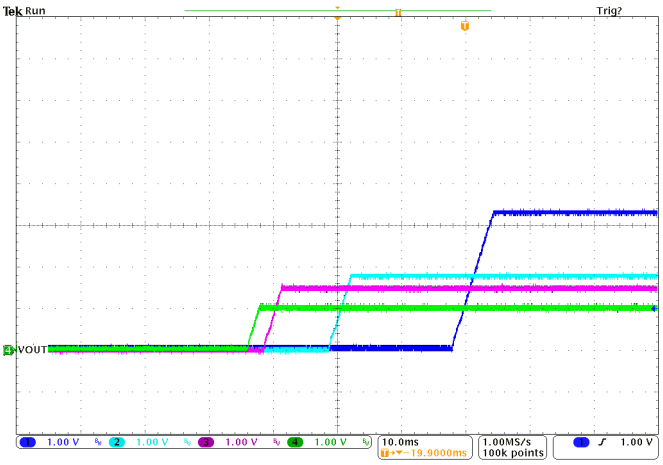


Figure 7: Sequential, Conditional Start-Up

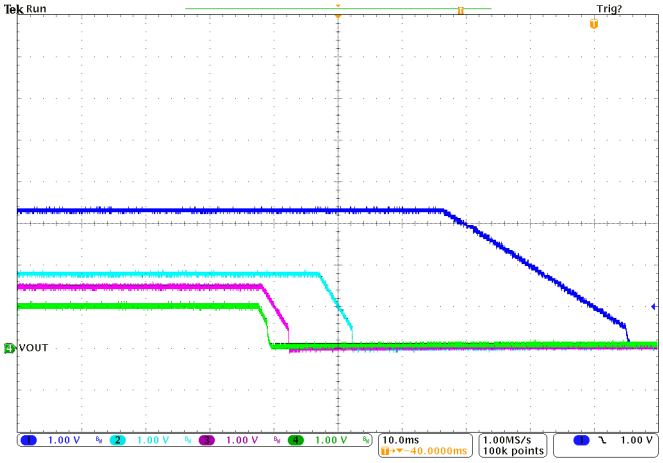


Figure 8: Sequential, Conditional Shut-Down

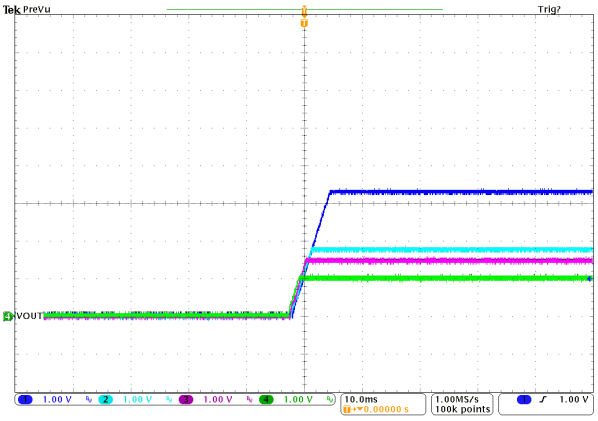


Figure 9: Simultaneous Start-Up

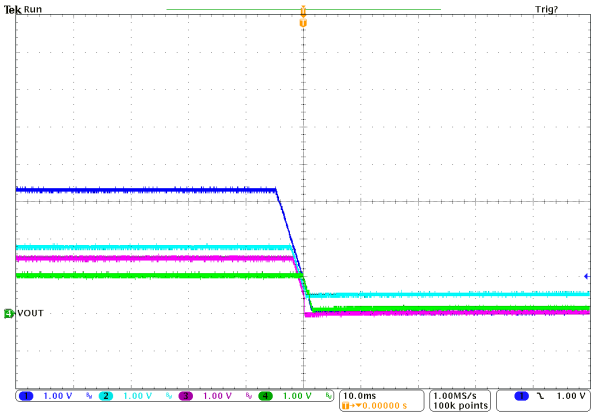


Figure 10: Simultaneous Shut-Down

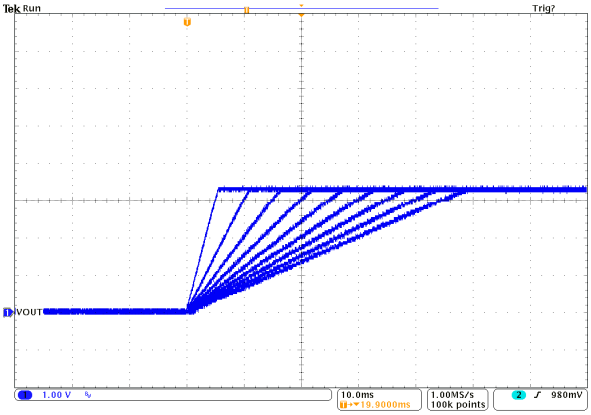


Figure 11: Ramp-Up Rate Dynamic Sweep

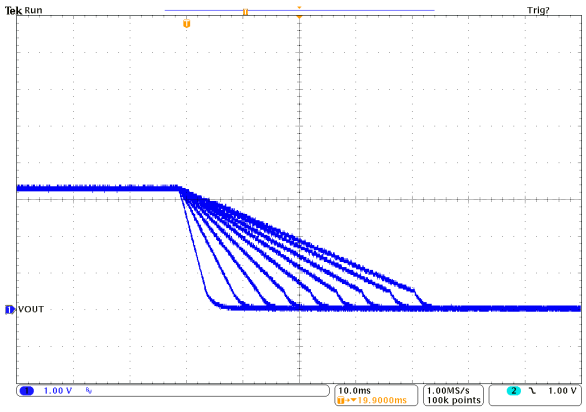


Figure 12: Ramp-Down Rate Dynamic Sweep

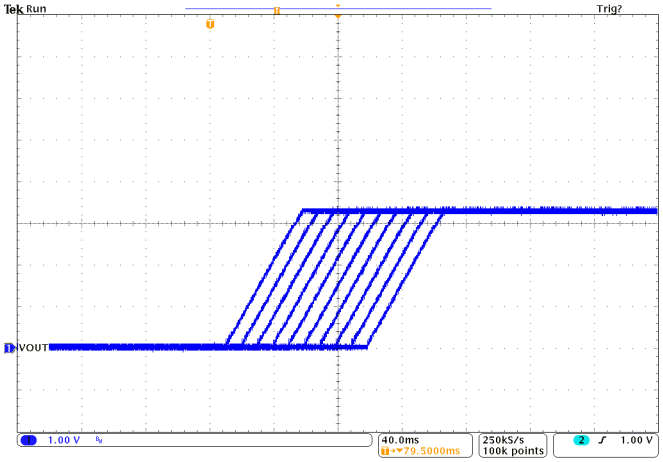


Figure 13: Start-Up Delay Dynamic Sweep

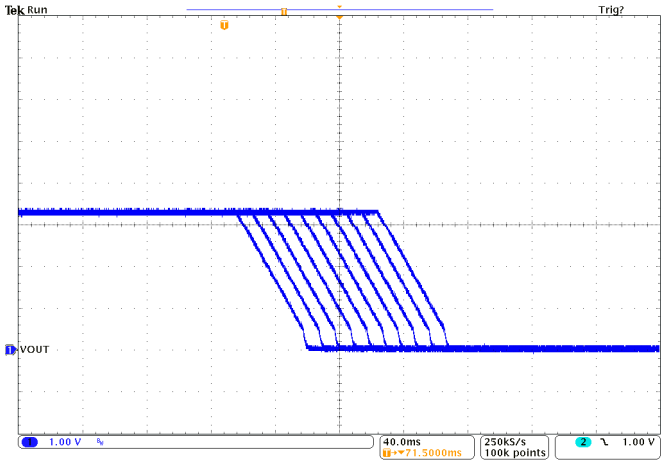


Figure 14: Shut-Down Delay Dynamic Sweep

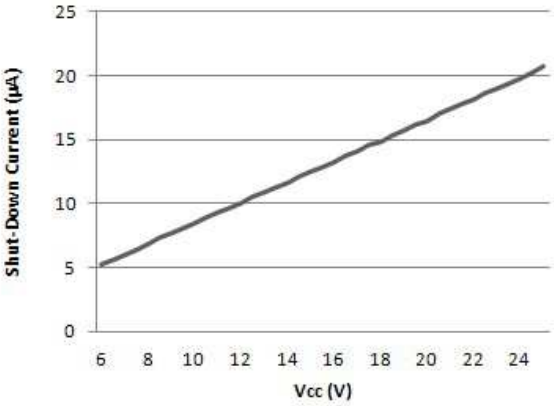


Figure 15: Shut-Down Current Versus VCC

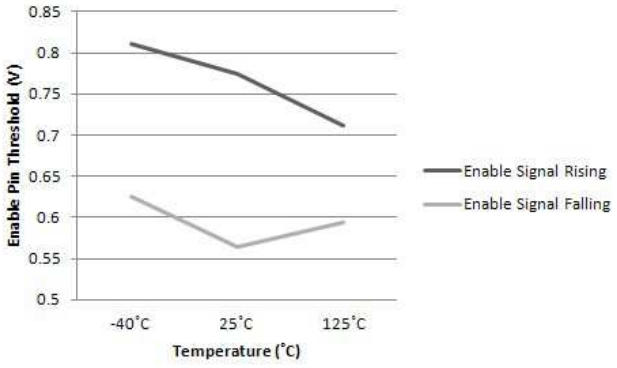


Figure 16: Enable Threshold Over Temperature at VCC=12V

Functional Description

Overview

The XR77128 is a quad-output digital pulse width modulation (PWM) controller with integrated gate drivers for use with synchronous buck switching regulators. Each output voltage can be programmed from 0.6V to 5.5V without the need for an external voltage divider. The wide range of programmable PWM switching frequency (from 105 kHz to 1.2 MHz) enables the user to optimize for efficiency or component sizes. Since the digital regulation loop requires no external passive components, loop performance is not compromised due to external component variation or operating condition.

The XR77128 provides a number of critical safety features such as Over-Current Protection (OCP), Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), plus input Under-Voltage Lockout (UVLO). In addition, it has a number of key health monitoring features such as warning level flags for the safety functions, Power Good (PGOOD), etc., plus full monitoring of system voltages and currents. The above are all programmable and/or readable from the SMBus and many are steerable to the IOs for hardware monitoring.

For hardware communication, the XR77128 has two logic level General Purpose Input-Output (GPIO) pins and three 15V, open drain, Power System Input-Output (PSIO) pins. Two pins are dedicated to the SMBus data (SDA) and clock (SCL). Additional pins include Chip Enable (Enable), Aux Boost Feedback (BFB) and External PLL Capacitor (CPLL).

In addition to providing four switching outputs, the XR77128 also provides control for an Aux boost supply, and two stand-by linear regulators for a total of seven customer usable supplies in a single device.

The 5V LDO is used for internal power and is also available for customer use to power external circuitry. LDOOUT is solely for customer use and is not used by the chip. There is also a 1.8V linear regulator which is for internal use only and should not be used externally.

A key feature of the XR77128 is its advanced power management capabilities. All four outputs are independently programmable and provide the user full control of the delay, ramp, and sequence during power up and power down. The user may also control how the outputs interact and power down in the event of a fault. This includes active ramp down of the output voltages to remove an output voltage as quickly as possible. Another useful feature is that the outputs can be defined and controlled as groups.

The XR77128 has two main types of programmable memory. The first type is runtime registers that contain configuration, control and monitoring information for the chip. The second type is rewritable Non-Volatile Flash Memory that is used for permanent storage of the configuration data along with various chip internal functions. During power up, the run time registers are loaded from the flash memory allowing for standalone operation.

The XR77128 brings an extremely high level of functionality and performance to a programmable power system. Ever decreasing product budgets require the designer to quickly make good cost/performance tradeoffs to be truly successful. By incorporating 4 switching channels, two user LDOs, a charge pump boost controller, along with internal gate drivers, all in a single package, the XR77128 allows for extremely cost effective power system designs. Another key cost factor that is often overlooked is the unanticipated Engineering Change Order (ECO). The programmable versatility of the XR77128, along with the lack of hard wired configuration components, allows for minor and major changes to be made in circuit by simple reprogramming.

Regulation Loops

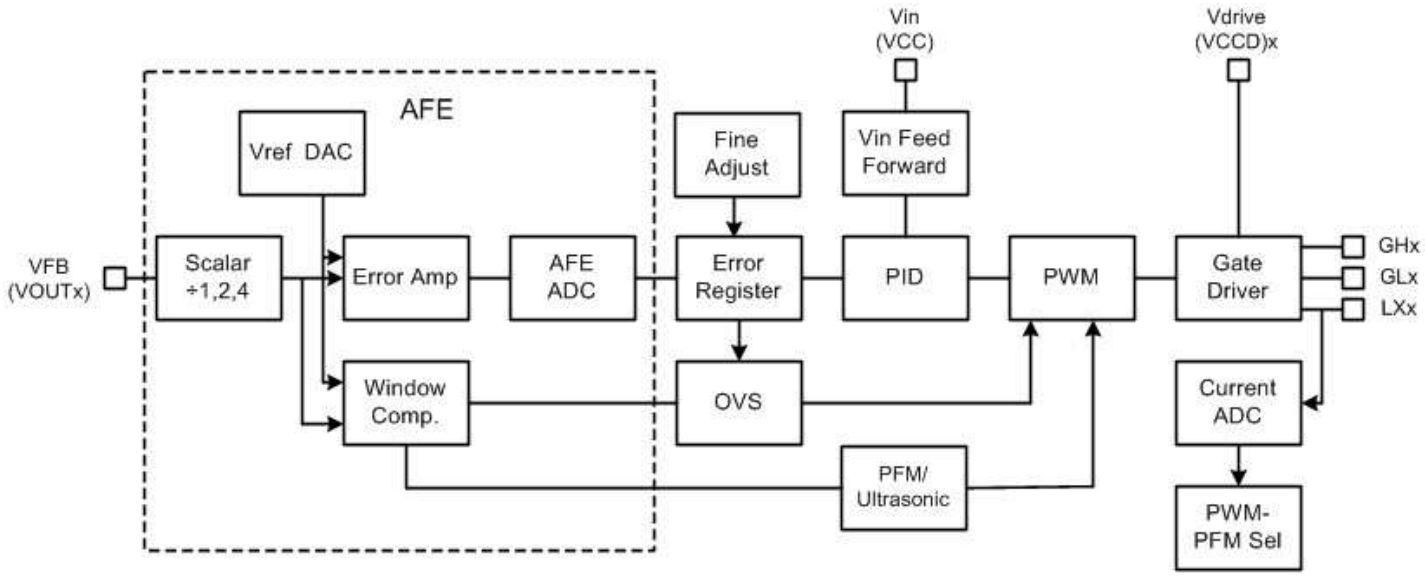


Figure 17: Regulation Loops

Figure 17 shows a simplified functional block diagram of the regulation loops for one output channel of the XR77128. There are four separate parallel control loops: Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), Ultrasonic, and Over Sampling (OVS). Each of these loops is fed by the Analog Front End (AFE) as shown at the left of the diagram. The AFE consist of an input voltage scaler, a programmable Voltage Reference (Vref) DAC, Error Amplifier, and a window comparator. Some of the functional blocks are common and shared by each channel by means of a multiplexer.

PWM Loop

The PWM loop operates in Voltage Control Mode (VCM) with optional Vin feed forward based on the voltage at the VCC pin. The reference voltage (Vref) for the error amp is created by a 0.15V to 1.6V DAC that has a 12.5mV resolution. In order to provide a 0.6V to 5.5V output voltage range, an input scaler is used to reduce feedback voltages for higher output voltages to bring them within the 0.15V to 1.6V control range. So for output voltages up to 1.6V (low range), the scaler has a gain of 1. For output voltages from 1.6V to 3.2V (mid range) the scalar gain is 1/2, and for voltages greater than 3.2V (high range) the gain is 1/4. This results in the low range having a reference voltage resolution of 12.5mV, the mid range having a resolution of 25mV, and the high range having a resolution of 50mV. The error amp has a gain of 4 and compares the output voltage of the scaler to Vref to create an error voltage on its output. This is converted to a digital error term by the AFE ADC and is stored in the error register. The error register has a fine adjust function that can be used to improve the output voltage set point resolution by a factor of 5 resulting in a low range resolution of 2.5mV, a mid range resolution of 5mV and a high range resolution of 10mV. The output of the error register is then used by the Proportional Integral Derivative (PID) controller to manage the loop dynamics.

The XR77128 PID is a 17-bit five-coefficient control engine that calculates the required duty cycle under the various operating conditions and feeds it to the digital Pulse Width Modulator (PWM). Besides the normal coefficients, the PID also uses the VCC voltage to provide a feed forward function.

The XR77128 digital PWM includes a special delay timing loop that provides a timing resolution that is 16 times the master oscillator frequency (103MHz) for a timing resolution of 607ps for both the driver pulse width and dead time delays. The PWM produces the Gate High (GH) and Gate Low (GL) signals to the driver. The maximum and minimum on times and dead time delays are programmable by configuration resisters.

To provide current information, the output inductor current is measured by a differential amplifier that reads the voltage drop across the RDSON of the synchronous FET during its on time. There are two selectable ranges, a low range with a gain of 8 for a -120mV to +20mV voltage range, and a high range with a gain of 4 for -280mV to +40mV voltage range. The optimum range to use will depend on the maximum output current and the RDSON of the synchronous FET. The measured voltage drop is then converted to a digital value by the current ADC block. The resulting current

value is stored in a readable register and also used to determine when PWM to PFM transitions should occur.

PFM Loop

The XR77128 has a PFM loop that can be enabled to improve efficiency at light loads. By reducing switching frequency and operating in the discontinuous conduction mode (DCM), both switching and conduction losses are minimized.

Figure 18 shows a functional diagram of the PFM logic.

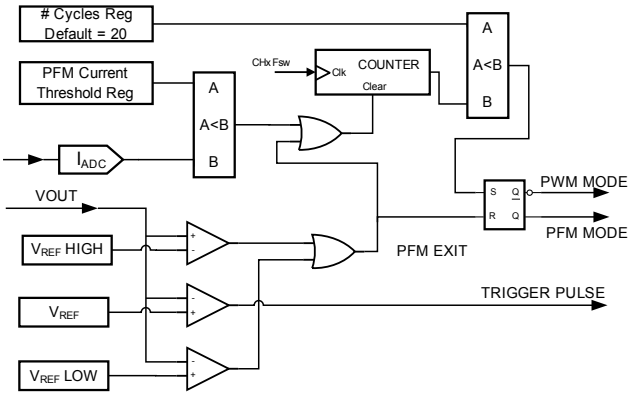


Figure 18: PFM Enter/Exit Functional Diagram

The PFM loop works in conjunction with the PWM loop and is entered when the output current falls below a programmed threshold level for a programmed number of cycles. When PFM mode is entered, the PWM loop is disabled and instead, the scaled output voltage is compared to Vref with a window comparator. The window comparator has three thresholds; normal (Vref), high (Vref + %high) and low (Vref - %low). The %high and %low values are programmable and track Vref.

In PFM mode, the normal comparator is used to regulate the output voltage. If the output voltage falls below the Vref level, the comparator is activated and triggers the PWM to start a switching cycle. When the switching FET is turned on, the inductor current ramps up which charges up the output capacitors and increases their voltage. After the completion of the high side and low side on-times, the synchronous FET is turned off to inhibit any inductor reverse current flow. The load current then discharges the output capacitors until the output voltage falls below Vref and the normal comparator is activated. This triggers the PWM to start the next switching cycle. The time from the end of the switching cycle to the next trigger is referred to as the dead zone. When PFM mode is initially entered, the switching cycle is equal to the steady-state PWM duty cycle.This will cause the inductor ripple current to be at the same level that is in PWM mode of operation. During operation the PFM duty cycle is calculated based on the ratio of the output voltage to VCC. This method ensures that the output voltage ripple is well controlled and is much lower than in other architectures which use a “burst” methodology.

If the output voltage ever goes outside the high/low windows, PFM mode is exited and the PWM loop is reactivated.

Although the PFM mode is effective at improving efficiency at light load, at very light loads the dead zone time can increase to the point where the switching frequency can enter the audio hearing range. When this happens some components, like the output inductor and ceramic capacitors, can emit audible noise. The amplitude of the noise depends mainly on the board design and on the manufacturer and construction details of the components. Proper selection of components can reduce the sound to very low levels. In general Ultrasonic Mode is not used unless required as it reduces light load efficiency.

Ultrasonic Mode

Ultrasonic mode is an extension of PFM to ensure that the switching frequency never enters the audible range. When this mode is entered, the switching frequency is set to 30kHz and the duty cycle of the switching and synchronous FETs which are fixed in PFM mode, are decreased as required to keep the output voltage in regulation while maintaining the 30kHz switching frequency.

Under extremely light or zero load currents, the GH on time pulse width can decrease to its minimum width. When this happens, the synchronous FET on time is increased slightly to allow a small amount of reverse inductor current to flow back into Vin to keep the output voltage in regulation while maintaining the switching frequency above the audio range.

Oversampling (OVS) Mode

Oversampling (OVS) mode is a feature added to the XR77128 to improve transient responses. This mode can only be enabled when the channel switching frequency is operating in 1x frequency mode. In OVS mode, the output voltage is sampled 4 times per switching cycle and is monitored by the AFE window comparator. If the voltage goes outside the set high or low limits, the OVS control electronics can immediately modify the pulse width of the GH or GL drivers to respond accordingly without having to wait for the next cycle to start. OVS has two types of response depending on whether the high limit is exceeded during an unloading transient (Over Voltage), or the low limit is exceeded during a loading transient (Under Voltage).

Under Voltage OVS: If there is an increasing current load step, the output voltage will drop until the regulator loop adapts to the new conditions to return the voltage to the correct level. Depending on where in the switching cycle the load step happens there can be a delay of up to one switching cycle before the control loop can respond. With OVS enabled if output voltage drops below the lower limit of the window comparator, an immediate GH pulse will be generated and sent to the driver to increase the output inductor current toward the new load level without having to wait for the next cycle to begin. If the output voltage is still below the lower limit of the window comparator at the beginning of the next cycle, OVS will work in conjunction with the PID to insert additional GH pulses to quickly return the output voltage back within its regulation band. The result of this system is transient response capabilities on par or exceeding those of a constant on-time control loop.

Over Voltage OVS: When there is a step load current decrease, the output voltage will increase (bump up) as the excess inductor current that is no longer used by the load, flows into the output capacitors causing the output voltage to rise. The voltage will continue to rise until the inductor current decreases to the new load current level. With OVS enabled, if the output voltage exceeds the high limit of the window comparator, a blanking pulse is generated to truncate the GH signal. This causes inductor current to immediately begin decreasing to the new load level. The GH signal will continue to be blanked until the output voltage falls below the high limit of the window comparator. Again, since the output voltage is sampled at four times the switching frequency, overshoot will be decreased and the time required to get back into the regulation band is also decreased.

OVS can be used in conjunction with both the PWM and PFM operating modes. When it is activated it can noticeably decrease output voltage excursions when transitioning between PWM and PFM modes.

Internal Drivers

The internal high and low gate drivers use totem pole FETs for high drive capability. They are powered by two external 5V power pins (VCCD1-2) and (VCCD3-4). VCCD1-2 powers the drivers for channels 1 and 2 while VCCD3-4 powers channels 3 and 4. The drivers can be powered by the internal 5V LDO by connecting their power pins to the LDO5 output through an RC filter to avoid conducted noise back into the analog circuitry.

To minimize power dissipation in the 5V LDO, it is recommended to power the drivers from an external 5V power source either directly or by using the V5EXT input. Good quality 1uF to 4.7uF capacitors should be connected directly between the power pins to ground to optimize driver performance and minimize noise coupling to the 5V LDO supply.

The driver outputs should be connected directly to their corresponding output switching FETs with the Lx output connected to the drain of the synchronous FET for the best current monitoring accuracy.

See ANP-32 “Practical Layout Guidelines for PowerXR Designs”

LDOs

The XR77128 has two internal Low Drop Out (LDO) linear regulators that generate 5.0V (LDO5) and configurable voltage (LDOOUT) for both internal and external use. XR77128 can be programmed to four LDOOUT output voltage settings, 3.3V, 2.8V, 2.5V and 1.8V. Additionally, XR77128 has a 1.8V regulator that supplies power for the XR77128 internal circuits. LDO5 is the main power input to the device and is supplied by an external 5.5V to 25V (VCC) supply. The output of LDO5 should be bypassed by a good quality 4.7uF or larger capacitor connected between the pin and ground close to the device. The 5V output is used by the XR77128 as a standby power supply and is also used to power the LDOOUT and 1.8V linear regulators inside the chip, and can also supply power to the 5V gate drivers. The total output current that the 5V LDO can provide is 130mA. The XR77128 consumes approximately 20mA and the rest is shared between LDOOUT and the gate drive currents.

The LDOOUT output available on the LDOOUT pin is solely for customer use and is not used internally. This supply is turned on or off by the configuration registers. Again a good bypass capacitor should be used.

The AVDD pin is the 1.8V regulator output and needs to be connected externally to the DVDD pin on the device. A good quality capacitor should be connected between this pin and ground close to the package.

Clocks and Timing

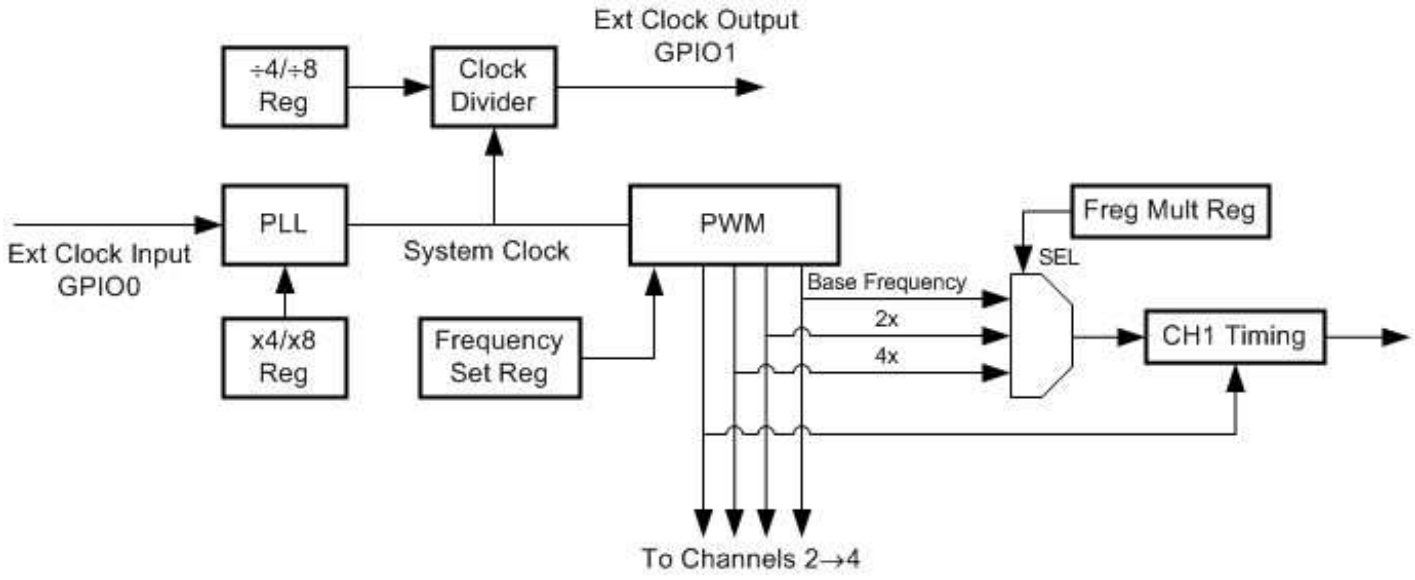


Figure 19: XR77128 Timing Block Diagram

Figure 19 shows a simplified block diagram of the XR77128 timings. Again, please note that the function blocks and signal names used are chosen for ease of understanding and do not necessarily reflect the actual device design.

The system timing is generated by a 103MHz internal system clock (Sys_Clk). There are two ways that the 103 MHz system clock can be generated. These include an internal oscillator and a Phase Locked Loop (PLL) that is synchronized to an external clock input. The basic timing architecture is to divide the Sys_Clk down to create a fundamental switching frequency (Fsw_Fund) for all the output channels that is settable from 105kHz to 306kHz. The switching frequency for a channel (Fsw_CHx) can then be selected as 1 time, 2 times or 4 times the fundamental switching frequency.

To set the base frequency for the output channels, an "Fsw_Set" value representing the base frequency shown in Table 1 is entered into the switching frequency configuration register. Note that Fsw_Set value is basically equal to the Sys_Clk divided by the base frequency. The system timing is then created by dividing down Sys_Clk to produce a base frequency clock, 2X and 4X times the base frequency clocks, and sequencing timing to position the output channels relative to each other. Each output channel then has its own frequency multiplier register that is used to select its final output switching frequency.

Table 1 shows the available channel switching frequencies for the XR77128 device. In practice the PowerArchitect™ 5.2 (PA 5.2) design tool handles all the details and the user only has to enter the fundamental switching frequency and the 1x, 2x, 4x frequency multiplier for each channel.

If an external clock is used, the frequencies in this table will shift according to percentage of frequency deviation between the clock supplied and nominal value for a given locking range.

Table 1: Available Channel Switching Frequencies

Base Frequency (kHz)	Available 2x Frequencies (kHz)	Available 4x Frequencies (kHz)
105.5	211.1	422.1
107.3	214.6	429.2
109.1	218.2	436.4
111.0	222.0	444.0
112.9	225.9	451.8
115.0	229.9	459.8
117.0	234.1	468.2
119.2	238.4	476.9
121.5	242.9	485.8
123.8	247.6	495.2
126.2	252.5	504.9
128.8	257.5	515.0
131.4	262.8	525.5
134.1	268.2	536.5
137.0	273.9	547.9
139.9	279.9	559.8
143.1	286.1	572.2
146.3	292.6	585.2
149.7	299.4	598.8
153.3	306.5	613.1
157.0	314.0	628.0
160.9	321.9	643.8
165.1	330.1	660.3
169.4	338.8	677.6
174.0	348.0	695.9
178.8	357.6	715.3
183.9	367.9	735.7
189.3	378.7	757.4
195.1	390.2	780.3
201.2	402.3	804.7
207.7	415.3	830.6
214.6	429.2	858.3
222.0	444.0	887.9
229.9	459.8	919.6

Table 1: Available Channel Switching Frequencies

Base Frequency (kHz)	Available 2x Frequencies (kHz)	Available 4x Frequencies (kHz)
238.4	476.9	953.7
247.6	495.2	990.4
257.5	515.0	1030.0
268.2	536.5	1072.9
279.9	559.8	1119.6
292.6	585.2	1170.5
306.5	613.1	1226.2

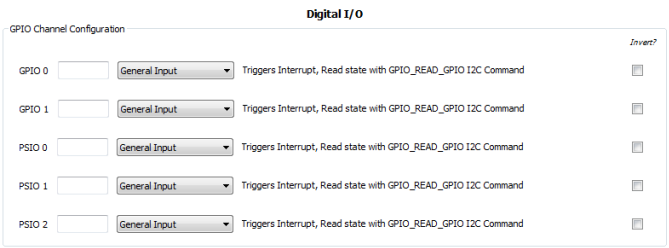
Note: Some table entries are affected by rounding.

Supervisory and Control

Power system design with XR77128 is accomplished using PowerArchitect™ design tool version 5.2 or later (PA 5.2). All figures referenced in the following sections are taken from PA 5.2. Furthermore, the following sections reference I^2C commands. For more information on these commands refer to ANP-38.

Digital I/O

XR77128 has two General Purpose Input Output (GPIO) and three Power System Input Output (PSIO) user configurable pins.

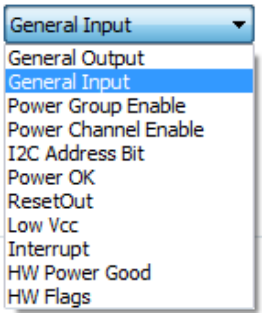


- GPIOs are 3.3V CMOS logic compatible and 5V tolerant.
- PSIOs configured as outputs are open drain and require external pull-up resistors. These I/Os are 3.3V and 5V CMOS logic compatible, and up to 15V capable.

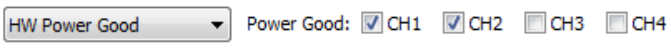
The polarity of the GPIO/PSIO pins is set in PA 5.2 or with an I^2C command.

Configuring GPIO/PSIOs

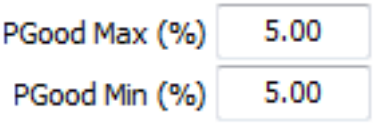
The following functions can be controlled from or forwarded to any GPIO/PSIO:



- **General Output** – set with an I^2C command
- **General Input** – triggers an interrupt; state read with an I^2C command
- **Power Group Enable** – controls enabling and disabling of channels placed in Group 1and Group 2
- **Power Channel Enable** – controls enabling and disabling of a individual channel including LDOOUT
- **I^2C Address Bit** – controls an I^2C address bit
- **Power OK** – indicates that selected channels have reached their target levels and have not faulted. Multiple channel selection is available in which case the resulting signal is the AND logic function of all channels selected
- **ResetOut** – is delayed Power OK. Delay is programmable in 5ms increments with the range of 0 to 255ms. When no channels selected, the transition will indicate the controller has finished the booting process and is ready to communicate.
- **Low VCC** – indicates when VCC has fallen below the UVLO fault threshold and when the UVLO condition clears (VCC voltage rises above the UVLO warning level)
- **Interrupt** – the controller generated interrupt selection and clearing is done through I^2C commands
- **HW Power Good** – the Power Good hardware monitoring function. It is an output voltage monitoring function that is a hardware comparison of channel output voltage against its user defined Power Good threshold limits (Power Good minimum and maximum levels). It has no hysteresis. Multiple channel selection will be combined using the AND logic function of all channels selected.



The Power Good minimum and maximum levels are expressed as percentages of the target voltage.



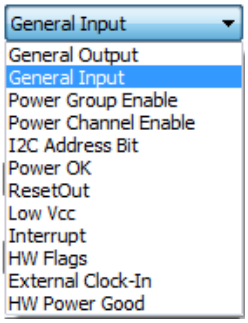
"PGood Max" is the upper window and "PGood Min" is the lower window. The minimum and maximum for each of these values can be calculated with the following equation:

$$\text{PGOOD (\%)} = \frac{N \times \text{LSB (mV)} \times 10^5}{\text{Vtarget (V)}}$$

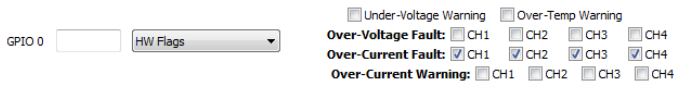
Where N=1 to 63 for the PGood Max value, and N=1 to 62 for the PGood Min value. For example, with the target voltage of 1.5V and set point resolution of 2.5mV (LSB), the Power Good Min and Max values can range from 0.17% to 10.50% respectively. A user can effectively double the Power Good range by changing to the next higher output voltage range setting, but at the expense of reduced set point resolution.

Interrupt, Low VCC, Power OK and ResetOut signals can only be forwarded to a single GPIO/PSIO.

In addition, the following are functions that are unique to GPIO0 and GPIO1.

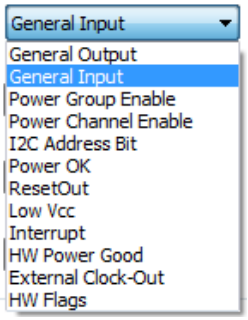


- **HW Flags** – these are hardware monitoring functions forwarded to GPIO0 only. The functions include Under-Voltage Lockout Warning, Over-Temperature Warning, Over-Voltage Fault, Over-Current Fault and Over-Current Warning for every channel. Multiple selections will be combined using the OR logic selected function.



A subset of hardware flags which includes Under-Voltage Lockout Warning, Over-Temperature Warning, and Over-Voltage Fault for every channel is available on the other I/Os.

- **External Clock-In** – enables the controller to lock to an external clock including one from another XR77128 applied to the GPIO0 pin. There are two ranges of clock frequencies the controller accepts, selectable by a user.



- **External Clock-Out** – clock sent out through GPIO1 for synchronizing with another XR77128 (see the clock out section for more information).

Fault Handling

There are seven different types of fault handling in XR77128:

- **Under Voltage Lockout (UVLO)** monitors voltage supplied to the VCC pin and will cause the controller to shutdown all channels if the supply drops to critical levels.
- **Over Temperature Protection (OTP)** monitors temperature of the chip and will cause the controller to shutdown all channels if temperature rises to critical levels.
- **Over Voltage Protection (OVP)** monitors regulated voltage of a channel and will cause the controller to react in a user specified way if the regulated voltage surpasses threshold level.
- **Over Current Protection (OCP)** monitors current of a channel and will cause the controller to react in a user specified way if the current level surpasses threshold level.
- **Start-up Time-out Fault** monitors whether a channel gets into regulation in a user defined time period.
- **LDO5 Over Current Protection (LDO5 OCP)** monitors current drawn from the regulator and will cause the controller to be reset if the current exceeds LDO5 limit.
- **LDOOUT Over Current Protection (LDOOUT OCP)** monitors current drawn from the regulator and will cause the controller to shut down the regulator if the current exceeds LDOOUT limit.

UVLO

Both UVLO warning and fault levels are user programmable and set at 200mV increments in PA 5.2.

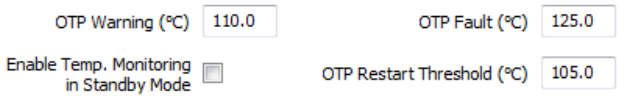
When the warning level is reached the controller will generate the UVLO_WARNING_EVENT interrupt. In addition, the host can be informed about the event through HW Flags (see the Digital I/O section).

When an UVLO fault condition occurs, the XR77128 outputs are shut down and the UVLO_FAULT_ACTIVE_EVENT interrupt is generated. In addition, the host can be informed by forwarding the Low VCC signal to any GPIO/PSIO (see the Digital I/O section). This signal transitions when the UVLO fault occurs. When coming out of the fault, rising VCC crossing the UVLO fault level will trigger the UVLO_FAULT_INACTIVE_EVENT interrupt.

Once UVLO condition clears (VCC voltage rises to or above the user defined UVLO warning level), the Low VCC signal will transition and the controller will be reset.

OTP

User defined OTP warning, fault and restart levels are set at 5°C increments in PA 5.2.



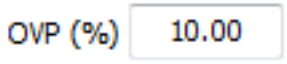
When the warning level is reached the controller will generate the TEMP_WARNING_EVENT interrupt. In addition, the host can be informed about the event through HW Flags (see the Digital I/O section).

When an OTP fault condition occurs, the XR77128 outputs are shutdown and the TEMP_OVER_EVENT interrupt is generated.

Once temperature reaches a user defined OTP Restart Threshold level, the TEMP_UNDER_EVENT interrupt will be generated and the controller will reset.

OVP

A user defined OVP fault level is set in PA 5.2 and is expressed in percentages of a regulated target voltage.



Resolution is the same as for the target voltage (expressed in percentages). The OVP minimum and maximum values are calculated by the following equation where the range for N is 1 to 63:

$$\text{OVP (\%)} = \frac{N \times \text{LSB (mV)} \times 10^5}{\text{Vtarget (V)}}$$

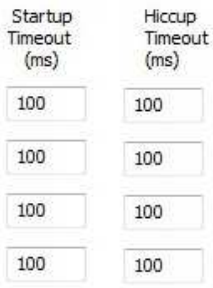
When the OVP level is reached and the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I^2C command to check which channel is at fault.

In addition, OVP fault can be monitored through any I/O.

A user can choose one of three options in response to an OVP event: to shutdown the faulting channel, to shut down faulting channel and to perform auto-restart of the channel, or to restart the chip.

Choosing the “Restart Chip” option during development is not recommended as it makes debug efforts difficult.

For the case of Shutdown and Auto-restart Channel, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 ms increments with a maximum value of 255 ms.



Note: The Channel Fault Action response is the same for an OVP or OCP event.

OCP

A user defined OCP fault level is set with 10mA increments in PA 5.2. PA 5.2 uses calculations to give the user the approximate DC output current entered in the current limit field. However, the actual current limit trip value programmed into the part is limited to 280mV as defined in the electrical characteristics. The maximum value the user can program is limited by RDSON of the synchronous Power FET and current monitoring ADC range. For example, using a synchronous FET with RDSON of 30mΩ and the wider ADC range, the maximum current limit programmed would be:

$$\text{OCP Max (A)} = \frac{280mV}{30m\Omega} = 9.33A$$

XR77128 samples current approximately 30ns before the synchronous FET turns off, so the actual measured DC output current in this example would be 9.33A plus approximately half the inductor ripple.

The output current reported by the XR77128 is processed through a seven sample median filter in order to reduce noise.

When the OCP level is reached and the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I^2C command to check which channel is at fault.

In addition, OCP fault can be monitored through HW Flags on GPIO0. The host can also monitor OCP warning flag through HW Flags on GPIO0. The OCP warning level is calculated by PA 5.2 as 85% of the OCP fault level.

A user can choose one of three options in response to an OCP event: shut down the faulting channel, shut down the faulting channel and perform auto-restart of the channel, or restart the chip.

Choosing the “Restart Chip” option during development is not recommended as it makes debug efforts difficult.

For the case of Shutdown and Auto-restart Channel, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 ms increments with a maximum value of 255 ms.

Note: The Channel Fault Action response is the same for an OCP or OVP event.

Start-up Time-out Fault

A channel will be at Startup Timeout Fault if it does not come up in the time period specified in the “Startup Timeout” box.

When the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the con-

troller. The host then can use an I²C command to check which channel is at fault.

LDO5 OCP

When current is drawn from LDO5 that exceeds LDO5 current limit, the controller gets reset.

LDOOUT OCP

When current drawn from LDOOUT exceeds LDOOUT current limit the regulator gets shut down, a fault is generated, and the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can through an I²C command check which channel/regulator is at fault. Once the fault condition is removed, the host needs to turn the regulator on again.

V5EXT Switchover and Control

The XR77128 has a function called V5EXT that allows an external 5V power supply to be used to supply its internal 5V (LD05) housekeeping voltage instead of using its internal 5V LDO. This function can notably reduce the controller's power dissipation and improve overall system operating efficiency (particularly in the PFM mode).

When enabled in PA5.2, LD05 will automatically switch over to the external supply and disable the internal LDO when the V5EXT voltage reaches a programmable threshold voltage. The switchover thresholds are programmable in 50mV steps with a total range of 200mV. Hysteresis to switch the external 5 Volt supply in and out is 150mV. LDO5 automatically turns off when the external voltage is switched in. This is referred to as Forward Transfer.

There are two voltage sequencing requirements to use the V5EXT function:

1. Power On - The chip's VCC voltage has to be applied prior to the V5EXT voltage. If the V5EXT voltage however is present before VCC is applied, adding a simple logic FET to the V5EXT input will meet this requirement. This is described in detail in the "Operating from a System 5V" section.

2. Power Off - Once the forward transfer is complete, the controller's internal circuits are then operating on the external 5V supply, so the V5EXT voltage has to remain in regulation, above the switchover threshold, as long as any output is operating. Once all outputs are disabled the V5EXT supply can be turn off (Off Last). This will ensure that no false faults are indicated during shutdown.

When using V5EXT, an additional good quality 22uF capacitor needs to be placed from the LDO5 pin to ground to filter out any potential noise from getting into the internal analog blocks.
If the V5EXT function is not used, the V5EXT pin should be either grounded or left floating, in conjunction with making sure the function gets disabled through PA 5.2.

Operating from a Generated 5V Output

It is recommended when using the 5VEXT function, that the 5V rail be generated by one of the XR77128 outputs and routed back to the V5EXT pin. This meets the Power On sequence requirement. Power down sequencing requires that the V5EXT supply remains on until the all outputs are powered down. Therefore, the 5V rail should be defined in PA 5.2 as the last to be shut down. If the 5V output has no requirement for being actively shut down, then set the "Active Shutdown Threshold" to 5V.

Operating from a System 5V

The system 5V rail must be regulated to a value of 5V, -5%/+10% and the V5EXT switchover threshold must be set to 4.8V in PA 5.2.
VCC must be applied to the chip before connecting the System 5V to the V5EXT pin. If the system 5V rail is an always on rail, a simple way to meet the Power On sequencing requirement is to add a logic NFET, with the Source connected to the V5EXT pin, the Gate to VCC pin and the Drain to the system 5V supply. For proper operation the VCC input voltage must be greater than 5V plus the NFET threshold voltage. In this configuration, the ENABLE pin of the XR77128 should be left floating. Again the V5EXT supply has to remain on until all the output have been turned off.

Fault Management

Fault management settings, when V5EXT is XR77128 generated require, that the other three rails follow the 5V rail if it faults. There are three fault actions the 5V rail may take: "Shutdown Channel", "Shutdown and Auto-restart Channel", and "Restart Chip". If "Shutdown Channel" is selected, outside interaction is required to restart the 5V and the other three rails. This may be through I²C, I/Os or VCC power cycling. If "Shutdown and Auto-restart Channel" is selected, to restart the other channels, an I/O should be assigned as HW Power Good or Power OK for the 5V output and connected to a second I/O configured to "Enable" for the other three outputs. Lastly, "Restart Chip" is the simplest to use for auto recovery.

Fault management settings when using the system 5V for V5EXT require that all outputs have OVP set to 5% with fault action set to “Restart Chip”.

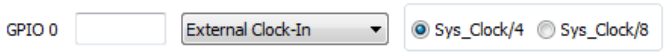
External Clock Synchronization

XR77128 can be run off an external clock available in the system or another XR77128. The external clock must be in the ranges of 10MHz to 15.5MHz or 20MHz to 31MHz. Locking to the external clock is done through an internal Phase Lock Loop (PLL) which requires an external loop capacitor of 2.2nF to be connected between the CPLL pin and AGND.

In applications where this functionality is not desired, the CPLL capacitor is not necessary and can be omitted, and the pin shall be left floating. In addition, the user needs to make sure the function gets disabled through register settings.

The external clock must be routed to GPIO0. The GPIO0 setting must reflect the range of the external clock applied to it: Sys_Clock/8 corresponds to the range of 10MHz to 15.5MHz while Sys_Clock/4 setting corresponds to the range of 20Mhz to 31MHz.

The functionality is enabled in PA 5.2 by selecting External Clock-in function under GPIO0.

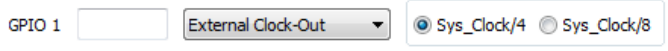


When the controller switches over to the external clock, the PLL_LOCK_IN interrupt is generated to inform the host. To the contrary, when the controller switches back to the internal clock source, the PLL_LOCK_OUT interrupt gets generated.

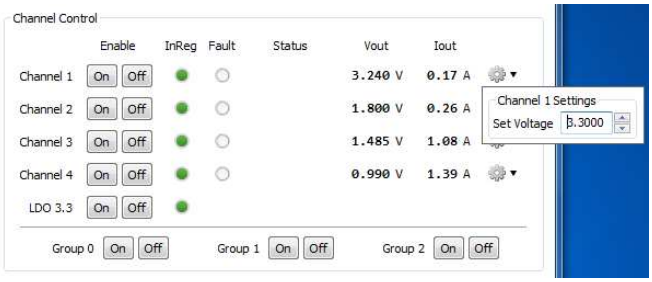
Clock Out

XR77128 can supply clock out to be used by another XR77128 controller. The clock is routed out through GPIO1 and can be set to the system clock divided by 8 (Sys_Clock/8) or the system clock divided by 4 (Sys_Clock/4) frequencies.

The functionality is enabled in PA 5.2 by selecting External Clock-Out function under GPIO1.



Channel Control



Channels including LDOOUT can be controlled independently by any GPIO/PSIO or I^{2}C command. Channels will start-up or shut-down following transitions of signals applied to GPIO/PSIOs set to control the channels. The control can always be overridden with an I^{2}C command.

Regardless of whether the channels are controlled independently or are in a group, the ramp rates will be followed as specified (see the Power Sequencing section).

Regulated voltages and voltage drops across the synchronous FET on each switching channel can be read back using I^{2}C commands. The regulated voltage read back resolution is 15mV, 30mV and 60mV per LSB depending on the target voltage range. The voltage drop across the synchronous FET read back resolution is 1.25mV and 2.5mV per LSB depending on the range.

Through an I^{2}C command the host can check the status of the channels; whether they are in regulation or at fault.

Regulated voltages can be dynamically changed on switching channels using I^{2}C commands with resolution of 2.5mV, 5mV and 10mV depending on the target voltage range (in PWM mode only).

For more information on I^{2}C commands refer to ANP-38, or contact Exar or your local Exar representative.

Power Sequencing

All four channels and LDOOUT can be grouped together and will start-up and shut-down in a user defined sequence.

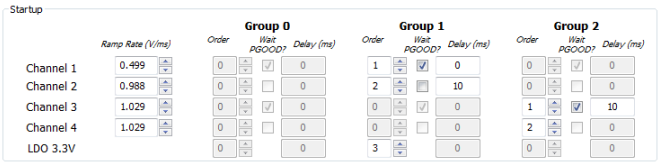
Selecting none means channel(s) will not be assigned to any group and therefore, will be controlled independently.

Group Selection

There are three groups:

- **Group 0** – is controlled by the chip ENABLE or an I^2C command. Channels assigned to this group will come up with the ENABLE signal being high (plus additional delay needed to load a configuration from Flash memory to run-time registers), and will go down with the ENABLE signal being low. The control can always be overridden with an I^2C command.
- **Group 1** – can be controlled by any GPIO/PSIO or an I^2C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I^2C command.
- **Group 2** – can be controlled by any GPIO/PSIO or an I^2C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I^2C command.

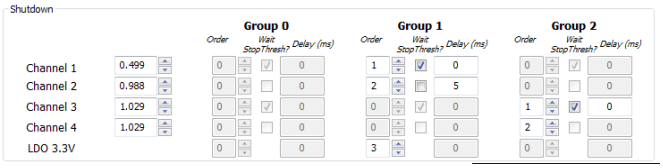
Start-up



For each channel within a group a user can specify the following start-up characteristics:

- **Ramp Rate** – expressed in Volts per milliseconds. It does not apply to LDOOUT.
- **Order** – position of a channel to come-up within the group
- **Wait PGOOD?** – selecting this option for a channel means the next channel in the order will not start ramping-up until this channel reaches the target level and its Power Good flag is asserted.
- **Delay** – an additional time delay a user can specify to postpone a channel start-up with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0ms to 255ms.

Shut-down



For each channel within a group a user can specify the following shut-down characteristics:

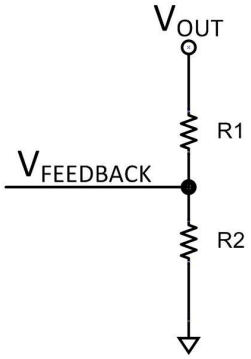
- **Ramp Rate** – expressed in Volts per milliseconds. It does not apply to LDOOUT.
- **Order** – position of a channel to come-down within the group
- **Wait Stop Thresh?** – selecting this option for a channel means the next channel in the order will not start ramping down until this channel reaches the Stop Threshold level.
- **Delay** – additional time delay a user can specify to postpone a channel shut-down with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0ms to 255ms.

Monitoring VCC and Temperature

Through I^2C commands, the host can read back voltage applied to the VCC pin and the die temperature respectively. The VCC read back resolution is 200mV per LSB; the die temperature read back resolution is 5C° per LSB. For more on I^2C commands refer to ANP-38.

Regulating Higher than 5.5V

To set the output voltage higher than 5.5V, the user needs to add an external voltage divider. The resistors used in the voltage divider should be below 20kΩ. In practice, the PA 5.2 design tool handles all the details and the user only has to enter the desired output voltage. The PA 5.2 tool will recommend resistor divider values which can be modified by the user.



External Driver Mode

XR77128 may be configured to drive external DrMOS or similar devices using the GL pin. Although not supported by PA 5.2 as of this publication date, future releases will support this feature. Exar's technical support team can provide assistance to enable the feature.

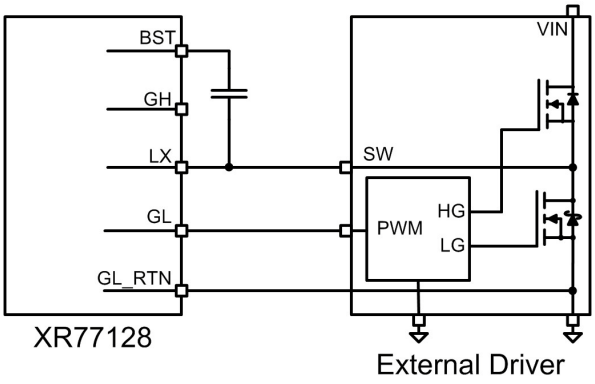
When the controller is in external driver mode, the PWM signal is internally routed to the GL pin and can be used to directly drive the PWM input of DrMOS devices according

to the interface schematics shown below. The GH pin is not used in this mode and needs to be left floating.

Connecting the LX pin to the switch node and the GL_RTN pin to the PGND (synchronous MOSFET source) of the DrMOS device allows current monitoring, Over-Current Warning and Over-Current Fault operation. The boost cap must be connected between the LX and BST pins to ensure proper biasing of the internal circuitry.

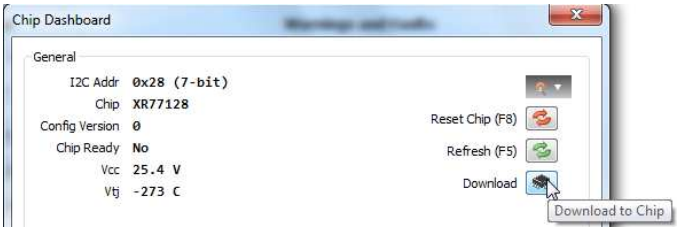
If current monitoring is not needed, the LX pin should be grounded. The boost cap will be connected between the BST and LX pins.

The PWM output is a 5V signal and does not support tri-state. Only CCM operation is recommended. When setting the Active Shutdown Threshold level, using a low value (100mV for instance) to discharge the output capacitors and avoid a possibility of a negative ring on the output during shut down is recommended.



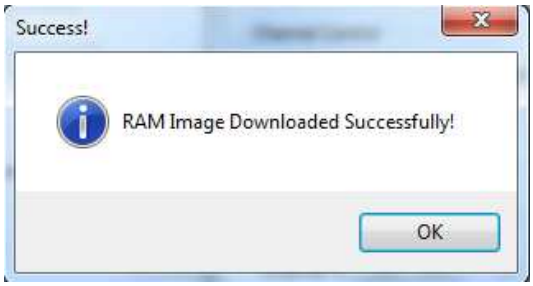
Downloading Configuration to XR77128

A key benefit of Exar's programmable power technology is the ability to easily update the design and chip configuration during development. The best way to do this is to program the RAM memory rather than programming the FLASH NVM.



PA 5.2 provides a RAM download function accessible through the Dashboard or through the "Tools" menu.

RAM programming requires that there is no valid configuration in the FLASH NVM. A valid configuration is loaded in the chip if in the Dashboard window, the "Reset Chip" (F8) button is clicked and after a short delay the "Chip Ready" indicates "Yes". When a new configuration is loaded into RAM with a chip that already contains a valid configuration in FLASH NVM, the first step will be to invalidate the FLASH configuration. The device will be reset to clear the prior RAM content and then the new run time configuration gets loaded. PA 5.2 will indicate that it successfully downloaded the configuration to run time registers after which the "Chip Ready" indicator will be asserted by PA 5.2 acting as a host.



If the configuration changes I^2C address, the device will respond to the new address at this point.

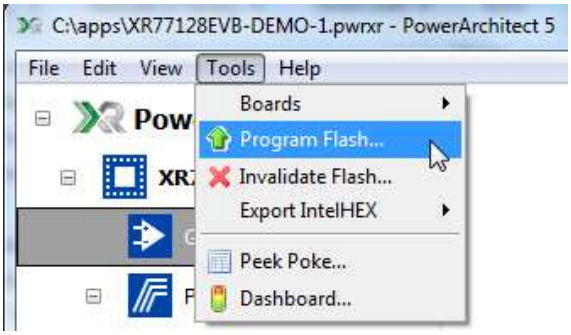
For users that wish to create their own downloading procedure, they can refer to ANP-39.

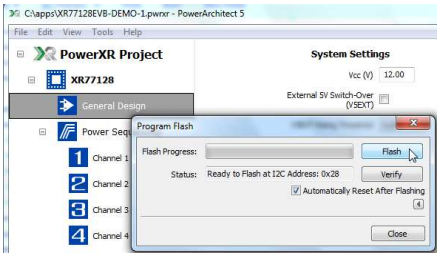
Programming XR77128

Once the design has been tested and verified its configuration can permanently be saved into FLASH NVM.

XR77128 is a Flash based device which means its configuration can be programmed into Flash NVM and re-programmed a number of times.

Programming of FLASH NVM is done through PA 5.2.





By clicking on the Flash button, user will start programming sequence of the design configuration into the Flash NVM. After the programming sequence completes, the chip will