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XR82C684

CMOS Quad Channel UART (QUART)

September 1999-2

FEATURES

- Four Full-Duplex, Independent Channels
- Asynchronous Receiver and Transmitter
- Quadruple-Buffered Receivers and Transmitters
- Programmable Stop Bits in 1/16 bit increments
- Pin Selectable “88” and “68 Mode”
- Internal Bit Rate Generators with more than 33 Bit Rates
- Independent Bit Rate Selection for each Transmitter and Receiver
- External Clock Capability
- Maximum Bit Rate: 1X clock - 1Mb/s, 16X clock - 125 kb/s
- Normal, AUTOECHO, Local LOOPBACK and Remote LOOPBACK Modes
- Two Multi-function 16-bit Counter/Timers
- Interrupt Output with Sixteen Maskable Interrupt Conditions
- Interrupt Vector Output on Acknowledge
- Programmable Interrupt Daisy Chain (Z-Mode Operation only)
- 16 General Purpose Output pins
- 16 General Purpose Input pins with Change of States Detectors on 8 Inputs
- Multi-drop Mode Compatible with 8051 Nine Bit Mode
- On-chip Oscillator for Crystal
- Standby Mode to Reduce Operating Power
- Advanced CMOS Low Power Technology

GENERAL DESCRIPTION

The EXAR Quad Universal Asynchronous Receiver and Transmitter (QUART) is a data communications device that provides four fully independent full-duplex asynchronous communication channels in a single package. The QUART is designed for use in microprocessor based systems and may be used in a polled or interrupt-driven environment.

The XR82C684 device offers a single IC solution for various microprocessor families. The “88” and “68 modes” (for the 8800 and 68000 family of processors, respectively) can be selected by tying the SEL pin to V_{DD} or V_{SS}.

The QUART is fabricated using advanced two layer metal, with a high performance density EPI/CMOS 1.8• process to provide high performance and low power consumption, and is packaged in a 44 pin PLCC and a 68 pin PLCC.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR82C684CJ/44	44 pin PLCC	0°C to 70°C
XR82C684CJ	68 pin PLCC	0°C to 70°C
XR82C684J/44	44 pin PLCC	-40°C to 85°C
XR82C684J	68 pin PLCC	-40°C to 85°C

PRINCIPLES OF OPERATION

Figure 1 and *Figure 2* present an overall block diagram of the QUART when operating in the 68 and 88 Modes, respectively. As illustrated in these block diagrams, the QUART consists of the following major functional blocks:

- Data Bus Buffer
- Interrupt Control
- Input Port
- Serial Communication Channels A, B, C, and D
- Operation Control
- Timing Control
- Output Port

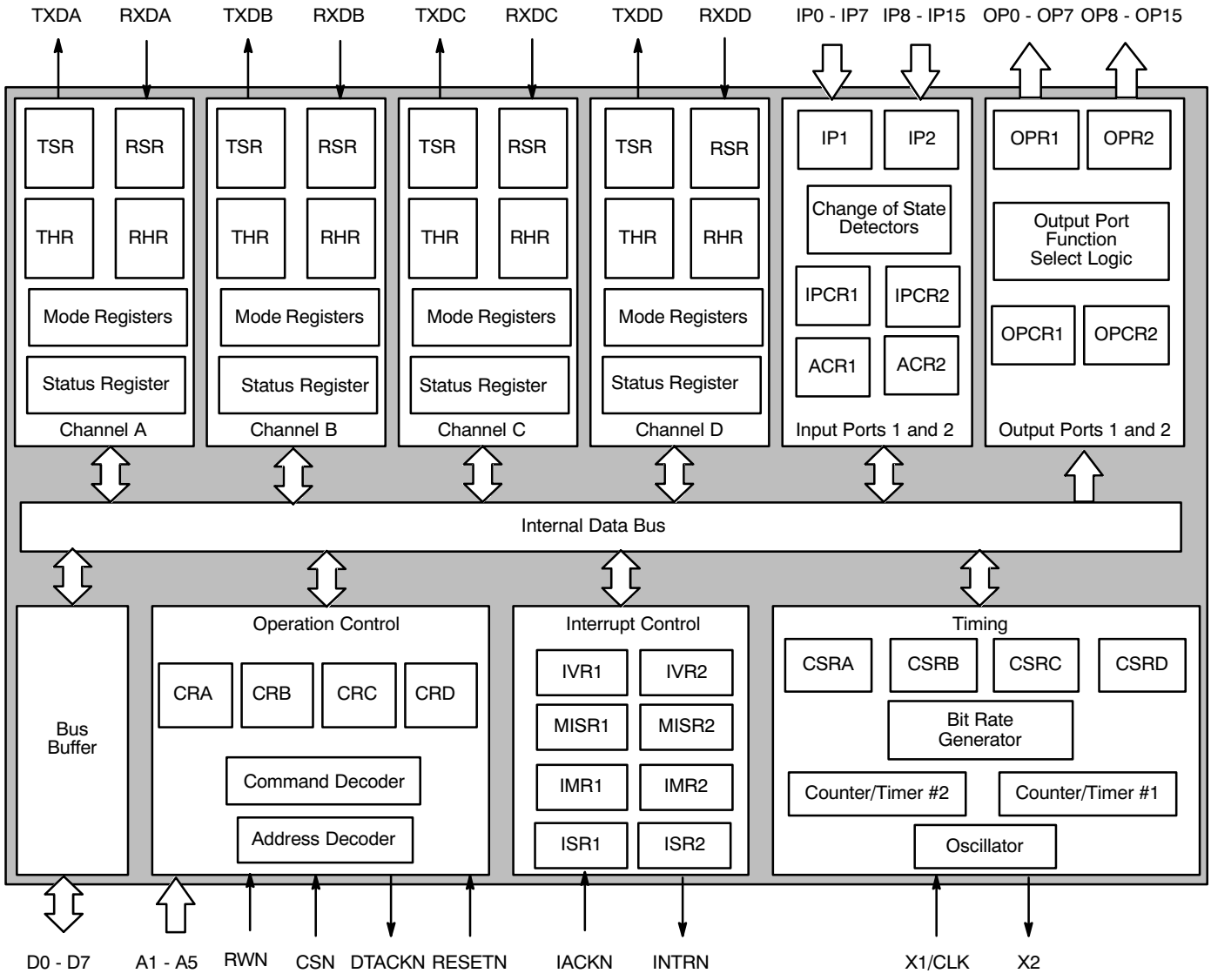


Figure 1. Block Diagram of the XR82C684 in the 68 Mode

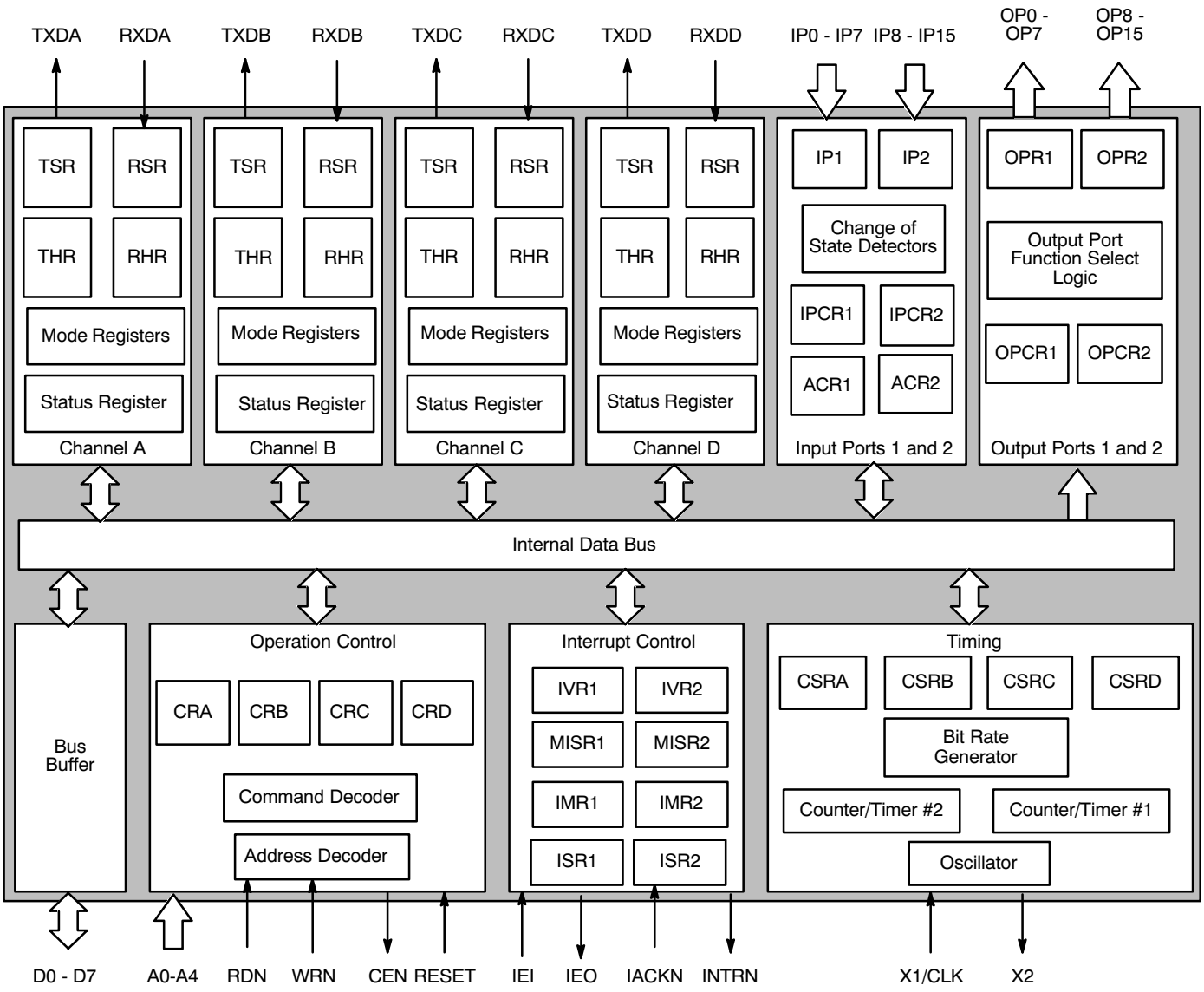
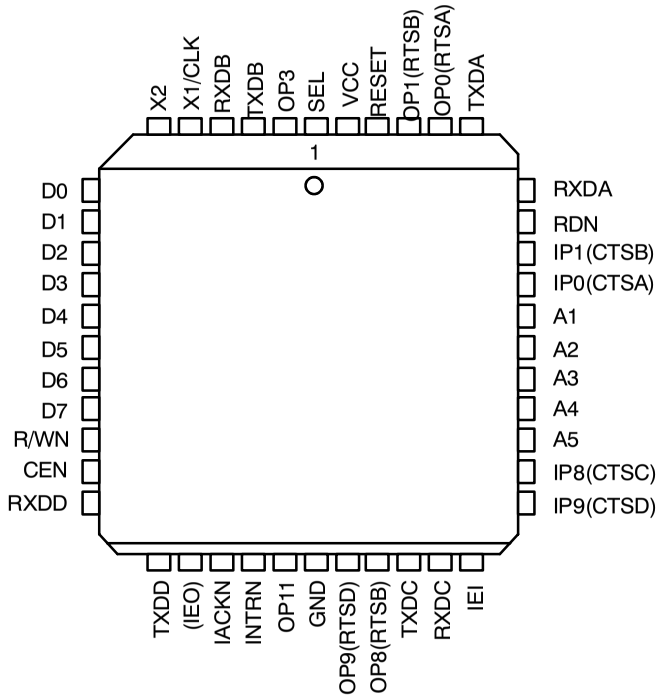
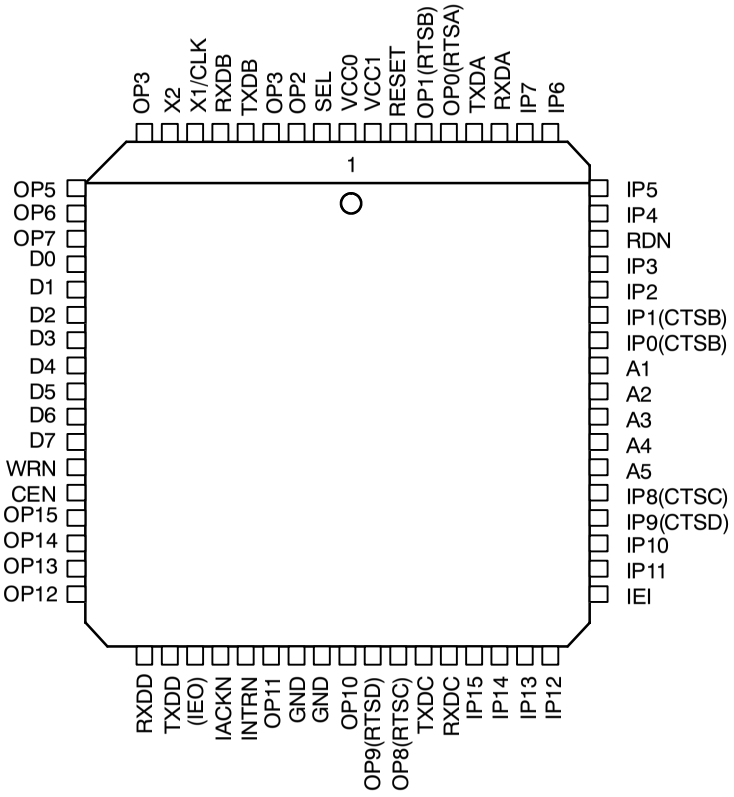


Figure 2. Block Diagram of the XR82C684 in the 88 Mode



44 Pin PLCC



68 Pin PLCC

PIN DESCRIPTION

Pin # 68 Pin PLCC	Pin # 44 Pin PLCC	Symbol	Type	Description
1		$V_{CC}0$		**Power Supply Pin.**
2	1	SEL	I	**Mode Select.** "88 mode" can be selected by tying this pin to GND; connecting this pin to V_{CC} will select the "68 mode."
3		OP2 (TXCA_16X) (TXCA_1X) (RXCA_1X)	O	**Output Port 2 (General Purpose Output).** This pin can also be configured to function as the "Channel A Transmitter 16x or 1x clock" output, or the "Channel A Receiver 1X clock" output.
4	2	OP3 (TXCB_1X) (RXCB_1X) (C/T_1_RDY)	O	**Output 3 (Active low).** Can be programmed as a general purpose output, the "Channel B transmitter 1x clock" output, the "Channel B receiver 1x clock" output, or an open drain "Counter/Timer 1 ready" output.
5	3	TXDB	O	**Transmitter Serial Data Output (Channel B).** The least significant bit of the character is transmitted first. This output is held in the "high" (marking state) when the transmitter is idle, disabled, or when the channel is operating in the local LOOPBACK mode. If an external transmitter clock is specified, TXCB, the transmitted data is shifted out of the TSR (Transmitter Shift Register) on the falling the edge of this clock.
6	4	RXDB	I	**Receiver Serial Data Input (Channel B).** The least significant bit of the character is received first. If the external receiver clock, RXCB, is specified, then the serial input data is sampled on the rising edge of this clock.
7	5	X1/CLK	I or O	**Crystal Output or External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used. If the oscillator is not used, an external clock signal must be supplied at this input. In order for the XR82C684 device to function properly, the user must supply a signal with frequencies between 2.0 MHz and 8.0 MHz. This requirement can be met by either a crystal oscillator or by the external TTL-compatible clock signal.
8	6	X2	I	**Crystal Input.** Connection for one side of the crystal (opposite of X1/CLK). If the oscillator is used, a capacitor must also be connected from this pin to ground. This pin must be left open if an external clock is supplied at the X1/CLK pin.
9		OP4 (RXRDY/ -FFULL_A)	O	**Output 4 (General Purpose Output).** This output pin can also be configured to function as the active-low "Receiver-Ready/FIFO Full" indicator for Channel A (RXRDY/-FFULL_A).
10		OP5 (RXRDY/ -FFULL_B)	O	**Output 5 (General Purpose Output).** This output pin can be configured to function as the active-low "Receiver-Ready/FIFO Full" indicator for Channel B (RXRDY/-FFULL_B).

Pin # 68 Pin PLCC	Pin # 44 Pin PLCC	Symbol	Type	Description
11		OP6 (TXRDY_A)	O	**Output 6 (General Purpose Output).** This output pin can be configured to function as the active-low "Transmitter-Ready" indicator for Channel A (-TXRDY_A).
12		OP7 (TXRDY_B)	O	**Output 7 (General Purpose Output).** This output pin can be configured to function as the active-low "Transmitter-Ready" indicator for Channel B (-TXRDY_B).
13	7	D0	I/O	**LSB of the Eight Bit Bi-Directional Data Bus.** All transfers between the CPU and the QUART take place over this bus (consisting of pins D0 - D7). The bus is tri-stated when the -CS input is "high", except during an IACK cycle (in the Z-Mode).
14	8	D1	I/O	**Bi-Directional Data Bus.**
15	9	D2	I/O	**Bi-Directional Data Bus.**
16	10	D3	I/O	**Bi-Directional Data Bus.**
17	11	D4	I/O	**Bi-Directional Data Bus.**
18	12	D5	I/O	**Bi-Directional Data Bus.**
19	13	D6	I/O	**Bi-Directional Data Bus.**
20	14	D7	I/O	**MSB of the Eight Bit Bi-Directional Data Bus.** All transfers between the CPU and the QUART take place over this bus (consisting of pins D0 - D7). The bus is tri-stated when the -CS input is "high", except during an IACK cycle (in the Z-Mode).
21	15	R/-W (68 Mode)	I	**Read/-Write (Input).** If this input is high while -CS is low, then the CPU is performing a READ cycle with the QUART. If this input is low, while -CS is low, then the CPU is performing a WRITE cycle with the QUART.
21	15	WRN (88 Mode)	I	**Write Strobe (Active Low).** A "low" on this input while -CS is also "low" writes the contents of the Data Bus into the addressed register, within the QUART. The transfer occurs on the rising edge of -WR.
22	16	-CS	I	**Chip Select (Active Low).** The data bus is tri-stated when -CS is high. Data transfers between the CPU and the QUART via D0 - D7 are enabled when -CS is low.
23		OP15 (-TXRDY_D)	O	**Output 15 (General Purpose Output).** This output port pin can be configured to function as the open-drain, active-low "Transmitter Ready" indicator for Channel D (-TXRDY_D).
24		OP14 (-TXRDY_C)	O	**Output 14 (General Purpose Output).** This output port pin can be configured to function as the open-drain. active-low "Transmitter Ready" indicator for Channel C (-TXRDY_C).
25		OP13 (RXRDY/ -FFULL_D)	I/O	**Output 13 (General Purpose Output).** This output port pin can be configured to function as the open-drain, active low "Receiver Ready" or "FIFO Full" indicator for Channel D (RXRDY/-FFULL_D).
26		OP12 (RXRDY/ -FFULL_C)	O	**Output 12 (General Purpose Output).** This output port pin can be configured to function as the open-drain, active-low "Receiver Ready" or "FIFO Full" indicator for Channel C (RXRDY/-FFULL_C).

Pin # 68 Pin PLCC	Pin # 44 Pin PLCC	Symbol	Type	Description
27	17	RXDD	I	**Receiver Serial Data Input (Channel D).** The least significant bit of the character is received first. If the external receiver clock, RXCD, is specified, then the serial input data is sampled on the rising edge of this clock.
28	18	TXDD	O	**Transmitter Serial Data Output (Channel D).** The least significant bit of the character is transmitted first. This output is held in the high (marking state) when the transmitter is idle, disabled, or when the channel is operating in the local LOOPBACK mode. If an external transmitter clock is specified, TXCD, the transmitted data is shifted out of the TSR (Transmitter Shift Register) on the falling the edge of this clock.
29	19	DTACKN (68 mode)	O	**Data Transfer Acknowledge (Three-State, Active-Low).** The QUART asserts -DTACK in order to inform the CPU that the present READ or WRITE operation is nearly complete. The 68000 Family of CPUs requires this signal from its peripheral devices in order to quickly and properly complete a READ or WRITE cycle. If the QUART asserts -DTACK during a READ operation, it indicates (to the CPU) that the requested data is on the databus. If -DTACK is asserted during an Interrupt Acknowledge cycle, the QUART is informing the CPU that the contents of the IVR (Interrupt Vector Register) are available on the data bus. If the QUART asserts the -DTACK during a WRITE cycle, it is informing the CPU that the data, on the data bus, has been latched into the data bus buffer of the QUART device.
29	19	IEO (88 mode)	O	**Interrupt Enable Output (Z Mode; Active High).** This output pin is normally “high”. However, either one of the following two conditions can cause this output pin to be negated (toggle “low”.) 1. If the IEI (Interrupt Enable Input) pin is “low”. If IEO is “low” because of the IEI pin, IEO will toggle “high” once the IEI pin has toggled “high”. 2. The QUART has issued an Interrupt Request to the CPU (-INTR pin is toggled “low”). If IEO is “low” because the QUART has requested an Interrupt, then IEO will remain “low”, throughout the Interrupt Service Routine, until the CPU has invoked the “RESET IUS” Command.
30	20	IACKN (68 or Z-Mode)	I	**Interrupt Acknowledge (Active Low).** This input is the CPU’s response to the interrupt request issued by the QUART device. When the CPU asserts this input, it indicates that the QUART’s interrupt request is about to be serviced, and that the very next bus cycle will be an interrupt acknowledge (IACK) cycle. The QUART will respond to the CPU’s interrupt acknowledge signal by placing the contents of the Interrupt Vector Register (IVR) on the data bus (D0 - D7).

Pin # 68 Pin PLCC	Pin # 44 Pin PLCC	Symbol	Type	Description
31	21	-INTRN	O	**Interrupt Request Output (Active Low, Open-Drain).** -INTR is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions. This signal will remain asserted throughout the Interrupt Service Routine and will be negated once the condition(s) causing the Interrupt Request has been eliminated.
32	22	OP11 (TXCD_1X) (RXCD_1X) (-C/T_2_RDY)	O	**Output 11 (General Purpose Output).** This output port pin can also be configured to function as the "Channel D Transmitter 1X clock" output (TXCD_1X), the "Channel D Receiver 1X clock" output, or the active-low "Counter/Timer #2 Ready" Output (-C/T_2_RDY)
33	23	GND		
34		GND		
35		OP10 (TXCC_1X) (TXCC_16X) (RXCC_1X)	O	**Output 10 (General Purpose Output).** This output port pin can be configured to function as the "Channel C Transmitter 1X or 16X clock" output; or as the "Channel C Receiver clock" output.
36	24	OP9 (-RTSD)	O	**Output 9 (General Purpose Output).** This output port pin can be configured to function as the active-low, open-drain "Channel D, Request-to-Send" output (-RTSD).
37	25	OP8 (-RTSC)	O	**Output 8 (General Purpose Output).** This output port pin can be configured to function as the active-low, open-drain "Channel C Request-to-Send" output (-RTSC).
38	26	TXDC	O	**Transmitter Serial Data Output (Channel D).** The least significant bit of the character is transmitted first. This output is held in the high (marking state) when the transmitter is idle, disabled, or when the channel is operating in the local LOOPBACK mode. If an external transmitter clock is specified, TXCD, the transmitted data is shifted out of the TSR (Transmitter Shift Register) on the falling the edge of this clock.
39	27	RXDC	I	**Receive Serial Data Input (Channel D).** The least significant bit is received first. If external receiver clock is specified, the data is sampled on the rising edge of the clock.
40		IP15	I	**Input 15 (General Purpose Input).**
41		IP14 (RXCD_EX)	I	**Input 14 (General Purpose Input).** This input pin can also be configured to function as the external clock input for the Receiver of Channel D (RXCD_EX).
42		IP13 (TXCD_EX)	I	**Input 13 (General Purpose Input).** This input pin can also be configured to function as the external clock input for the Transmitter of Channel D (TXCD_EX).
43		IP12 (RXCC_EX)	I	**Input 12 (General Purpose Input).** This input pin can also be configured to function as the external clock input for the Receiver of Channel C (RXCC_EX).

Pin # 68 Pin PLCC	Pin # 44 Pin PLCC	Symbol	Type	Description
44	28	IEI (Z-Mode)	I	**Interrupt Enable Input (Z-Mode; Active High).** If this active-high input is at a logic "high", the QUART is capable of generating all non-masked Interrupt Requests to the CPU. If this input is at a logic "low", the QUART is inhibited from generating any Interrupt Requests to the CPU. ***Note:*** *if the user is operating this device in the "68 Mode" or in the "88 I-Mode," then this pin should be tied to V_{CC}.*
45		IP11 (TXCC_EX)	I	**Input 11 (General Purpose Input).** This input pin can also be configured to function as the external clock input for the Transmitter of Channel C (TXCC_EX).
46		IP10 (CT2_EX)	I	**Input 10 (General Purpose Input).** This input pin can be configured to function as the external clock input for Counter/Timer # 2.
47	29	IP9 (-CTSD)	I	**Input 9 (General Purpose Input).** This input pin can be configured to function as the active-low, "Channel D Clear-to-Send" input (-CTSD).
48	30	IP8 (-CTSC)	I	**Input 8 (General Purpose Input).** This input pin can be configured to function as the active-low, "Channel C Clear-to-Send" input (-CTSC).
49	31	A5	I	**MSB of Address Input.**This input, along with address inputs, A1 - A5 are used to select certain registers within the QUART device during read and write operations with the CPU.
50	32	A4	I	**Address Input.**
51	33	A3	I	**Address Input.**
52	34	A2	I	**Address Input.**
53	35	A1	I	**LSB of Address Input.**
54	36	IP0 (-CTSA)	I	**Input 0 (General Purpose Input).** This input can be configured to function as the active-low "Clear-to-Send" input for Channel A (-CTSA).
55	37	IP1 (-CTSB)	I	**Input 1 (General Purpose Input).** This input can be configured to function as the active-low "Clear-to-Send" input for Channel B (-CTSB).
56		IP2 (CT1_EX)	I	**Input 2 (General Purpose Input).** This input can be configured to function as the external clock input for Counter/Timer # 1.
57		IP3 (TXCA_EX)	I	**Input 3 (General Purpose Input).** This input can be configured to function as the external clock input for the Channel A Transmitter.
58	38	-RD (88 Mode)		**Read Strobe ("88 Mode"; Active Low).** A "low" on this input while -CS is also "low" places the contents of the addressed QUART register, on the Data Bus. ***Note:*** If the user is operating this device in the "68-Mode" then this input should be tied to V_{CC}.
59		IP4 (RXCA_EX)	I	**Input 4 (General Purpose Input).** This input can be configured to function as the external clock input for the Channel A Receiver.

Pin # 68 Pin PLCC	Pin # 44 Pin PLCC	Symbol	Type	Description
60		IP5 (TXCB_EX)	I	**Input 5 (General Purpose Input).** This input can be configured to function as the external clock input for the Channel B Transmitter.
61		IP6 (RXCB_EX)	I	**Input 6 (General Purpose Input).** This input can be configured to function as the external clock input for the Channel B Receiver.
62		IP7	I	**Input 7 (General Purpose Input).**
63	39	RXDA	I	**Reveive Serial Data Input (Channel A).** The least significant bit of the character is received first. If external receiver clock, RXCA, is specified, the data is sampled on the rising edge of this clock.
64	40	TXDA	O	**Transmitter Serial Data Output (Channel A).** The least significant bit of the character is transmitted first. This output is held in the high (marking state) when the transmitter is idle, disabled, or when the channel is operating in the local LOOPBACK mode. If an external transmitter clock is specified, TXCA, the transmitted data is shifted out of the TSR (Transmitter Shift Register) on the falling the edge of this clock.
65	41	OP0 (-RTSA)	O	**Output 0 (General Purpose Output).** This output port pin can also be configured to function as the active-low, open-drain Request-to-Send output for Channel A (-RTSA).
66	42	OP1 (-RTSB)	O	**Output 1 (General Purpose Output).** This output port pin can also be configured to function as the active-low, open-drain Request-to-Send output for Channel B (-RTSB).
67	43	RESET	I	**Master Reset (Active High for the "88 Mode", and Active Low for the "68 Mode").** Asserting this input clears the following internal registers: SRn, ISRn, IMRn, OPRn, OPCRn, and initializes the IVRn to 0Fh, stops both of the Counter/Timers, puts 0P0 - OP15 in the high state, and places all four serial channels in the inactive state with the TXDA, TXDB, TXDC, and TXDD output marking (high).
68	44	$V_{CC}1$		

DC ELECTRICAL CHARACTERISTICS [1, 2]

Test Conditions: T_A = 25°C, V_{CC} = 5V ± 5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IHX1}	Input High Voltage (X1/CLK)	4.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	IOL = 2.4mA
V_{OH}	Output High Voltage	2.4			V	IOH = -400• A
I_{IL}	Input Leakage Current	-25		25	• A	VIN = 0 to V_{CC}
I_{ILSEL}	Select Pin Leakage Current	-30		30	• A	VIN = 0 to V_{CC}
I_{X1L}	X1 Input Low Current		-20		• A	VIN = 0
I_{X2L}	X2 Input Low Current		-7		mA	
I_{XIH}	X1 Input High Current		20		• A	VIN = V_{CC}
I_{X2H}	X2 Input High Current		20		• A	VIN = V_{CC}
I_{LL}	Data Bus Tri-State Leakage Current	-10		10	• A	VO = 0 to V_{CC}
I_{OC}	Open Drain Output Leakage Current	-10		10	• A	VO = 0 to V_{CC}
I_{CCA}	Power Supply Current[3]		6	15	mA	Active Mode
I_{CCS}	Power Supply Current[3]		3	10	mA	Standby Mode

Notes

[1] Parameters are valid over the specified temperature and operating supply ranges. Typical values are 25°C, V_{CC} = 5V and typical processing parameters.

[2] All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See NO TAG.

[3] Measured operating with a 3.6864 MHz crystal and with all outputs open.

[4] The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's Receiver is operating in external 1X clock mode.

AC ELECTRICAL CHARACTERISTICS [1, 2, 3]

Test Conditions: T_A = 25°C, V_{CC} = 5V ± 5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Reset Timing (See *Figure 56*)						
tRES	RESET Pulse Width	1.0			• s	
XR82C684 Read and Write Cycle Timing - 88 Mode (*Figure 57*) [7]						
t_{AS}	A0-A4 Setup Time to RD, WR Low	10			ns	
t_{AH}	A0-A4 Hold Time from RD, WR Low	0			ns	
t_{CS}	-CS Setup Time to RD, WR Low	0			ns	
t_{CH}	-CS Hold Time from -RD, -WR High	0			ns	
t_{RW}	-RD, -WR Pulse Width	225			ns	
t_{DD}	Data Valid from -RD Low		60	175	ns	
t_{DF}	Data Bus Floating from -RD High	10		100	ns	
t_{DS}	Data Setup Time to -WR High	100			ns	
t_{DH}	Data Hold Time from -WR High	5			ns	
t_{RWD}	High Time between Reads and/ or Writes [8, 9]		100		ns	
Z-Mode Interrupt Cycle Timing (*Figure 58*)						
t_{DIO}	IEO Delay Time from IEI			100	ns	
t_{IAS}	IACK Setup Time to RD Low[10]		Note 10		ns	
t_{IAH}	IACK Hold Time from RD High		0		ns	
t_{EIS}	IEI Setup Time to RD Low		50		ns	
t_{EOD}	IEO Delay Time from INTR Low			100	ns	
XR82C684 Read, Write and Interrupt Cycle Timing -68 Mode (*Figure 59*, *Figure 60* and *Figure 61*)						
t_{AS}	A1-A5 Setup Time to -CS Low	10			ns	
t_{AH}	A1-A5 Hold Time from -CS High	0			ns	
t_{RWS}	R/-W Setup Time to -CS Low	0			ns	
t_{RWH}	R/-W Setup Time from -CS High	0			ns	
t_{CSW}	-CS High Pulse Width [9, 11]	90			ns	
t_{CSD}	-CS or -IACK High from -DTACK Low	20			ns	
t_{DD}	Data Valid from -CS or -IACK Low			175	ns	
t_{DF}	Data Bus Floating from -CS or -IACK High	10		100	ns	
t_{DS}	Data Setup Time to -CS Low	0			ns	
t_{DH}	Data Hold Time from -CS Low	125			ns	
t_{DAL}	-DTACK Low from Read Data Valid	0			ns	

AC ELECTRICAL CHARACTERISTICS [1, 2, 3] (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
XR82C684 Read, Write and Interrupt Cycle Timing -68 Mode (*Figure 59*, *Figure 60* and *Figure 61*) (Cont'd)						
t_{DAH}	-DTACK High from -CS or -IACK High			100	ns	
t_{DAT}	-DTACK High Impedance from -CS or -IACK High			125	ns	
Port Timing - XR82C684 (Figure 62) [7]						
t_{PS}	Port Input Setup Time to -RD/ -CS Low	0			ns	
t_{PH}	Port Input Hold Time from -RD/ -CS High	0			ns	
t_{PD}	Port Output Valid from -WR/-CS High			400	ns	
Interrupt Output Timing - XR82C684 (*Figure 63*)						
t_{IR}	-INTR or OP3 - OP7 when used as Interrupts High from:			300	ns	
	Clear of Interrupts Status Bits in ISR or IPCR			300	ns	
	Clear of Interrupt Mask in IMR					
Clock Timing (*Figure 64*)						
t_{CLK}	X1/CLK (External) High or Low Time	100			ns	
t_{CLK}	X1/CLK Crystal or External Frequency	2.0	3.684	7.372	MHz	
t_{CTC}	Counter/Timer External Clock High or Low Time (IP2)	100			ns	
t_{CTC}	Counter/Timer External Clock Frequency	0		7.372	MHz	
t_{RTX}	RXCn and TXCn (External) High or Low Time[9]	220			ns	
f_{RTX}	RXCn and TXCn (External) Frequency					
	16X	0		16.0	MHz	
	1X	0		1.0	MHz	
Transmitter Timing (*Figure 65*)						
t_{TXD}	TXD Output Delay - TXC (External) Low			350	ns	
t_{TCS}	TXD Output Delay - TXC (Internal)			150	ns	

AC ELECTRICAL CHARACTERISTICS [1, 2, 3] (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Receiver Timing XR82C684 (*Figure 66*)						
t_{RXS}	RXD Data Setup Time to RXC (External) High	240			ns	
t_{RXH}	RXD Data Hold Time from RXC (External) High	200			ns	

Notes

[1] Parameters are valid over the specified temperature and operating supply ranges. Typical values are 25°C, V_{CC} = 5V and typical processing parameters.

[2] All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and 2.4V with a transition time of 20 ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 50.

[3] AC test conditions for outputs: CL = 50 pF, RL = 2.7 kohm to V_{CC}.

[4] If -CS is used as the strobing input, this parameter defines the minimum high time between -CSs.

[5] Consecutive write operations to the same register require at least three edges of the X1 clock between writes.

[6] This specification imposes a 6 MHz maximum 68000 clock frequency if a read or write cycle follows immediately after the previous read or write cycle. A higher 68000 clock can be used if this is not the case.

[7] This specification imposes a lower bound on -CS and -IACK low, guaranteeing that they will be low for at least one CLK period.

[8] This parameter is specified only to insure that -DTACK is asserted with respect to the rising edge of X1/CLK as shown in the timing diagram, not to guarantee operation of the part. If the specified setup time is violated, -DTACK may be asserted as shown or may be asserted one clock cycle later.

[9] The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's Receiver is operating in external 1X clock mode.

ABSOLUTE MAXIMUM RATINGS[1]

DC Supply Voltage 7V

Storage Temperature . . . . . -65°C to 150°C

All Voltages with respect to Ground [2] . . . -0.5V to +7V

Notes

[1] Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the "Electrical Characteristics" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYSTEM DESCRIPTION

The XR82C684 consists of four independent, full-duplex communication channels; each consisting of their own Transmitter and Receiver. Each channel of the QUART may be independently programmed for operating mode and data format. The QUART can interface to a wide range of processors with a minimal amount of components. The operating speed of each receiver and transmitter may be selected from one of 33 internally generated fixed bit rates, from a clock derived from an internal counter/timer, or from an externally supplied 1x or 16x clock. The bit rate generator (the source of the 33 different fixed bit rates) can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the QUART attractive for split speed channel applications such as clustered terminal systems.

Receiver and transmitter data are both quadrupled buffered via on-chip FIFOs in order to minimize the risk of receiver overrun and to reduce overhead in interrupt driven applications. The QUART also provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving QUART is full, thus preventing loss of data.

The QUART also provides two general-purpose 16-bit counter/timer (which may also be used as programmable bit rate generators), a 16 bit multi-purpose input port pins and an 16 bit multi-purpose output port pins.

A. DATA BUS BUFFER

The data bus buffer provides the interface between the internal (within the chip) and external data buses. It is controlled by the operation control block to allow data transfers to take place between the host CPU and the QUART.

B. OPERATION CONTROL BLOCK

The control logic of the Operation Control block receives operating commands from the CPU and generates the proper signals to the various sections of the QUART. The Operation Control Block functions as the user interface to the rest of the device. Specifically, it is responsible for QUART Register Address Decoding, and Command Decoding. Therefore all commands to set baud rates,

parity, other communication protocol parameters, start or stop the Counter/Timer or reading a “status register” to monitor data communication performance must go through the Operation Control Block.

The Operation Control Block will control QUART performance based upon the following input signals, depending upon whether it is operation in the “68” or “88 Mode”:

68 Mode	88 Mode
Address Inputs, A1 - A5	Address Inputs, A0 - A4
-RW	-RD
-CS	-WR
-RESET	-CS
	RESET

The “68 Mode” QUART also includes a data transfer acknowledge (-DTACK) output which is asserted during read and write cycles in order to inform the CPU that the requested operation has been completed. An asserted -DTACK signal indicates that the input data has been latched during a write cycle, that the requested data is on the data bus during a read cycle, or that the interrupt vector is on the data bus during an interrupt acknowledge cycle.

When interfacing the QUART to a 6800 family processor, the QUART should be configured to operate in the “88 Mode”. Additionally, the QUART will require some glue logic in order to properly interface to a 6800 Family processor. *Figure 3* presents a schematic of the appropriate glue logic circuitry.

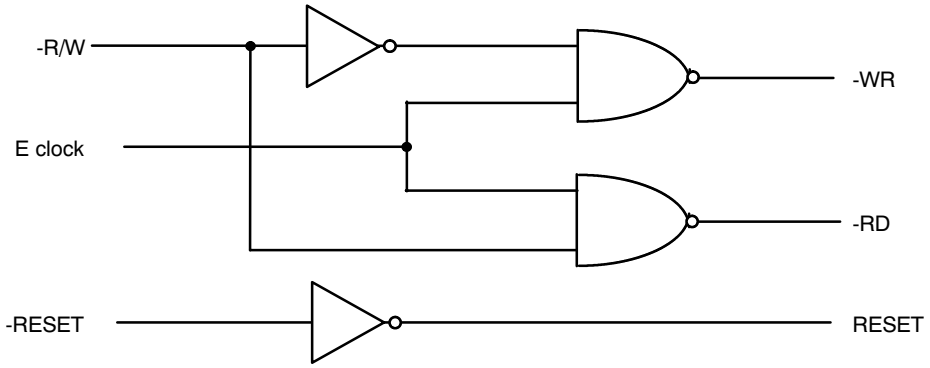


Figure 3. External Logic Circuitry Required To Interface a 6800 Family Processor to an "88-Mode" XR82C684 Device

B.1 Quart Register Addressing

The addressing of the internal registers of the QUART is presented in *Table 1*. *Please note that some of the registers are "Read Only" and others are "Write Only". Each channel is provided with the following dedicated (addressable) registers.*

- Command Registers
- Mode Registers (MR1 and MR2)
- Status Registers
- Clock Select Registers
- Receiver Holding Register (RHR) and Transmit Holding Register (THR)

Additionally, the QUART contains the following registers that support/control channel pairs.

- Interrupt Status Register 1 (Channels A & B)
- Interrupt Status Register 2 (Channels C & D)
- Interrupt Mask Register 1 (Channels A & B)
- Interrupt Mask Register 2 (Channels C & D)
- Masked Interrupt Status Register 1 (Channels A & B)
- Masked Interrupt Status Register 2 (Channels C & D)
- Interrupt Vector Register 1 (Channels A & B)
- Interrupt Vector Register 2 (Channels C & D)
- Auxiliary Control Register 1 (Channels A & B)
- Auxiliary Control Register 2 (Channels C & D)

And finally, the QUART also contains other registers that support functions other than serial data communication, such as the parallel ports and the Counters/Timers.

- OPCR1 - Output Port Control Register 1
- OPCR2 - Output Port Control Register 2
- IPCR1 - Input Port Configuration Register 1
- IPCR2 - Input Port Configuration Register 2
- CTUR1 - Counter/Timer Upper Byte Register 1
- CTUR2 - Counter/Timer Upper Byte Register 2
- CTLR1 - Counter/Timer Lower Byte Register 1
- CTLR2 - Counter/Timer Lower Byte Register 2

	Read Mode Registers		Write Mode Registers	
Address (Hex)	Register Name	Symbol	Register Name	Symbol
00	Mode Register, Channel A	MR1A, MR2A	Mode Register, Channel A	MR1A, MR2A
01	Status Register, Channel A	SRA	Clock Select Register, Channel A	CSRA
02	Masked Interrupt Status Register 1	MISR1	Command Register A	CRA
03	Rx Holding Register, Channel A	RHRA	Tx Holding Register, Channel A	THRA
04	Input Port Change Register 1	IPCR1	Auxiliary Control Register 1	ACR1
05	Interrupt Status Register 1	ISR1	Interrupt Mask Register 1	IMR1
06	Counter/Timer Upper Byte Register 1	CTU1	Counter/Timer Upper Byte Register 1	CTU1
07	Counter/Timer Lower Byte Register 1	CTL1	Counter/Timer Lower Byte Register	CTL1
08	Mode Register, Channel B	MR1B, MR2B	Mode Register, Channel B	MR1B, MR2B
09	Status Register, Channel B	SRB	Clock Select Register, Channel B	CSRB
0A	RESERVED	-	Command Register, Channel B	CRB
0B	Rx Holding Register, Channel B	RHRB	Tx Holding Register, Channel B	THRB
0C	Interrupt Vector Register	IVR1	Interrupt Vector Register 1	IVR1
0D	Input Port	IP1	Output Port Configuration Register (OP0 - OP7)	OPCR1
0E	Start Counter/Timer 1 Command	SCC1	Set Output Port Bits 1 Command	SOPBC1
0F	Stop Counter/Timer 1 Command	STC1	Clear Output Port Bits 1 Command	COPBC1
10	Mode Register C	MR1C, MR2C	Mode Register C	MR1C, MR2C
11	Status Register C	SRC	Clock Select Register C	CSRC
12	Masked Interrupt Status Register 2	MISR2	Command Register C	CRC
13	Rx Holding Register C	RHRC	Tx Holding Register C	THRC
14	Input Port Change Register 2	IPCR2	Auxiliary Control Register 2	ACR2
15	Interrupt Status Register 2	ISR2	Interrupt Mask Register 2	IMR2
16	Counter/Timer 2, Upper Byte Register	CTU2	Counter/Timer 2, Upper Byte Register	CTU2
17	Counter/Timer 2, Lower Byte Register	CTL2	Counter/Timer 2, Lower Byte Register	CTL2
18	Mode Register D	MR1D, MR2D	Mode Register D	MR1D, MR2D
19	Status Register D	SRD	Status Register D	SRD
1A	RESERVED	-	Command Register D	CRD
1B	Rx Holding Register D	RHRD	Tx Holding Register D	THRD
1C	Interrupt Vector Register 2	IVR2	Interrupt Vector Register 2	IVR2
1D	Input Port 2	IP2	Output Port Configuration Register 2 (OP8 - OP15)	OPCR2
1E	Start Counter/Timer 2 Command	SCC2	Set Output Port Bits 2 Command	SOPBC2
1F	Stop Counter/Timer 2 Command	STC2	Clear Output Port Bits 2 Command	COPBC2

Note: *The shaded blocks are not Read/Write registers but are rather "Address-Triggered" Commands.*

Table 1. Quart Port And Register Addressing

Table 1 indicates that each channel is equipped with two Mode Registers. Associated with each of these Mode Register pairs is a "Mode Register" pointer or MR pointer. Upon chip/system power up or RESET each MR pointer is "pointing to" the channel MR1n register. (*Please note that the suffix "n" is used at the end of many of the QUART registers symbols in order to refer, generically, to any one of the four channels*). However, the contents of the MR pointer will shift from the address of the MR1n register to that of the MR2n register, immediately following any Read or Write access to the MR1n register. The MR pointer will continue to "point to" the MR2n register until a hardware reset occurs or until a "RESET MR POINTER" command has been invoked. The "RESET MR POINTER" command can be issued by writing the appropriate data to the appropriate channel's Command Register. Therefore, both Mode Registers, within a given channel, have the same logical address. The features and functions of the QUART that are controlled by the Mode Registers are discussed in detail in *Section G.3*.

B.2 Command Decoding

Each channel is equipped with a Command Register. In general, the role of these Command Registers are to enable/disable the Transmitter, enable/disable the Receiver, along with facilitating a series of other miscellaneous channel and chip related commands. The bit format for each Command Register is presented below.

CRA, CRB, CRC, CRD

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Miscellaneous Commands				**Enable/Disable Receiver**		**Enable/Disable Transmitter**	
See Following Text				00 = No Change 01 = Enable Rx 10 = Disable Rx 11 = Not valid (do not use)		00 = No Change 01 = Enable Tx 10 = Disable Tx 11 = Not Valid (Do not use)	

The function of the lower nibble of the Command Registers is fairly straight-forward. This nibble is used to either enable or disable the Transmitter and/or Receiver.

The upper nibble of the Command Register is used to invoke a series of miscellaneous commands. *Table 2* defines the commands associated with the upper nibble of the Command Registers. *Please note that the upper nibble commands 116 through B effects only the performance of Command Register's Channel. However, commands C and D effects system (or chip) level operation.*

Bit 7	Bit 6	Bit 5	Bit 4	Description
0	0	0	0	**Null Command:**
0	0	0	1	**Reset MRn Pointer:** Causes the Channel's MRn pointer to point to MR1n.
0	0	1	0	**Reset Receiver:** Reset the individual channel receiver as if a Hardware Reset has been applied. The Receiver is disabled and the FIFO is flushed.
0	0	1	1	**Reset Transmitter:** Resets the individual channel transmitter as if a Hardware Reset had been applied. The TXDn output is forced to a high level.
0	1	0	0	**Reset Error Status:** Clears the Received Break (RB), Parity Error (PE), Framing Error (FE) and Overrun Error (OE) status bits, SR[7:3]. Specifically, if the Error Mode, for a particular channel is set at "Block" Error Mode, this command will reset all of the Receiver Error Indicators in the Status Register. In the Block Error Mode, once either a PE, FE, OE, or RB occurs, the error will continue to be flagged in the Status Register, until this command is issued. If the Error Mode, for a particular channel is set to "Character Error Mode", then the contents of the Status Register for PE, FE, and RB are reflected on a character by character basis. In the "Character Error Mode", the state of these indicators is based only upon the character that is at the top of the RHR. Note: The OE indicator is always presented as a "Block Error Mode" indicator, and requires this command to be reset.
0	1	0	1	**Reset Break Change Interrupt:** Clears the channel's break change interrupt status bit, within the appropriate Interrupt Status Register.

Bit 7	Bit 6	Bit 5	Bit 4	Description
0	1	1	0	**Start Break:** Forces the TXDn output low. The transmitter must be enabled to start a break. If the transmitter is empty, the start of the break may be delayed up to two bit times. If the transmitter is active, the break begins when the transmission of those characters in the THR is completed, viz., TXEMP must be true before the break will begin.
0	1	1	1	**Stop Break:** The TXDn line will go high within two bit times. TXDn will remain high for one bit time before the next character, if any, is transmitted.
1	0	0	0	**Set Rx BRG Select Extend Bit:** Sets the channel's "Receiver BRG Select Extend Bit" to 1.
1	0	0	1	**Clear Rx BRG Select Extend Bit:** Clears the channel's "Receiver BRG Select Extend Bit" to 0.
1	0	1	0	**Set Tx BRG Select Extend Bit:** Sets the channel's "Transmitter BRG Select Extend Bit" to 1.
1	0	1	1	**Clear Tx BRG Select Extend Bit:** Clears the channel's "Transmitter BRG Select Extend Bit" to 0.
1	1	0	0	**Set Standby Mode (Channel A):** When this command is invoked via the Channel A Command Register, power is removed from each of the transmitters, receivers, counter/timer and additional circuits to place the QUART in the standby (or lower power) mode. *Please note that this command effects the operation of the entire chip. Normal operation is restored by a hardware reset or by invoking the "SET ACTIVE MODE" command.* **Reset IUS Latch (Channel B):** When this command is invoked via the Channel B Command Register, and the QUART is operating in Z-mode, it causes the Interrupt-Under-Service (IUS) latch to be reset. This, in turn, will cause the IEO output to toggle "high". **Select Direct System Clock (Channel C):** Following a hardware RESET, and prior to invoking this command, the QUART is operating in a "Divided System Clock" mode. Specifically, this means that the oscillator clock frequency is divided by two, prior to entering the baud rate generator portion of the Timing Control Block. If the QUART operates in the "Divided Systems Clock" mode, then the baud rate achieved (for all four channels) will be one-half of that presented in *Table 15* and *Table 15A*. If the user invokes this command via the Channel C Command Register, then this "Divide-by-2" network is removed from the "timing signal" path, and the user will achieve the baud rates, specified in *Table 15* and *Table 15A*.
1	1	0	1	**Set Active Mode (Channel A):** When this command is invoked via the Channel A Command Register, the QUART is removed from the Standby Mode and resumes normal operation. **Set Z-Mode (Channel B):** When this command is invoked via the Channel B Command Register, the QUART is conditioned to operate in the Z-Mode. For a detailed discussion of the QUART's operation while in the Z-Mode, Please see *Section C.6.2*. (Available for 88 Mode only) **Select Divided System Clock (Channel C):** This command is the reverse of the "Select Direct Systems Clock mode" command. This command will return a "divide by 2" network into the BRG timing signal path. The effect of this command is to reduce the baud rate by one-half of that presented in *Table 15* and *Table 15A*. *Please note that this command effects the baud rates for all four channels of the QUART.*
1	1	1	0	**Reserved**
1	1	1	1	**Reserved**

Table 2. Miscellaneous Commands, Upper Nibble of All Command Registers, Unless Otherwise Specified

In addition to the commands which are available through the command registers, the QUART also offers "Address-Triggered" "commands. These commands are listed in *Table 1*, "Quart Port and Register Addressing," and are further identified by being "shaded" in this table. Specifically, these commands are:

- Start Counter/Timer 1 Command
- Stop Counter/Timer 1 Command
- Start Counter/Timer 2 Command
- Stop Counter/Timer 2 Command
- Set Output Port Bits 1 Command
- Set Output Port Bits 2 Command
- Clear Output Port Bits 1 Command
- Clear Output Port Bits 2 Command

Each command is invoked by either reading or writing data to its corresponding QUART address, as specified in *Table 1*.

For example, the Start Counter/Timer 1 Command is invoked by the procedure of reading QUART address $0E_{16}$. *Please note that this "Read Operation" will not result in placing the contents of a QUART register on the data bus. The only thing that will happen, in response to this procedure is the Counter/Timer #1 will initiate counting. For a detailed discussion into the operation of the Counter/Timers, please see Section D.2.*

Another example of an Address-Triggered commands is the "Set Output Port Bits 1" Command. This command is invoked by performing a write of data to QUART address $0E_{16}$. When the user invokes this command, he/she is setting certain bits (to "1") within OPR1 (Output Port Register 1). All other bits, within OPR1 (not specified to be set), are not changed. The state of the output port pins, OP0 - OP7 are complements of the individual bits within OPR1. Likewise, the state of output port pins OP8 - OP15 are complements of the individual bits with OPR2. Hence, if OPR1[0] (e.g., bit 0 within OPR1) is set to "1", the state of the corresponding output port pin, OP0, is now set to a logic "0". Consequently, one can think of the "Set Output Port Bits" command as the "Clear Output Port Pins" command. For a more detailed discussion into the operation of the Output Ports, please see *Section F*.

C. Interrupt Control Block

The Interrupt Control Block allows the user to apply the QUART in an "Interrupt-Driven" environment. The QUART includes an active-low, open-drain interrupt request output signal (-INTR), which may be programmed to be asserted upon the occurrence of any of the following events:

- Transmit Hold Register A, B, C, or D Ready
- Receive Hold Register A, B, C, or D Ready
- Receive FIFO A, B, C or D Full
- Start or End of Received Break in Channels A, B, C or D
- End of Counter/Timer Count Reached (for either Counter/Timer 1 or Counter/Timer 2)
- Change of State on input pins, IP0, IP1, IP2, IP3, IP8, IP9, IP10, or IP11

The Interrupt Control Block consists of two Interrupt Status Registers (ISR1 and ISR2), two Interrupt Mask Registers (IMR1 and IMR2), two Masked Interrupt Status Registers (MISR1 and MISR2) and two Interrupt Vector Registers (IVR1 and IVR2). *Table 3* lists these registers and their address location (within the QUART).

Register	Description	Address Location (in QUART Address Space)
ISR1	Interrupt Status Register 1	05_{16} (Read Only)
ISR2	Interrupt Status Register 2	15_{16} (Read Only)
IMR1	Interrupt Mask Register 1	05_{16} (Write Only)
IMR2	Interrupt Mask Register 2	15_{16} (Write Only)
MISR1	Masked Interrupt Status Register 1	02_{16} (Read Only)
MISR2	Masked Interrupt Status Register 2	12_{16} (Read Only)
IVR1	Interrupt Vector Register 1	$0C_{16}$
IVR2	Interrupt Vector Register 2	$1C_{16}$

Table 3. Listing and Brief Description of Interrupt System Registers

The role and purpose of each of these registers are defined below:

C.1 Interrupt Status Registers (ISR1 and ISR2)

The contents of the ISRs indicates the status of all potential interrupt conditions. If any bits within these registers are toggled "high", then the corresponding condition has or is occurring. In general, the contents of the ISR will indicate to the processor, the source or the reason for the Interrupt Request from the QUART. Therefore, any interrupt service routine for the QUART should begin by reading either these registers or the MISRs (Masked Interrupt Status Registers). The bit-format of the two ISRs are presented below:

ISR1 Register Bit Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change	Delta Break B	RXRDY/ FFULLB	TXRDYB	Counter #1 Ready	Delta Break A	RXRDY/ FFULLA	TXRDYA
0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No
1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes

ISR2 Register Bit Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change	Delta Break D	RXRDY/ FFULL D	TXRDY D	Counter #2 Ready	Delta Break C	RXRDY/ FFULL C	TXRDY C
0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No
1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes

The definition of the meaning behind each of these bits is presented below.

C.1.1 ISR1 Register - Channels A and B

ISR1[7]: Input Port Change of State:

If this bit is at a logic "1", then a change of state was detected at Input Port pins IP0 - IP3. The user services this interrupt by reading IPCR1 (if ISR1[7] = 1). ISR1[7] is cleared when the CPU has read the Input Port Configuration Register # 1 (IPCR1). By reading IPCR1, the user will determine:

- The Input Port pin that changed state
- The final state of the monitored input ports, following the Change of State.

For a detailed description of the IPCR1, please see *Section E*.

Please note that in order to enable this Interrupt Condition, the user must do two things:

1. *Write the appropriate data to the lower nibble of the Auxiliary Control Register, ACR1[3:0]. In this step, the user is specifying which of the four Input Pins, IP0 - IP3, should trigger an "Input Port Change" Interrupt request.*
2. *Write a logic "1" to IMR1[7].*

ISR1[6] Delta Break Indicator - Channel B:

When this bit is set, it indicates that the Channel B receiver has detected the beginning or end of a received break (RB). This bit is cleared (or reset) when the CPU invokes a channel B "RESET BREAK CHANGE INTERRUPT" command (see *Table 2*). For more information into the QUART's response to a BREAK condition, please see *Section G.2*.

ISR1[5] RXRDY/FFULL B - Channel B Receiver Ready or FIFO Full

The function of this bit is selected by programming MR1B[6]. If this bit field is configured to function as the Receiver Ready indicator (RXRDYB), then a "1" in this bit-field indicates that at least one character of data is in RHRB and is ready to be read by the CPU. This bit is set when a character is transferred from the receiver shift register to the RHRB and is cleared when the CPU reads the RHRB. If there are still more characters in RHRB after the read operation, the bit will be set again after RHRB is "popped".

If this bit is configured to function as the "FIFO Full" Indicator (FFULLB), then it is set when a character is transferred from the RSR to RHRB and the transfer causes RHRB to become full. This bit is cleared when the CPU reads RHRB; and thereby "popping" the FIFO,

making room for the next character. If a character is waiting in the RSR because RHRB is full, this bit will be set again after the read operation, when that character is loaded into RHRB.

Note: *If this bit is configured to reflect the FFULLB indicator, this bit will not be set (nor will produce an interrupt request) if one or two characters are still remaining in RHRB, following data reception. Hence, it is possible that the last two characters in a string of data (being received) could be lost due to this phenomenon.*

ISR1[4] TXRDYB - Channel B Transmitter Ready

This bit is a duplicate of TXRDY B, SRB[2].

This bit, when set, indicates that THRB is empty and is ready to accept a character from the CPU. The bit is cleared when the CPU writes a new character to THRB; and is set again, when that character is transferred to the TSR. TXRDYB is set when the transmitter is initially enabled and is cleared when the transmitter is disabled. Characters loaded into THRB while the transmitter is disabled will not be transmitted.

ISR1[3] Counter #1 Ready

In the TIMER mode, C/T #1 (Counter/Timer #1) will set ISR1[3] once for each cycle of the resultant square wave (which is available at the OP3 pin). ISR1[3] will be cleared by invoking the address-triggered "STOP COUNTER 1" command. Bear in mind, that in the TIMER mode, the "STOP COUNTER" command will not stop the C/T.

In the COUNTER mode, this bit is set when counter #1 reaches the terminal count (0000) and is cleared when the counter is stopped by a "STOP COUNTER" command. When the Counter/Timer is in the COUNTER Mode, the "STOP COUNTER" command will stop the Counter/Timer. A detailed discussion on the operation of the Counter/Timers can be found in *Section D*.

ISR1[2]: Delta Break A - Channel A Change in Break

Assertion of this bit indicates that the channel A receiver has detected the beginning of or the end of a received break (RB). This bit is cleared when the CPU invokes a channel A "RESET BREAK CHANGE INTERRUPT" command. For more information into the QUART's response to a BREAK condition, please see *Section G.2*.

ISR1[1] RXRDYA/FFULL A - Channel A Receiver Ready or FIFO Full

The function of this bit is selected by programming MR1A[6]. If this bit field is configured to function as the "Receiver Ready" indicator (RXRDYA), a "1" in this bit field indicates that there is at least one character of data in RHRA, and is ready to be read by the CPU. This bit is set when a character is transferred from the RSR to RHRA and is cleared when the CPU reads (or "pops") RHRA. If there are still more characters in RHRA, following the read operation, the bit will be set again after RHRA is "popped".

If this bit is configured to function as the FIFO (RHR) full indicator (FFULLA), it is set when a character is transferred from the RSR to RHRA and the newly transferred character causes RHRA to become full. This bit is cleared when the CPU reads RHRA. If a character is waiting in the RSR because RHRA is full, this bit will be set again, following the read operation, when that character is loaded into RHRA.

Note: *If this bit is configured to reflect the FFULLA indicator, this bit will not be set (nor will produce an interrupt request) if one or two characters are still remaining in RHRA, following data reception. Hence, it is possible that the last two characters in a string of data (being received) could be lost due to this phenomenon. Therefore, the user is advised to read RHRA until empty.*

ISR1[0]: Channel A Transmitter Ready

This bit is a duplicate of TXRDY A, SRA[2].

This bit, when set, indicates that THRA is empty and is ready to accept a character from the CPU. The bit is cleared when the CPU writes a new character to THRA; and is set again, when that character is transferred to the TSR. TXRDYA is set when the transmitter is initially enabled and is cleared when the transmitter is disabled. Characters loaded into THRA while the transmitter is disabled will not be transmitted.

C.1.2 ISR2 Register - Channels C and D

ISR2[7]: Input Port Change of State:

If this bit is at a logic "1", then a change of state was detected at Input Port pins IP8 - IP11. The user services this interrupt by reading the IPCR2 (if ISR2[7] = 1). ISR2[7] is cleared when the CPU has read the Input Port Configuration Register (IPCR2). By reading the IPCR2, the user will determine:

- The individual Input Port pin that changed state

- The final state of the monitored input ports, following the Change of State.

For a detailed description of IPCR2, please see *Section E*.

Please note that in order to enable this Interrupt Condition, the user must do two things:

1. *Write the appropriate data to the lower nibble of the Auxiliary Control Register, ACR2[3:0]. In this step, the user is specifying which of the four Input Pins (IP8 - IP11) should trigger an "Input Port Change" Interrupt request.*
2. *Write a logic "1" to IMR2[7].*

ISR2[6] Delta Break Indicator - Channel D:

When this bit is set, it indicates that the Channel D receiver has detected the beginning or end of a received break (RB). This bit is cleared (or reset) when the CPU invokes a channel D "Reset Break Change Interrupt" command (see *Table 2*). For more information into the QUART's response to a break condition, please see *Section G.2*.

ISR2[5] RXRDY/FFULL D - Channel D Receiver Ready or FIFO Full

The function of this bit is selected by programming MR1D[6]. If this bit field is configured to function as the "Receiver Ready" indicator (RXRDYD), a "1" in this bit field indicates that at least one character of data is in RHRB and is ready to be read by the CPU. This bit is set when a character is transferred from the receiver shift register to RHRD and is cleared when the CPU reads the RHRD. If there are still more characters in RHRD after the read operation, the bit will be set again after RHRD is "popped".

If this bit is configured to function as the "FIFO Full" indicator (FFULLD), this bit-field is set when a character is transferred from the RSR to RHRD and the transfer causes RHRD to become full. This bit is cleared when the CPU reads RHRD; and thereby "popping" the FIFO, making room for the next character. If a character is waiting in the RSR because RHRD is full, this bit will be set again after the read operation, when that character is loaded into RHRD.

Note: *If this bit is configured to reflect the FFULLD indicator, this bit will not be set (nor will produce an interrupt request) if one or two characters are still remaining in RHRD, following data reception. Hence, it is possible that the last two characters in a string of data (being received) could be lost due to this phenomenon.*

ISR2[4] TXRDYD - Channel D Transmitter Ready

This bit is a duplicate of TXRDY D, SRD[2].

This bit, when set, indicates that THRD is empty and is ready to accept a character from the CPU. The bit is cleared when the CPU writes a new character to THRD; and is set again, when that character is transferred to the TSR. TXRDYD is set when the transmitter is initially enabled and is cleared when the transmitter is disabled. Characters loaded into THRD while the transmitter is disabled will not be transmitted.

ISR2[3] Counter # 2 Ready

In the TIMER mode, C/T#2 (Counter/Timer #2) will set ISR2[3] once for each cycle of the resultant square wave (which is available at the OP11 pin). ISR2[3] will be cleared by invoking the address-triggered "Stop Counter 2" command. Bear in mind, that in the TIMER mode, the "STOP COUNTER" command will not stop the C/T.

In the COUNTER mode, this bit is set when the counter reaches the terminal count (0000) and is cleared when the counter is stopped by a "STOP COUNTER" command. When the Counter/Timer is in the COUNTER Mode, the "STOP COUNTER" command will stop the Counter/Timer. A detailed discussion on the operation of the Counter/Timer can be found in *Section D*.

ISR2[2]: Delta Break C - Channel C Change in Break

Assertion of this bit indicates that the channel C receiver has detected the beginning of or the end of a received break (RB). This bit is cleared when the CPU invokes a channel C "Reset Break Change Interrupt" command. For more information into the QUART's response to a BREAK condition, please see *Section G.2*.

ISR2[1] RXRDYA/FFULL C - Channel C Receiver Ready or FIFO Full

The function of this bit is selected by programming MR1C[6]. If this bit-field is configured to function as the "Receiver Ready" indicator (RXRDYC), a "1" in this bit-field indicates that there is at least one character of data in RHRC, and is ready to be read by the CPU. This bit is set when a character is transferred from the RSR to RHRC and is cleared when the CPU reads (or "pops") RHRC. If there are still more characters in RHRC,

following the read operation, the bit will be set again after RHRC is "popped".

If this bit field is configured to function as the FIFO (RHR) full indicator (FFULLC), this bit-field is set when a character is transferred from the RSR to RHRC and the newly transferred character causes RHRC to become full. This bit is cleared when the CPU reads RHRC. If a character is waiting in the RSR because RHRC is full, this bit will be set again, following the read operation, when that character is loaded into RHRC.

Note: *If this bit is configured to reflect the FFULLC indicator, this bit will not be set (nor will produce an interrupt request) if one or two characters are still remaining in RHRC, following data reception. Hence, it is possible that the last two characters in a string of data (being received) could be lost due to this phenomenon. Therefore, the user is advised to read RHRC until empty.*

ISR2[0]: Channel C Transmitter Ready

This bit is a duplicate of TXRDY C, SRC[2].

This bit, when set, indicates that THRC is empty and is ready to accept a character from the CPU. The bit is cleared when the CPU writes a new character to THRC; and is set again, when that character is transferred to the TSR. TXRDYC is set when the transmitter is initially enabled and is cleared when the transmitter is disabled. Characters loaded into THRC while the transmitter is disabled will not be transmitted.

C.2 Interrupt Mask Registers (IMR1 and IMR2)

The Interrupt Mask Registers are each "Write Only" registers which enables the user to select the conditions that will cause the QUART to issue an Interrupt Request to the processor. Therefore, the bit-format of the IMR is essentially the same as the ISR. However, for completeness, the Bit Format of the IMR1 and IMR2 are presented below.

IMR1 Bit Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change	**Delta Break B**	**RXRDY/ FFULLB**	**TXRDYB**	**Counter Ready**	**Delta Break A**	**RXRDY/ FFULLA**	**TXRDYA**
0 = Off	0 = Off	0 = Off	0 = Off	0 = Off	0 = Off	0 = Off	0 = Off
1 = On	1 = On	1 = On	1 = On	1 = On	1 = On	1 = On	1 = On

IMR2 Bit Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change	**Delta Break D**	**RXRDY/ FFULLD**	**TXRDY D**	**Counter Ready**	**Delta Break C**	**RXRDY/ FFULLC**	**TXRDYC**
0 = Off	0 = Off	0 = Off	0 = Off	0 = Off	0 = Off	0 = Off	0 = Off
1 = On	1 = On	1 = On	1 = On	1 = On	1 = On	1 = On	1 = On

If the user wishes to enable a certain interrupt, he/she should write a "1" to the bit within the IMR, corresponding to that Interrupt Condition. Likewise, to disable or mask out a certain condition causing an interrupt, the user should write a "0" to the bit location corresponding to that condition.

Please note that the IMRs are Write Only Registers, and can therefore not be read by the processor.

C.3 Masked Interrupt Status Register (MISR1 and MISR2)

The content of the MISRn register is basically the results of ANDing the ISRn and IMRn together.

MISRn Content = [ISRn Contents]·[IMRn Contents]

One limitation of QUART Interrupt Service Routines that rely on reading the ISRs is that the bits within the ISRs can toggle "high" due to their corresponding conditions

whether or not they are enabled by the appropriate IMR. Therefore, the user, following reading the Interrupt Status Register, will have to make provisions for; and execute a "bit-by-bit" AND of the ISR and IMR contents. Since the IMRs are "Write Only" registers and cannot be read by the processor, the contents of the IMRs will have to be stored in system memory, for later recall. The additional hardware and software overhead required to support this activity can be eliminated via use of the MISRs.

C.4 Interrupt Vector Registers, IVR1 and IVR2

These registers are only used for Interrupt Vector generation when the QUART is operating in the "68 Mode" or has been commanded into the special Z-Mode (a subset of the "88-Mode"). While in one of these modes, the contents of the IVR is typically related to the starting address of the QUART's Interrupt Service Routine. Otherwise, in the I-Mode, Interrupt Vector generation is typically performed off-chip. When the QUART is operating in the I-Mode, the IVRs can be used as general purpose read/write registers. The role of the IVRs, while the QUART is operating in the 68 or Z-Mode is presented in section C.6.

C.5 Limitations of the QUART Interrupt Structure

The Interrupt Structure offered by the QUART allows the user to program the QUART to generate interrupts in response to certain THR and RHR (FIFO) conditions; the Counter/Timer Ready condition, and to changes in the Break Condition (at the Receiver). However, aside from the "Delta Break Condition" (RB), the QUART does not generate interrupts due to Receiver problems such as Parity Error (PE), Receiver Overrun Error (OE), or Framing Error (FE). The QUART also does not offer the user to ability to configure one of the output ports to relay the occurrence of any of these adverse conditions. Therefore, unless the user is implement some sort of "Data Link Layer" error checking scheme such as CRC, the user is advised to "validate" the received data by frequently reading the Status Register; and checking for any non-zero upper-nibble values. This is especially the case if the user has set the Error Mode to "Character" (MR1n[5] = 0).

C.6 Servicing QUART Interrupts

Interrupt servicing with the XR82C684 QUART falls into two broad categories: "68 Mode" and "88 Mode." Within the "88 Mode", interrupt servicing can be further divided into the I-Mode and the Z-Mode. Interrupt Servicing for each of these modes is discussed in detail below.

C.6.1 "68 Mode" Interrupt Servicing

The 68000 family of microprocessors supports vectored-interrupt processing. Specifically, during interrupt servicing, the QUART will respond to the interrupt acknowledge, from the CPU, by placing the contents of one of the IVRs (IVR1 or IVR2) on the data bus, to be read by the CPU. During normal operation, the contents of each of the IVRs are related to a locations in memory, where the appropriate interrupt service routines (for the interrupting QUART) resides.

Therefore, in vectored interrupt applications, the contents of the IVRs accomplish two things:

1. Identify the peripheral components requesting the interrupt.
2. Allow the CPU to determine the location of; and branch program control to the location, in program memory, that contains the appropriate Interrupt Service Routine for the interrupting QUART.

The advantage of using "Vectored-Interrupt" processing over "polled-interrupt" processing is significant in time-critical applications using many peripherals devices. In "polled-interrupt" processing, upon the detection of the Interrupt Request, the microprocessor will have to go through and poll each and every peripheral device in order to determine the device causing the interrupt. Only after this polling procedure is completed can the microprocessor branch program control to the appropriate interrupt service routine. The time required to poll each of these peripheral devices adds to the interrupt latency period over and above that which would occur during vectored-interrupt processing.

Consequently, during initialization of the QUART, the user will have to load each of the IVRs with a hexadecimal numbers of values between 40h through FFh, inclusively. This is the range of the values, in the 680x0's exception vector table, that have been reserved for "User Interrupt Vector". The memory location of the "QUART" interrupt service routines can be found by multiplying the contents of the IVR by 4. Hence, the user should take care to make sure that the Interrupt Service Routine for the interrupt conditions addressed by ISR1, starts at [Contents of IVR1]·4 in Program Memory. Likewise, the user must issue that the Interrupt Service Routine for the interrupt conditions addressed by ISR2, start at [Contents of IVR2]·4 in Program Memory.