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XR88C681

CMOS Dual Channel UART (DUART)

June 2006

FEATURES

- Two Full Duplex, Independent Channels
- Asynchronous Receiver and Transmitter
- Quadruple-Buffered Receivers and Dual Buffered Transmitters
- Programmable Stop Bits in 1/16 Bit Increments
- Internal Bit Rate Generators with More than 23 Bit Rates
- Independent Bit Rate Selection for Each Transmitter and Receiver
- External Clock Capability
- Maximum Bit Rate: 1X Clock - 1Mb/s, 16X Clock - 125kb/s
- Normal, AUTOECHO, Local LOOPBACK and Remote LOOPBACK Modes
- Multi-function 16 Bit Counter/Timer
- Interrupt Output with Eight Maskable Interrupt Conditions
- Interrupt Vector Output on Acknowledge (40 Pin DIP and 44 Pin PLCC Packages Only)
- Programmable Interrupt Daisy Chain
- 8 General Purpose Outputs (40 Pin DIP and 44 Pin PLCC Packages Only)
- 7 General Purpose Inputs with Change of States Detectors on Inputs (40 Pin DIP and 44 Pin PLCC Packages Only)
- Multi-Drop Mode Compatible with 8051 Nine Bit Mode
- On-Chip Oscillator for Crystal
- Standby Mode to Reduce Operating Power
- Compatible with the Motorola MC2681 and Signetics SCC2692 devices
- Advanced CMOS Low Power Technology

APPLICATIONS

- Multimedia Systems
- Serial to Parallel/Parallel to Serial Converter
- DTE for Modem Communication Systems

GENERAL DESCRIPTION

The EXAR Dual Universal Asynchronous Receiver and Transmitter (DUART) is a data communications device that provides two fully independent full duplex asynchronous communication channels in a single package. The DUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

The XR88C681 device offers a single IC solution for the 8080/85, 8086/88, Z80, Z8000, 68xx and 65xx microprocessor families.

The DUART is fabricated using advanced two layer metal, with a high performance density EPI/CMOS 1.8□process to provide high performance and low power consumption, and is packaged in a 40 pin PDIP, a 28 pin PDIP, and a 44 pin PLCC.

ORDERING INFORMATION

Part No.	Pin Package	Operating Temperature Range
XR88C681CJ	44 PLCC	0°C to 70°C
XR88C681CN/40	40 CDIP	0°C to 70°C
XR88C681CP/28	28 PDIP	0°C to 70°C
XR88C681CP/40	40 PDIP	0°C to 70°C
XR88C681J	44 PLCC	-40°C to +85°C
XR88C681N/40	40 CDIP	-40°C to +85°C
XR88C681P/28	28 PDIP	-40°C to +85°C
XR88C681P/40	40 PDIP	-40°C to +85°C

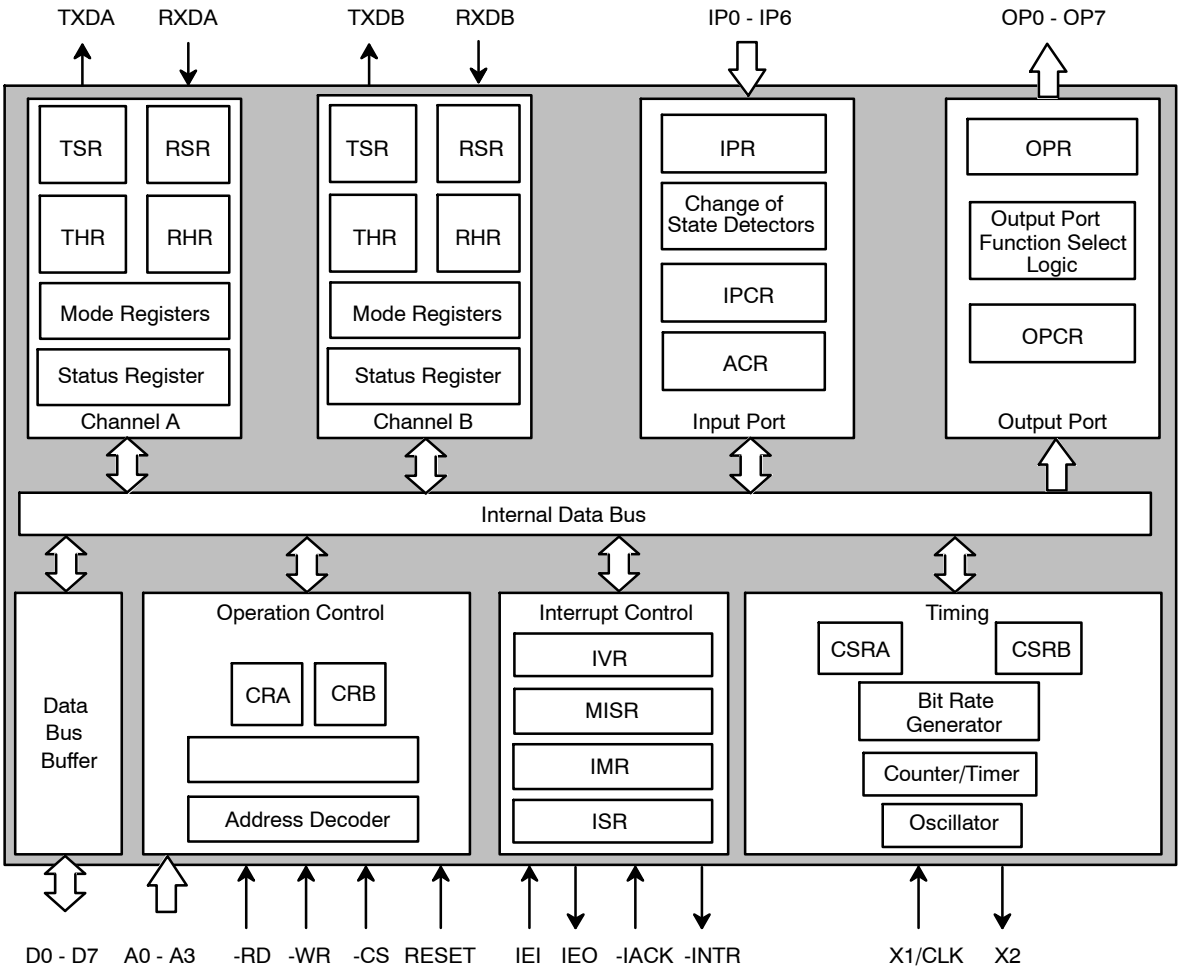
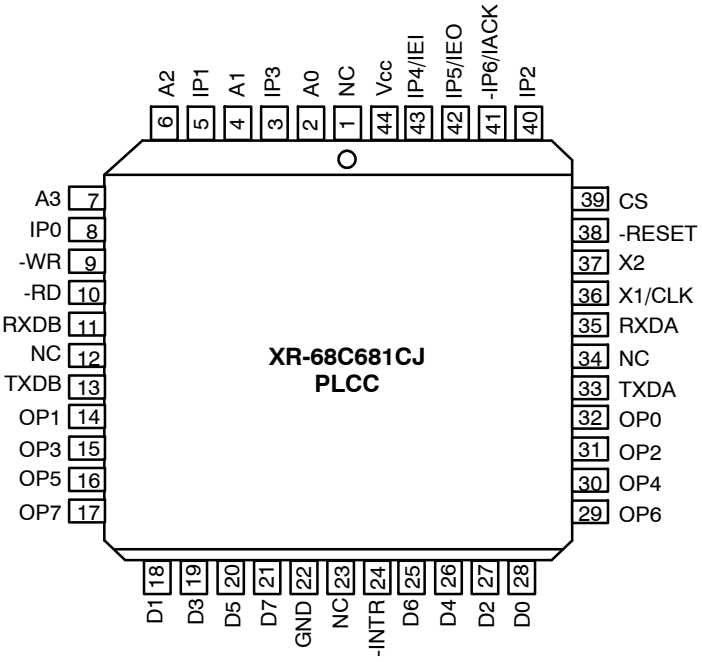
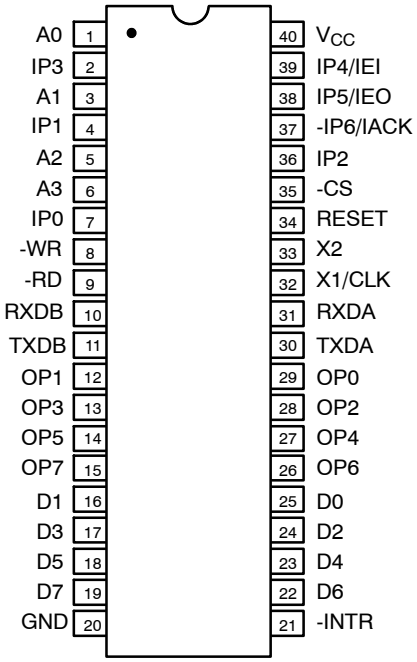


Figure 1. Block Diagram of the XR88C681

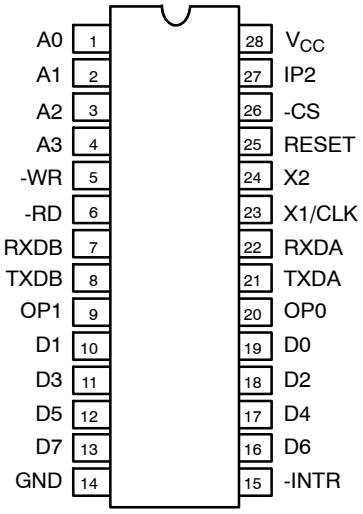
PIN CONFIGURATION



44 Lead PLCC



40 Lead PDIP, CDIP (0.600")



28 Lead PDIP (0.600")

PIN DESCRIPTION

44 PLCC	40 PDIP, CDIP	28 PDIP	Symbol	Type	Description
1			NC		**No Connection.**
2	1	1	A0	I	**LSB of Address Input.** This input, along with Address Inputs, A1 - A3 are used to select certain registers within the DUART device, during READ and WRITE operations with the CPU.
3	2		IP3 (TXCA - I) (RXCA - Z)	I	**Input Port 3.** General Purpose Input - When the DUART is operating in the I-mode, this input can also be used as the external clock input for the Channel A Transmitter (TXCA). When the DUART is operating in the Z-Mode, this input can be used as the external clock input for the Channel A Receiver (RXCA).
4	3	2	A1	I	**Address Input.**
5	4		IP1 (-CTSB)	I	**Input Port 1.** General Purpose Input - This input can also be used as the Active Low, “Channel B Clear to Send” input. (-CTSB)
6	5	3	A2	I	**Address Input.**
7	6	4	A3	I	**MSB of Address Input.** This input, along with Address Inputs, A0 - A2 are used to select certain registers within the DUART device, during READ and WRITE operations with the CPU.
8	7		IP0 (-CTSA)	I	**Input 0.** General Purpose Input - This input can also be used as the active-low, “Channel A Clear-to-Send” input. (-CTSA)
9	8	5	-WR	I	**Write Strobe (Active-Low).** A “low” on this input while -CS is also “low” writes the contents of the Data Bus into the addressed register, within the DUART. The transfer occurs on the rising edge of -WR.
10	9	6	-RD	I	**Read Strobe (Active Low).** A “low” on this input while -CS is also “low” places the contents of the addressed DUART register, on the data bus.
11	10	7	RXDB	I	**Receive Serial Data Input (Channel B).** The least significant bit of the character is received first. If external receiver clock, RXCB, is specified, the data is sampled on the rising edge of this clock.
12			NC		**No Connect.**
13	11	8	TXDB	O	**Transmitter Serial Data Output (Channel B).** The least significant bit of the character is transmitted first. This output is held in the high (marking state) when the transmitter is idle, disabled, or when the channel is operating in the local LOOPBACK mode. If an external transmitter clock is specified, TXCB, the transmitted data is shifted out of the TSR (Transmitter Shift Register) on the falling the edge of this clock.

44 PLCC	40 PDIP, CDIP	28 PDIP	Symbol	Type	Description
14	12	9	OP1 (-RTSB)	O	**Output 1 (General Purpose Output).** This output can also be programmed to function as the active-low, "Channel B Request-to-Send" Output (-RTSB).
15	13		OP3 (TXCB_1X) (RXCB_1X) (-C/T_RDY)	O	**Output 3 (General Purpose Output).** This output port can also be programmed to function as: the "Channel B Transmitter 1X clock" output (TXCB_1X), the "Channel B Receiver 1X clock" output (RXCB_1X), or the open drain, active-low "Counter/Timer Ready" output (-C/T_RDY).
16	14		OP5 (-RXRDY/ -FFULL_B)	O	**Output 5 (General Purpose Output Pin).** This output port pin can also be programmed to function as the open-drain, active-low, Channel B "Receive Ready" or "Receiver FIFO Full" indicator output (-RXRDY_B/-FFULL_B).
17	15		OP7 (TXRDY_B)	O	**Output 7. (General Purpose Output Pin).** This output port pin can also be programmed to function as the open-drain, active-low, "Transmitter Ready" indicator output for Channel B (-TXRDY_B).
18	16	10	D1	I/O	**Bi-Directional Data Bus.**
19	17	11	D3	I/O	**Bi-Directional Data Bus.**
20	18	12	D5	I/O	**Bi-Directional Data Bus.**
21	19	13	D7	I/O	**MSB of the Eight Bit Bi-Directional Data Bus.** All transfers between the CPU and the DUART take place over this bus (consisting of pins D0 - D7). The bus is tri-stated when the -CS input is "high", except during an IACK cycle (in the Z-Mode).
22	20	14	GND	PWR	**Signal Ground.**
23			NC		**No Connect.**
24	21	15	-INTR	O	**Interrupt Request Output (Active Low, Open Drain).** -INTR is asserted upon the occurrence of one or more of the chip's maskable interrupting conditions. This signal will remain asserted throughout the Interrupt Service Routine and will be negated once the condition(s) causing the Interrupt Request has been eliminated.
25	22	16	D6	I/O	**Bi-Directional Data Bus.**
26	23	17	D4	I/O	**Bi-Directional Data Bus.**
27	24	18	D2	I/O	**Bi-Directional Data Bus.**
28	25	19	D0	I/O	**LSB of the Eight Bit Bi-Directional Data Bus.** All transfers between the CPU and the DUART take place over this bus. The bus is tri-stated when the -CS input is "high", except during an IACK cycle (in the Z-Mode).
29	26		OP6 (-TXRDY_A)	O	**Output 6 (General Purpose Output).** This output pin can also be programmed to function as the open drain, active-low, "Transmitter Ready" indicator output for Channel A (-TXRDY_A).

44 PLCC	40 PDIP, CDIP	28 PDIP	Symbol	Type	Description
30	27		OP4 (RXRDY/ FFULL_A)	O	**Output 4 (General Purpose Output).** This output pin can also be programmed to function as the open-drain, active-low, “Receiver Ready” or “FIFO Full” indicator output for Channel A. (-RXRDY_A/-FFULL_A)
31	28		OP2 (TXCA_16) (TXCA-1X) (RXCA_1X)	O	**Output 2 (General Purpose Output).** This output pin can also be programmed to function as any of the following: The Channel A Transmitter 16X or 1X clock output (TXCA_16X or TXCA_1X), or the Channel A Receiver 1X clock output (RXCA_1X).
32	29	20	OP0 (-RTSA)	O	**Output 0 (General Purpose Output).** This output pin can also be programmed to function as the active-low, Request-to-Send output for Channel A (-RTSA).
33	30	21	TXDA	O	**Transmitter Serial Data Output (Channel A).** The least significant bit of the character is transmitted first. This output is held in the marking (high) state when the transmitter is idle, disabled, or operating in the Local LOOPBACK mode. If an external transmitter clock is specified, TXCA, the data is shifted out of the TSR (Transmitter Shift Register) on the falling the edge of the clock.
34			NC		**No Connect.**
35	31	22	RXDA	I	**Receive Serial Data Input (Channel A).** The least significant bit of the character is received first. If an external receiver clock, RXCA, is specified, the data is sampled on the rising edge of the clock.
36	32	23	X1/CLK	I	**Crystal Output of External Clock Input.** This pin is the connection for one side of the crystal and a capacitor to ground when the internal oscillator is used. If the oscillator is not used, an external clock signal must be supplied at this input. In order for the XR88C681 device to function properly, the user must supply a signal with frequencies between 2.0MHz and 4.0MHz. This requirement can be met by either a crystal oscillator or by the external TTL-compatible clock signal.
37	33	24	X2	O	**Crystal Input.** Connection for the one side of the crystal (opposite of X1/CLK). If the oscillator is used, a capacitor must also be connected from this pin to ground. This pin must be left open if an external clock is supplied at X1/CLK.

44 PLCC	40 PDIP, CDIP	28 PDIP	Symbol	Type	Description
38	34	25	RESET	I	**Master Reset (Active High).** Asserting this input clears internal registers, SR, ISR, IMR, OPR, OPCR, and initializes the IVR to 0F16. Asserting this input also stops the Counter/Timer, puts OP0 - OP7 in the high state, and places both serial channels in the inactive state with TXDA and TXDB outputs marking (high).
39	35	26	-CS	I	**Chip Select (Active Low).** The data bus is tri-stated when -CS is "high." Data transfers between the CPU and the DUART via D0 - D7 are enabled when -CS is "low".
40	36	27	IP2 (C/T_EX)	I	**Input 2. (General Purpose Input).** This input pin can also be programmed to function as the "Counter/Timer external clock" input (C/T_EX).
41	37		IP6 (RXCB)	I	**Input 6 (I-Mode).** General Purpose Input pin. This input pin can also be programmed to function as the External Receiver Clock for Channel B (RXCB).
41	37		-IACK	I	**Interrupt Acknowledge Input (Z-Mode).** Active Low. This input is the CPU's response to the Interrupt Request issued by the DUART device. When the CPU asserts this input, it indicates that the DUART's interrupt request is about to be serviced, and that the very next cycle will be an Interrupt Acknowledge Cycle. The DUART will respond to the CPU's Interrupt Acknowledge by placing the contents of the Interrupt Vector Register (IVR) on the data bus (D0 - D7).
42	38		IP5 (TXCB)	I	**Input 5 (I-Mode).** General Purpose Input pin. This pin can also be configured to function as the external clock input for the Transmitter of Channel B (TXCB).
42	38		IEO (Z-Mode)	O	**Interrupt Enable Output (Z-Mode).** Active High. This output pin is normally "high". However, either of the following two conditions can cause this output pin to be negated (toggled "low"). 1. If the IEI (Interrupt Enable Input) pin is "low". If IEO is "low" because of the IEI pin, IEO will toggle "high" once the IEI has toggled "high". 2. The DUART has issued an Interrupt Request to the CPU (-INTR pin is toggled "low"). If IEO is "low" because the DUART has requested an Interrupt, then IEO will remain "low", throughout the Interrupt Service Routine, until the CPU has invoked the "" command.
43	39		IP4 (RXCA)	I	**Input 4 (I-Mode).** General Purpose Input pin. This input pin can also be configured to function as the external clock input for the Receiver of Channel A (RXCA).
43	39		IEI (Z-Mode)	I	**Interrupt Enable Input (Z-Mode).** Active High. If this active-high input is at a logic "high", the DUART is capable of generating all non-masked Interrupt Requests to the CPU. If this input is at a logic "low", the DUART is inhibited from generating any Interrupt Requests to the CPU.
44	40	28	V_{CC}	PWR	**Most Positive Power Supply.**

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

Test Conditions: T_A = 0 - 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IH}	Input High Voltage (Military)	2.2			V	T_A = -55°C to 125°C
V_{IHX1}	Input High Voltage (X1/CLK)	4.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.4mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400□A
I_{IL}	Input Leakage Current	-25		25	□A	V_{IN} = 0 to V_{CC}
I_{ILSEL}	Select Pin Leakage Current	-30		+30	□A	V_{IN} = 0 to V_{CC}
I_{X1L}	X1 Input Low Current		-20		□A	V_{IN} = 0
I_{X2L}	X2 Input Low Current		-7		mA	
I_{XIH}	X1 Input High Current		20		□A	V_{IN} = V_{CC}
I_{X2H}	X2 Input High Current		20		□A	V_{IN} = V_{CC}
I_{LL}	Data Bus Tri-State Leakage Current	-10		10	□A	V_O = 0 to V_{CC}
I_{OC}	Open Drain Output Leakage Current	-10		10	□A	V_O = 0 to V_{CC}
I_{CCA}	Power Supply Current[4]		6	15	mA	Active Mode
I_{CCS}	Power Supply Current[4]		3	10	mA	Standby Mode

Notes

1. *Parameters are valid over the specified temperature and operating supply ranges. Typical values are 25°C, V_{CC} = 5V and typical processing parameters.*
2. *All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 50.*
3. *For prime grade N, P, J, L, M, ML, V_{CC} = 5V ± 10%.*
4. *Measured operating with a 3.6864MHz crystal and with all outputs open.*

AC ELECTRICAL CHARACTERISTICS [1, 2, 3]
Test Conditions: T_A = 0 - 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Reset Timing (See *Figure 51*)						
t_{RES}	RESET Pulse Width	1.0			□A	
XR88C681 Read and Write Cycle Timing (*Figure 52*)[4]						
t_{AS}	A0-A3 Setup Time to RD, WR Low	10			ns	
t_{AH}	A0-A3 Hold Time from RD, WR Low	0			ns	
t_{CS}	CS Setup Time to RD, WR Low	0			ns	
t_{CH}	CS Hold Time from -RD, -WR High	0			ns	
t_{RW}	-RD, -WR Pulse Width	225			ns	
t_{DD}	Data Valid from -RD Low		60	175	ns	
t_{DF}	Data Bus Floating from -RD High	10		100	ns	
t_{DS}	Data Setup Time to -WR High	100			ns	
t_{DH}	Data Hold Time from -WR High	5			ns	
t_{RWD}	High Time Between Reads and/or Writes[5, 6]		100		ns	
Z-Mode Interrupt Cycle Timing (*Figure 53*)						
t_{DIO}	IEO Delay Time from IEI			100	ns	
t_{IAS}	-IACK Setup Time to -RD Low[7]				ns	
t_{IAH}	-IACK Hold Time from -RD High		0		ns	
t_{EIS}	IEI Setup Time to RD Low		50		ns	
t_{EOD}	IEO Delay Time from -INTR Low			100	ns	
Port Timing (*Figure 54*)[4]						
t_{PS}	Port Input Setup Time to -RD/-CS Low	0			ns	
t_{PH}	Port Input Hold Time from -RD/-CS High	0			ns	
t_{PD}	Port Output Valid from -WR/-CS High			400	ns	
Interrupt Output Timing (*Figure 55*)						
t_{IR}	-INTR or OP3 - OP7 when used as Interrupts High from: Clear of Interrupts Status Bits in ISR or IPCR Clear of Interrupt Mask in IMR			300 300	ns ns	
Clock Timing (*Figure 56*)						

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CLK}	X1/CLK (External) High or Low Time	100			ns	
t_{CLK}	X1/CLK Crystal or External Frequency			7.372	MHz	

AC ELECTRICAL CHARACTERISTICS [1, 2, 3] (CONT'D)

Test Conditions: T_A = 0 - 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Clock Timing (*Figure 56*) (Cont'd.)						
t_{CTC}	Counter/Timer External Clock High or Low Time (IP2)	100			ns	
t_{CTC}	Counter/Timer External Clock Frequency	0		7.372	MHz	
t_{RTX}	RXCn and TXCn (External) High or Low Time[8]	220			ns	
f_{RTX}	RXCn and TXCn (External) Frequency					
	16X	0		16.0	MHz	
	1X	0		1.0	MHz	
Transmitter Timing (*Figure 57*)						
t_{TXD}	TXD Output Delay - TXC (External) Low			350	ns	
t_{TCS}	TXD Output Delay - TXC (Internal) Output Low			150	ns	
t_{RXS}	RXD Data Setup Time to RXC (External) High	240			ns	
t_{RXH}	RXD Data Hold Time from RXC (External) High	200			ns	

Notes

1. *Parameters are valid over the specified temperature and operating supply ranges. Typical values are 25°C, V_{CC} = 5V and typical processing parameters.*
2. *All voltages are referenced to ground (GND). For testing, input signal levels are 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate. See Figure 50.*
3. *AC test conditions for outputs: CL = 50pF, RL = 2.7k□ to V_{CC}.*
4. *If -CS is used as the strobing input, this parameter defines the minimum high time between -CSs.*
5. *Consecutive write operations to the same register require at least three edges of the X1 clock between writes.*
6. *This specification imposes a 6 MHz maximum 68000 clock frequency if a read or write cycle follows immediately after the previous read or write cycle. A higher 68000 clock can be used if this is not the case.*
7. *This specification imposes a lower bound on -CS and -IACK low, guaranteeing that they will be low for at least one CLK period.*
8. *The minimum high time must be at least 1.5 times the X1/CLK period and the minimum low time must be at least equal to the X1/CLK period if either channel's Receiver is operating in external 1X clock mode.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

DC Supply Voltage 7V
Storage Temperature ..... -65° C to 150° C
All Voltages with respect to Ground[2] ..... -0.5V to +7V

1. *Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the "Electrical Characteristics" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maximum.

SYSTEM DESCRIPTION

The XR88C681 consists of two independent, full-duplex communication channels; each consisting of their own Transmitter and Receiver. Each channel of the DUART may be independently programmed for operating mode and data format. The DUART can interface to a wide range of processors with a minimal amount of components. The operating speed of each receiver and transmitter may be selected from one of 23 internally generated fixed bit rates, from a clock derived from an internal counter/timer, or from an externally supplied 1x or 16x clock. The bit rate generator (the source of the 23 different fixed bit rates) can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the DUART attractive for split speed channel applications such as clustered terminal systems.

Receiver data is quadrupled buffered and the transmitter data is dual-buffered via on-chip FIFOs in order to minimize the risk of receiver overrun and to reduce overhead in interrupt driven applications. The DUART also provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving DUART is full, thus preventing loss of data.

The DUART also provides a general purpose 16 bit counter/timer (which may also be used as programmable bit rate generators), a 7 bit multi-purpose input port and an 8 bit multi-purpose output port (for the 40 pin DIP and 44 pin PLCC packages only).

PRINCIPLES OF OPERATION

Figure 1 presents an overall block diagram of the DUART. As illustrated in the block diagram, the DUART consists of the following major functional blocks:

- Data Bus Buffer
- Interrupt Control
- Input Port
- Serial Communication Channels A and B
- Operation Control
- Timing Control
- Output Port

A. DATA BUS BUFFER

The data bus buffer provides the interface between the internal (within the chip) and external data buses. It is controlled by the operation control block to allow data transfers to take place between the host CPU and the DUART.

B. OPERATION CONTROL BLOCK

The control logic of the Operation Control block receives operating commands from the CPU and generates proper signals to the various sections of the DUART. The Operation Control Block functions as the user interface to the rest of the device. Specifically, it is responsible for DUART Register Address Decoding, and Command Decoding. Therefore all commands to set baud rates, parity, other communication protocol parameters, start or stop the Counter/Timer or reading a “status register” to monitor data communication performance must go through the Operation Control Block.

The Operation Control Block will control DUART performance based upon the following input signals.

Address Inputs, A0 - A3
-RD
-WR
-CS
RESET

When using the 6800 family processor, the DUART will require some glue logic. Interfacing a 6800 Family Processor to the DUART can be easily achieved by including a small amount of external logic devices, as depicted in *Figure 2*.

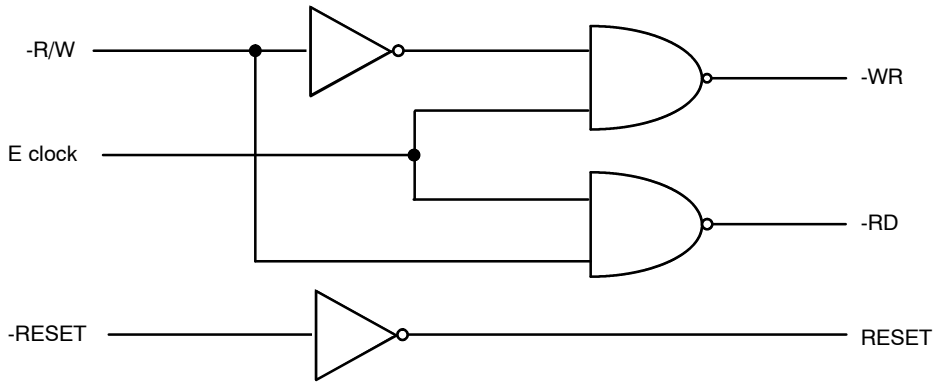


Figure 2. External Logic Circuitry required to interface a 6800 Family Processor to the XR88C681 Device

B.1 DUART Register Addressing

The addressing of the internal registers of the DUART is presented in *Table 1*. *Please note that some of the registers are "Read Only" and others are "Write Only".* Each channel is provided with the following dedicated (addressable) registers.

- Command Registers
- Mode Registers (MR1 and MR2)
- Status Registers
- Clock Select Registers
- Receiver Holding Register (RHR) and Transmit Holding Register (THR)

Additionally, the DUART contains the following registers that support/control both channels.

- Interrupt Status Register
- Interrupt Mask Register
- Masked Interrupt Status Register
- Interrupt Vector Register
- Auxiliary Control Register

And finally, the DUART also contains other registers that support functions other than serial data communication, such as the parallel ports and the counters/timers.

- OPCR- Output Port Control Register
- IPCR - Input Port Configuration Register
- CTUR - Counter/Timer Upper Byte Register
- CTLR - Counter/Timer Lower Byte Register

Address (Hex)	Read Mode Registers		Write Mode Registers	
	Register Name	Symbol	Register Name	Symbol
00	Mode Register, Channel A	MR1A, MR2A	Mode Register, Channel A	MR1A, MR2A
01	Status Register, Channel A	SRA	Clock Select Register, Channel A	CSRA
02	Masked Interrupt Status Register	MISR	Command Register A	CRA
03	Rx Holding Register, Channel A	RHRA	Tx Holding Register, Channel A	THRA
04	Input Port Change Register	IPCR	Auxiliary Control Register	ACR
05	Interrupt Status Register	ISR	Interrupt Mask Register	IMR
06	Counter/Timer Upper Byte Register	CTU	Counter/Timer Upper Byte Register	CTU
07	Counter/Timer Lower Byte Register	CTL	Counter/Timer Lower Byte Register	CTL
08	Mode Register, Channel B	MR1B, MR2B	Mode Register, Channel B	MR1B, MR2B
09	Status Register, Channel B	SRB	Clock Select Register, Channel B	CSRB
0A	RESERVED		Command Register, Channel B	CRB
0B	Rx Holding Register, Channel B	RHRB	Tx Holding Register, Channel B	THRB
0C	Interrupt Vector Register	IVR	Interrupt Vector Register	IVR
0D	Input Port	IP	Output Port Configuration Register (OP0 - OP7)	OPCR
0E	Start Counter/Timer Command	SCC	Set Output Port Bits Command	SOPBC
0F	Stop Counter/Timer Command	STC	Clear Output Port Bits Command	COPBC

Table 1. DUART Port and Register Addressing

Note: *The shaded blocks are not Read/Write registers but are rather "Address-Triggered" Commands.*

Table 1 indicates that each channel is equipped with two Mode Registers. Associated with each of these Mode Register pairs is a "Mode Register" pointer or MR pointer. Upon chip/system power up or RESET each MR pointer is "pointing to" the channel MR1n register. (*Please note that the suffix "n" is used at the end of many of the DUART registers symbols in order to refer, generically, to either channels A or B*). However, the contents of the MR pointer will shift from the address of the MR1n register to that of the MR2n register, immediately following any Read or Write access to the MR1n register. The MR pointer will continue to "point to" the MR2n register until a hardware reset occurs or until a "RESET MR POINTER" command has been invoked. The "RESET MR POINTER" command can be issued by writing the

appropriate data to the appropriate channel's Command Register. Therefore, both Mode Registers, within a given channel, have the same logical address. The features and functions of the DUART that are controlled by the Mode Registers are discussed in detail in *Section G.3*.

B.2 Command Decoding

Each channel is equipped with a Command Register. In general, the role of these Command Registers are to enable/disable the Transmitter, enable/disable the Receiver, along with facilitating a series of other miscellaneous commands. The bit format for each Command Register is presented herewith.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Miscellaneous Commands				**Enable/Disable Receiver**		**Enable/Disable Transmitter**	
See Following Text				00 = No Change 01 = Enable Rx 10 = Disable Rx 11 = Not valid (do not use)		00 = No Change 01 = Enable Tx 10 = Disable Tx 11 = Not Valid (Do not use)	

Table 2. (CRA, CRB) Bit Format for Command Registers of Channels A & B

The function of the lower nibble of the Command Registers is fairly straight-forward. This nibble is used to either enable or disable the Transmitter and/or Receiver.

The upper nibble of the Command Register is used to invoke a series of miscellaneous commands. *Table 3* defines the commands associated with the upper nibble of the Command Registers. *Please note that the upper nibble commands 1_{16} through B_{16} effects only the performance of Command Register's Channel*. However, commands C_{16} and D_{16} effects system (or chip) level operation.

Bit 7	Bit 6	Bit 5	Bit 4	Description
0	0	0	0	**Null Command.**
0	0	0	1	**Reset MRn Pointer.** Causes the Channel's MRn pointer to point to MR1n.
0	0	1	0	**Reset Receiver.** Reset the individual channel receiver as if a Hardware Reset has been applied. The Receiver is disabled and the FIFO is flushed.
0	0	1	1	**Reset Transmitter.** Resets the individual channel transmitter as if a Hardware Reset had been applied. The TXDn output is forced to a high level.

Table 3. Miscellaneous Commands, Upper Nibble of all Command Registers, Unless Otherwise Specified (Cont'd Next Page)

Bit 7	Bit 6	Bit 5	Bit 4	Description
0	1	0	0	**Reset Error Status.** Clears the Received Break (RB), Parity Error (PE), Framing Error (FE) and Overrun Error (OE) status bits, SR[7:3]. Specifically, if the Error Mode, for a particular channel is set at "Block" Error Mode, this command will reset all of the Receiver Error Indicators in the Status Register. In the Block Error Mode, once either a PE, FE, OE, or RB occurs, the error will continue to be flagged in the Status Register, until this command is issued. If the Error Mode, for a particular channel is set to "Character Error Mode", then the contents of the Status Register for PE, FE, and RB are reflected on a character by character basis. In the "Character Error Mode", the state of these indicators is based only upon the character that is at the top of the RHR. The OE indicator is always presented as a "Block Error Mode" indicator, and requires this command to be reset.
0	1	0	1	**Reset Break Change Interrupt.** Clears the channel's break change interrupt status bit.
0	1	1	0	**Start Break.** Forces the TXDn output low. The transmitter must be enabled to start a break. If the transmitter is empty, the start of the break may be delayed up to two bit times. If the transmitter is active, the break begins when the transmission of those characters in the THR is completed, viz., TXEMP must be true before the break will begin.
0	1	1	1	**Stop Break.** The TXDn line will go high within two bit times. TXDn will remain high for one bit time before the next character, if any, is transmitted.
1	0	0	0	**Set Rx BRG Select Extend Bit.** Sets the channel's "Receiver BRG Select Extend Bit" to 1.
1	0	0	1	**Clear Rx BRG Select Extend Bit.** Clears the channel's "Receiver BRG Select Extend Bit" to 0.
1	0	1	0	**Set Tx BRG Select Extend Bit.** Sets the channel's "Transmitter BRG Select Extend Bit" to 1.
1	0	1	1	**Clear Tx BRG Select Extend Bit.** Clears the channel's "Transmitter BRG Select Extend Bit" to 0.

Table 3. Miscellaneous Commands, Upper Nibble of all Command Registers, Unless Otherwise Specified (Cont'd)

Bit 7	Bit 6	Bit 5	Bit 4	Description
1	1	0	0	**Set Standby Mode (Channel A).** When this command is invoked via the Channel A Command Register, power is removed from each of the transmitters, receivers, counter/timer and additional circuits to place the DUART in the standby (or lower power) mode. *Please note that this command effects the operation of the entire chip*. Normal operation is restored by a hardware reset or by invoking the "SET ACTIVE MODE" command. **Reset IUS Latch (Channel B).** When this command is invoked via the Channel B Command Register, and the DUART is operating in Z-mode, it causes the Interrupt-Under-Service (IUS) latch to be reset. This, in turn, will cause the IEO output to toggle "high".
1	1	0	1	**Set Active Mode (Channel A).** When this command is invoked via the Channel A Command Register, the DUART is removed from the Standby Mode and resumes normal operation. **Set Z-Mode (Channel B).** When this command is invoked via the Channel B Command Register, the DUART is conditioned to operate in the Z-Mode. For a detailed discussion of the DUART's operation while in the Z-Mode, Please see *Section C.6.2*. (Not available for the 28 pin DIP packaged devices)
1	1	1	0	**Reserved.**
1	1	1	1	**Reserved.**

Table 3. Miscellaneous Commands, Upper Nibble of all Command Registers, Unless Otherwise Specified (Cont'd)

In addition to the commands which are available through the command registers, the DUART also offers "Address-Triggered" commands. These commands are listed in *Table 1*, "DUART PORT AND REGISTER ADDRESSING"; and are further identified by being "shaded" in *Table 1*. Specifically, these commands are:

- START COUNTER/TIMER COMMAND
- STOP COUNTER/TIMER COMMAND
- SET OUTPUT PORT BITS COMMAND
- CLEAR OUTPUT PORT BITS COMMAND

Each of these commands are invoked by either reading or writing data to their corresponding DUART addresses as specified in *Table 1*.

For Example:

The START COUNTER/TIMER COMMAND is invoked by the procedure of reading DUART address $0E_{16}$. *Please note that this "Read Operation" will not result in placing the contents of a DUART register on the data bus.* The only thing that will happen, in response to this procedure is the Counter/Timer will initiate counting. For a detailed discussion into the operation of the Counter/Timer, please see *Section D.2*.

Another example of an Address-Triggered commands is the "SET OUTPUT PORT BITS" Command. This command is invoked by performing a write of data to DUART address $0E_{16}$. When the user invokes this command, he/she is setting certain bits (to "1") within the OPR (Output Port Register). All other bits, within the OPR (not specified to be set), are not changed. The state of the output port pins are complements of the individual bits within the OPR. Hence, if OPR[0] is set to "1", the state of the corresponding output port pin, OP0, is now set to a logic "0". Consequently, one can think of the "SET OUTPUT PORT BITS" command as the "CLEAR OUTPUT PORT PINS" command. For a more detailed discussion into the operation of the Output Ports, please see *Section F*.

C. INTERRUPT CONTROL BLOCK

The Interrupt Control Block allows the user to apply the DUART in an "Interrupt Driven" environment. The DUART includes an interrupt request output signal (-INTR), which may be programmed to be asserted upon the occurrence of any of the following events:

- Transmit Hold Register A or B Ready
- Receive Hold Register A or B Ready
- Receive FIFO A or B Full
- Start or End of Received Break in Channels A or B
- End of Counter/Timer Count Reached
- Change of State on input pins, IP0, IP1, IP2, IP3

The Interrupt Control Block consists of an Interrupt Status Registers (ISR), an Interrupt Mask Registers (IMR), a Masked Interrupt Status Registers (MISR) and an Interrupt Vector Register (IVR). *Table 4* lists these registers, their address location (within the DUART).

Register	Description	Address Location (in DUART Address Space)
ISR	Interrupt Status Register	05_{16} (Read Only)
IMR	Interrupt Mask Register	05_{16} (Write Only)
MISR	Masked Interrupt Status Register	02_{16} (Read Only)
IVR	Interrupt Vector Register	$0C_{16}$

Table 4. Listing and Brief Description of Interrupt System Registers

The role and purpose of each of these registers are defined here.

C.1 Interrupt Status Registers (ISR)

The contents of the ISR indicates the status of all potential interrupt conditions. If any bits within these registers are toggled "high", then the corresponding condition has or is occurring. In general, the contents of the ISR will indicate to the processor, the source or the reason for the Interrupt Request from the DUART. Therefore, any interrupt service routine for the DUART should begin by reading either this register or the MISR (Masked Interrupt Status Register). The bit-format of the ISR is presented in *Table 5*:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change	**Delta Break B**	**RXRDY/ FFULLB**	**TXRDYB**	**Counter Ready**	**Delta Break A**	**RXRDY/ FFULLA**	**TXRDYA**
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

Table 5. ISR Bit Format

The definition of the meaning behind each of these bits is presented here.

ISR[7]: Input Port Change of State

If this bit is at a logic "1", then a change of state was detected at Input Port pins IP0 - IP3. The user would service this interrupt by reading the IPCR (if ISR[7] = 1). ISR[7] is cleared when the CPU has read the Input Port Configuration Register (IPCR). By reading the IPCR, the user will determine:

- The individual Input Port pin that changed state
- The final state of the monitored input ports, following the Change of State.

For a detailed description of the IPCR, see *Section F*.

Please note that in order to enable this Interrupt Condition, the user must do two things:

1. Write the appropriate data to the lower nibble of the Auxiliary Control Register, ACR[3:0]. In this step, the user is specifying which Input Pins should trigger an "Input Port Change" Interrupt request.

2. Write a logic "1" to IMR[7].

ISR[6] Delta Break Indicator - Channel B

When this bit is set, it indicates that the Channel B receiver has detected the beginning or end of a received break (RB). This bit is cleared (or reset) when the CPU invokes a channel B "RESET BREAK CHANGE INTERRUPT" command (see *Table 3*). For more information into the DUART's response to a BREAK condition, please see *Section G.2*.

ISR[5] RXRDY/FFULL B - Channel B Receiver Ready or FIFO Full

The function of this bit is selected by programming MR1B[6]. If programmed as the Receiver Ready indicator (RXRDYB), it indicates that at least one character of data is in RHRB and is ready to be read by the CPU. This bit is set when a character is transferred from the receiver shift register to RHRB and is cleared when the CPU reads the RHRB. If there are still more characters in RHRB after the read operation, the bit will be set again after RHRB is "popped".

If this bit is programmed as FIFO full indicator (FFULLB), it is set when a character is transferred from the RSR to RHRB and the transfer causes RHRB to become full. This bit is cleared when the CPU reads RHRB; and thereby "popping" the FIFO, making room for the next character. If a character is waiting in the RSR because RHRB is full, this bit will be set again after the read operation, when that character is loaded into RHRB.

Note:

If this bit is configured to reflect the FFULLB indicator, this bit will not be set (nor will produce an interrupt request) if one or two characters are still remaining in RHRB, following data reception. Hence, it is possible that the last two characters in a string of data (being received) could be lost due to this phenomenon.

ISR[4] TXRDYB - Channel B Transmitter Ready

This bit is a duplicate of TXRDY B, SRB[2].

This bit, when set, indicates that THRB is empty and is ready to accept a character from the CPU. The bit is cleared when the CPU writes a new character to THRB; and is set again, when that character is transferred to the TSR. TXRDYB is set when the transmitter is initially enabled and is cleared when the transmitter is disabled. Characters loaded into THRB while the transmitter is disabled will not be transmitted.

ISR[3] Counter Ready

In the TIMER mode, the C/T (Counter/Timer) will set ISR[3] once each cycle of the resultant square wave (available at the OP3 pin). ISR[3] will be cleared by invoking the "STOP COUNTER" command. Bear in mind, that in the TIMER mode, the "STOP COUNTER" command will not stop the C/T.

In the COUNTER mode, this bit is set when the counter reaches the terminal count (0000_{16}) and is cleared when the counter is stopped by a "STOP COUNTER" command. When the Counter/Timer is in the COUNTER Mode, the "STOP COUNTER" command will stop the Counter/Timer.

ISR[2]: Delta Break A - Channel A Change in Break

Assertion of this bit indicates that the channel A receiver has detected the beginning of or the end of a received break (RB). This bit is cleared when the CPU invokes a channel A "RESET BREAK CHANGE INTERRUPT" command. For more information into the DUART's response to a BREAK condition, please see *Section G.2*.

ISR[1] RXRDYA/FFULL A - Channel A Receiver Ready or FIFO Full

The function of this bit is selected by programming MR1A[6]. If programmed as the Receiver Ready indicator (RXRDYA), this bit indicates that there is at least one character of data in RHRA, and is ready to be read by the CPU. This bit is set when a character is transferred from the RSR to RHRA and is cleared when the CPU reads (or "pops") RHRA. If there are still more characters in RHRA, following the read operation, the bit will be set again after RHRA is "popped".

If this bit is programmed as the FIFO (RHR) full indicator (FFULLA), it is set when a character is transferred from the RSR to RHRA and the newly transferred character causes RHRA to become full. This bit is cleared when the CPU reads RHRA. If a character is waiting in the RSR because RHRA is full, this bit will be set again, following the read operation, when that character is loaded into RHRA.

Note:

If this bit is configured to reflect the FFULLA indicator, this bit will not be set (nor will produce an interrupt request) if

one or two characters are still remaining in RHRA, following data reception. Hence, it is possible that the last two characters in a string of data (being received) could be lost due to this phenomenon. Therefore, the user is advised to read RHRA until empty.

ISR[0]: Channel A Transmitter Ready
This bit is a duplicate of TXRDY A, SRA[2].

This bit, when set, indicates that THRA is empty and is ready to accept a character from the CPU. The bit is cleared when the CPU writes a new character to THRA; and is set again, when that character is transferred to the TSR. TXRDYA is set when the transmitter is initially enabled and is cleared when the transmitter is disabled. Characters loaded into THRA while the transmitter is disabled will not be transmitted.

C.2 Interrupt Mask Register (IMR)

The Interrupt Mask Register is a "Write Only" register which enables the user to select the conditions that will cause the DUART to issue an Interrupt Request to the processor. In other words, the user has the option of masking or blocking certain conditions from causing the DUART to issue an Interrupt Request. Therefore, the bit-format of the IMR is essentially the same as the ISR. However, for completeness, the Bit Format of the IMR is presented here.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Port Change	**Delta Break B**	**RXRDY/ FFULLB**	**TXRDYB**	**Counter Ready**	**Delta Break A**	**RXRDY/ FFULLA**	**TXRDYA**
0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 6. IMR Bit Format

If the user wishes to enable a certain interrupt, he/she should write a "1" to the bit within the IMR, corresponding to that Interrupt Condition. Likewise, to disable or mask out a certain condition causing an interrupt, the user should write a "0" to the bit location corresponding to that condition. To enable all interrupts the user would write FF_{16} (all "1"s) to this registers.

Please note that IMR is a Write Only Registers, and can therefore not be read by the processor.

C.3 Masked Interrupt Status Register (MISR)

The content of the MISR register is basically the results of ANDing the ISR and IMR together.

MISR Content = [ISR Contents] • [IMR Contents]

One limitation of DUART Interrupt Service Routines that rely on reading the ISR is that the bits within the ISR can toggle "high" due to their corresponding conditions whether or not they are enabled by the IMR. Therefore, the user, following reading the Interrupt Status Register, will have to make provisions for; and execute a "bit-by-bit" AND of the ISR and IMR contents. Since the IMR is a "Write Only" register and cannot be read by the processor, the contents of the IMR will have to be stored in system memory, for later recall. The additional hardware and software overhead required to support this activity can be eliminated via use of the MISR.

C.4 Interrupt Vector Register, IVR

This register is only used for Interrupt Vector generation when the DUART is commanded into the special Z-Mode. While in this mode, the contents of the IVR is typically related to the starting address of the DUARTs Interrupt Service Routine. Otherwise, in the I-Mode, Interrupt Vector generation is typically performed off-chip. When the DUART is operating in the I-Mode, the IVR can be used as general purpose read/write registers. The role of the IVR, while the DUART is operating in the Z-Mode is presented in *Section C.6*.

C.5 Limitations of the DUART Interrupt Structure

The Interrupt Structure offered by the DUART allows the user to program the DUART to generate interrupts in response to certain THR and RHR (FIFO) conditions; the Counter/Timer Ready condition, and to changes in the Break Condition (at the Receiver). However, aside from the "Delta Break Condition" (RB), the DUART's Interrupt Structure does not allow for interrupt requests due to

Receiver problems such as Parity Error (PE), Receiver Overrun Error (OE), or Framing Error (FE). The DUART also does not offer the user to ability to configure one of the output ports to relay the occurrence of any of these conditions. Therefore, unless the user is implementing some sort of "Data Link Layer" error checking scheme such as CRC, the user is advised to "validate" the received data by frequently reading the Status Register; and checking for any non-zero upper-nibble values. This is especially the case if the user has set the Error Mode to "Character" (MR1n[5] = 0).

C.6 Servicing DUART Interrupts

Interrupt servicing with the XR88C681 DUART falls into two broad categories: I-Mode and Z-Mode. I-Mode has historically been referred to as the "Intel" Mode. Likewise, the Z-Mode has been referred to as the "Zilog" Mode.

When the DUART is operating in the Z-Mode, the DUART will place an 8 bit "interrupt vector" on the data bus, to the CPU, during the "Interrupt Acknowledge" or IACK cycle. The CPU will read this interrupt vector from the Data Bus, and determine (from the Interrupt Vector data) the location of the appropriate interrupt service routine, in system memory. Additionally, the Z-Mode gives the user a hardware approach to prioritize the interrupt requests among numerous peripheral devices. This phenomenon is discussed in greater detail in *Section C.6.2*.

When the DUART is operating in the I-Mode, the DUART will not provide any interrupt vector information to the CPU, during the IACK cycle. Interrupt Vector information, or any means to route program control to the appropriate Interrupt Service Routine, is accomplished external to the DUART.

The DUART will be in the I-Mode following power up or a hardware reset. The user must invoke the "Set Z-Mode" command, in order to command the DUART into the Z-Mode.

Although the I-Mode has been referred to as the "Intel" Mode, and the Z-Mode as the "Zilog" Mode; this does not mean that the user should only operate the DUART in the Z-Mode when interfacing a Zilog microprocessor, or in the I-Mode when interfacing to an Intel microprocessor. The division between I-Mode and Z-Mode is not necessary along "corporate" lines. If you are interfacing the DUART to the following microprocessors/ microcontrollers, then the DUART must operate in the I-Mode.

- 8051□P
- 8080□CP
- 8085□P
- 68HC11□C
- Z-80□P (Interrupt Modes 0 and 1)

However, the DUART should be operating in the Z-Mode when interfacing the following microprocessors/ microcontrollers.

- 8088□P
- 8086□P
- 80286 - 80486□Ps
- Pentium□P
- Z-80□P (Interrupt Modes 2)

The next few sections will provide detailed discussions of DUART/Microprocessor interfacing and interrupt processing on each of the above-mentioned microprocessors. From this discussion, a detailed description of I-Mode Interrupt processing and Z-Mode Interrupt processing will emerge.

C.6.1 I-Mode Interrupt Servicing

The DUART will be in the I-Mode following power up of the IC, or a hardware reset. In general, a CPU interfacing to a DUART operating in the I-Mode, will function as follows, during interrupt servicing.

If the DUART requires interrupt service from the CPU, it will asserts the -INTR pin to the CPU. Once the CPU has detected the interrupt request, it will determine the location of the appropriate interrupt service routine, and will branch program control to that location. The CPU will accomplish all of this without providing an "Interrupt Acknowledge" signal or any further interaction with the DUART. Once the CPU has eliminated the cause(s) of the DUART's interrupt request, the DUART will then negate its -INTR pin. The CPU will then exit the "DUART" interrupt service routine and will resume normal processing.

In general there are two approaches that CPUs commonly use to locate the appropriate interrupt service routine, when interfaced with an I-Mode DUART.

- Direct Interrupt Processing
- (External) Vectored-Interrupt Processing

Direct Interrupt Processing

If a CPU employs "Direct Interrupt Processing" then once the CPU has detected the interrupt request, and has completed its current instruction, the CPU will branch

program control to a specific location in system memory. For CPUs that employ direct interrupts, this “location” is fixed by the CPU circuitry itself.

For Example:

If the -INT0 interrupt request input pin, of the 8051□C, is asserted, the CPU will branch program control to location 0003_{16} in system memory. This location is fixed (by circuit design of the 8051□P) and cannot be changed by the user.

(External) Vectored Interrupt Processing

CPUs that employ this form of interrupt processing typically have an Interrupt Acknowledge output pin. This “IACK” or “-INTA” output will be used to gate “interrupt vector” information onto the Data Bus, via external (non-DUART) hardware. The term “External” is used to describe this form of vectored-interrupt processing; because the location of the interrupt service routine is determined by hardware “external” to the DUART. For some CPUs, (such as the 8080A and the 8085□P), this “interrupt vector” information is a one byte op-code for a CALL instruction to a special “RESTART subroutine”. The location of this “RESTART subroutine” is fixed by CPU circuit design. If the user employs this approach for interrupt processing, he/she is responsible for insuring that either the interrupt service routine, or an unconditional branch instruction (to the interrupt service routine) resides at this location in memory.

Each of these Interrupt Processing techniques will be presented in greater detail in the following sections.

As mentioned earlier, the DUART should be operating in the I-Mode, when interfaced to the □P/□C presented in *Table 7*. *Table 7* also presents the type of interrupt processing that is employed by each of these □Ps/□Cs.

□P/□C	Type of Interrupt Processing	Comments
8051□C	Direct	The 8051 □C has two external Interrupt Request inputs: -INT0 and -INT1.
8080A□P	External Vectored	The 8080A □P will allow the use of up to 8 different op codes for “CALL” instructions to the Interrupt Service Routines. The 8080A CPU module will output an interrupt acknowledge output, -INTA, which can be used to “gate” the “CALL” instructions on to the Data Bus.
8085□P	Direct and External Vectored	The 8085 □P has three “Direct” external Interrupt Request inputs: RST 7.5, RST 6.5, and RST 5.5. Additionally, this □P has the exact same “vector” options as does the 8080A □P.
68HC11□C	Direct	The 68HC11 □C has a single “maskable” external Interrupt Request input; -IRQ.
Z-80□P (Interrupt Mode 0)	External Vectored	The Z-80 CPU uses the exact same approach as presented for the 8080A CPU.
Z-80□P	Direct Interrupt	The Z-80 will branch to 0038H in system memory if the -INT interrupt request pin is asserted.

Table 7. Summary of □P/□C and their types of Interrupt Processing (I - Mode)

The information presented in *Table 7* is discussed in detail in the following sections.

C.6.1.1 8051 Microcontroller

The 8051 family of microcontrollers is manufactured by Intel and comes with a variety of amenities. Some of these amenities include:

- On chip serial port
- Four 8 bit I/O port (P0 - P3)
- Two 16 bit timers
- 4k bytes of ROM
- 128 bytes of RAM

Figure 3 presents a block diagram of the 8051 microcontroller, and *Figure 4* presents the pin out of this device.

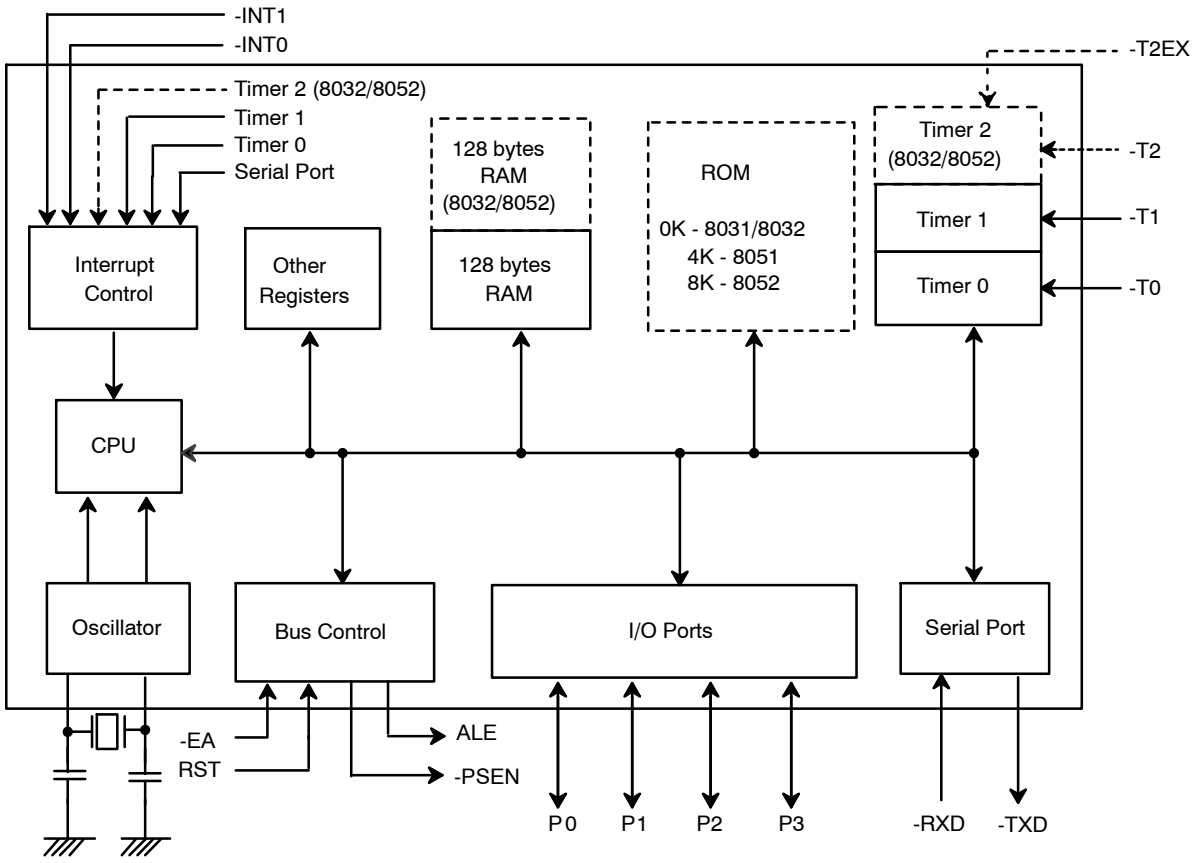


Figure 3. Block Diagram of the 8051 Microcontroller

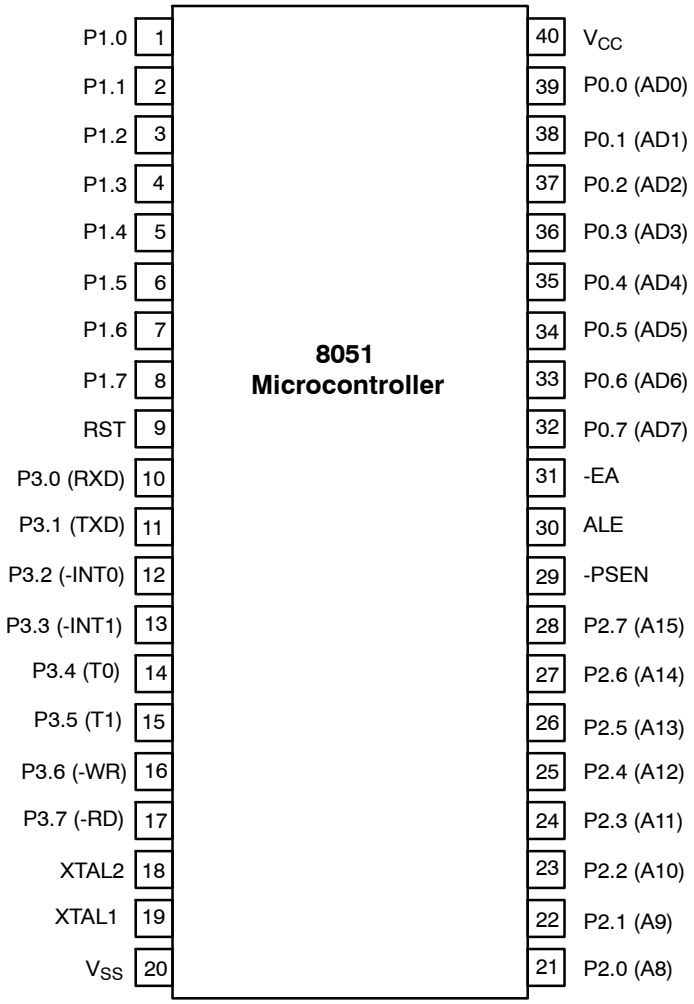


Figure 4. Pin Out of the 8051 Microcontroller

The 8051□C consists of 4 8-bit I/O ports. Some of these ports have alternate functions, as will be discussed here.

Port 0 (P0.0 - P0.7)

This port is a dual-purpose port on pins 32 - 39 of the 8051 IC. In minimal component designs, it is used as a general purpose I/O port. For larger designs with external memory, it becomes a multiplexed address and data bus (AD0 - AD7).

Port 2 (P2.0 - P2.7)

Port 2 (Pins 21 - 28) is a dual-purpose port that can function as general purpose I/O, or as the high byte of the address bus for designs with external code memory of more than 256 bytes of external data memory (A8 - A15).

Port 1 (P1.0 - P1.7)

Port 1 is a dedicated I/O port on pins 1 - 8. The pins, designated as P1.0, P1.1, P1.2, ..., are available for interfacing as required. No alternative functions are assigned for Port 1 pins; thus they are used solely for interfacing to external devices. Exceptions are the 8032/8052 ICs, which use P1.0 and P1.1 either as I/O lines or as external inputs to the third timer.