Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

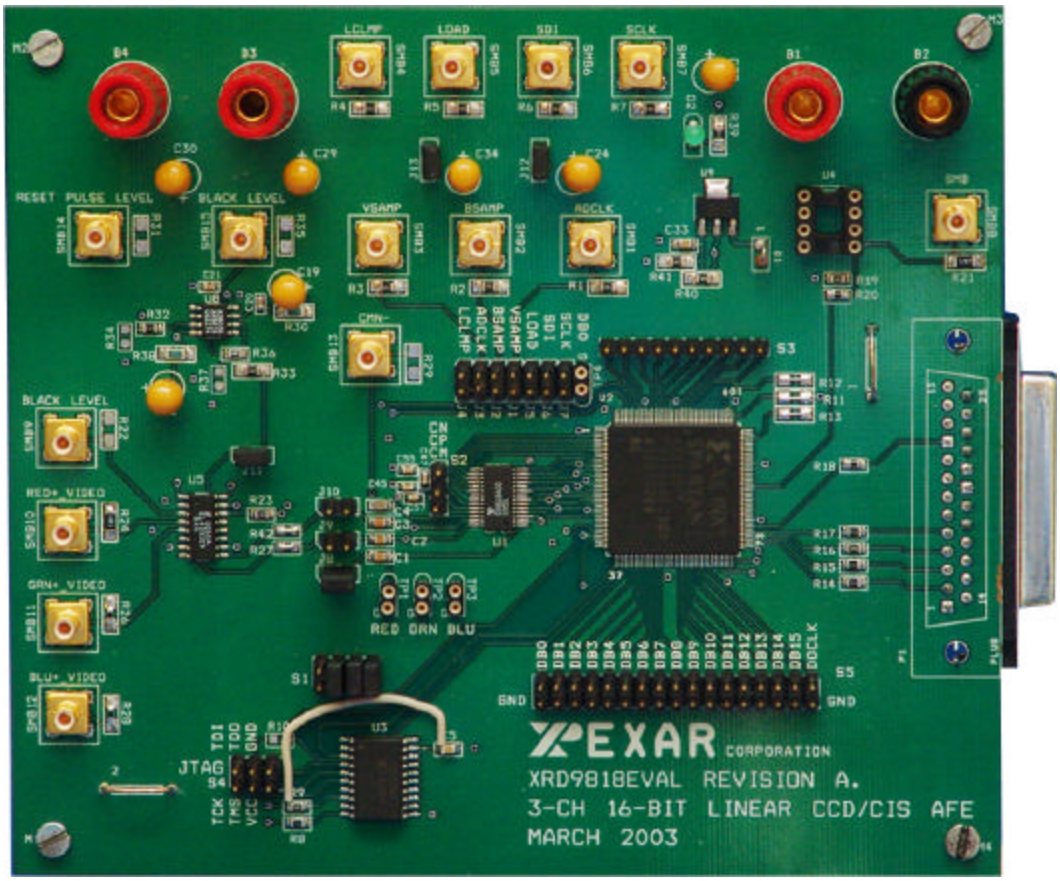
We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

XRD9818EVAL

Evaluation System User Manual



1.0 FEATURES

- XRD9818 28-pin TSSOP
- FPGA - Xilinx Spartan II XC2S50
- In-System PROM XC18V01
- Graphical User Interface (GUI) with 25-pin Din Connector for a Standard Parallel Port Interface
- Single Oscillator for Complete Timing Generation and Control
- Analog Switch (EL4331) for Emulating CCD Signals
- Clamping Amplifier (AD8036) for Reset Pulse Emulation
- Line Clamp Control for 40,000 Pixels
- De-Multiplexed Output Provided on a 17-pin Header including a Digital Output Clock

2.0 GENERAL DESCRIPTION

The XRD9818EVAL board is designed to be a test platform that provides a means to evaluate the performance and functionality of the XRD9818ACG. The eval board contains a Xilinx FPGA that provides all timing signals required for the proper operation of the XRD9818ACG. The timing and functionality of the FPGA will adjust and conform to the mode of operation of the XRD9818ACG. A Graphical User Interface (GUI) allows the evaluation platform to be configured to setup and test the XRD9818ACG in any of its possible modes of operation. The evaluation system contains emulation circuitry that provides a pseudo CCD signal including a reset pulse if desired.

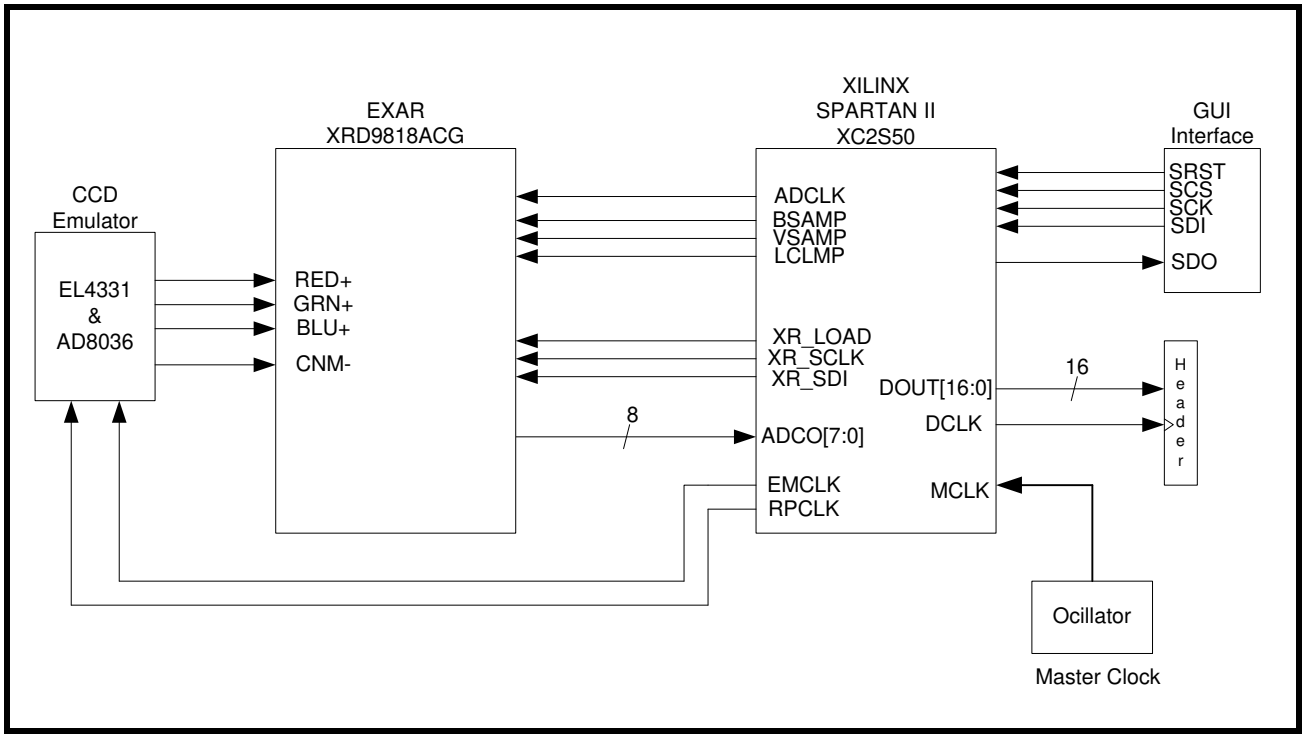


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF XRD9818EVAL

3.0 XRD9818EVAL APPLICATION PLATFORM

The XRD9818EVAL is an evaluation PCB layout designed to test functionality and performance of the XRD9818. The evaluation platform is controlled via a GUI interface on a PC and requires only power supplies, inputs to the CCD emulator and test equipment (Logic Analyzer, Oscilloscope) in order to evaluate most of the functional and performance aspects of the XRD9818. The following sections describe the functional blocks that make up the XRD9818EVAL system.

3.1 Graphical User Interface (GUI)

The GUI provides all serial port configurations for the XRD9818 plus options for controlling the XRD9818EVAL setup. To use the XRD9818 GUI simply run XRD9818.exe file and initiate "Start Test" located in the "TEST" pull down menu.

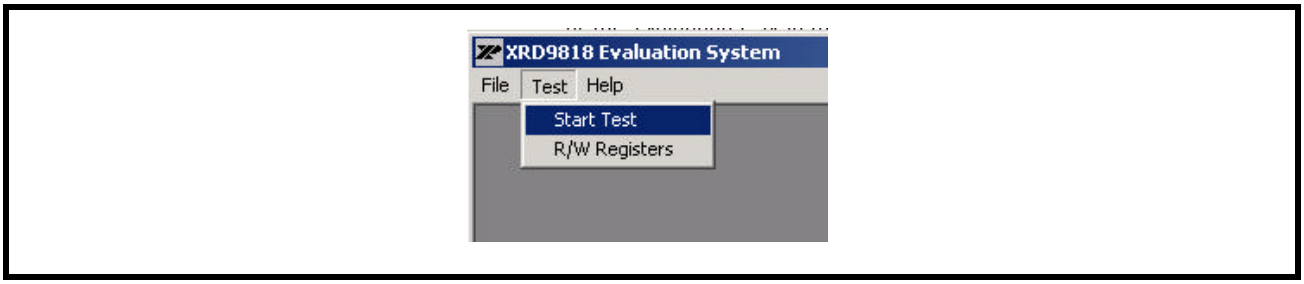


FIGURE 2. OPEN XRD98181 GUI

The GUI is broken into 7 sections that relate to various register functions of the XRD9818 and control features of the evaluation system: Color Options, Mode Options, Delay Registers, Polarity Options, Control Options, CPLD Options and Register Dump. Any changes become activated when the "Update" button is hit.

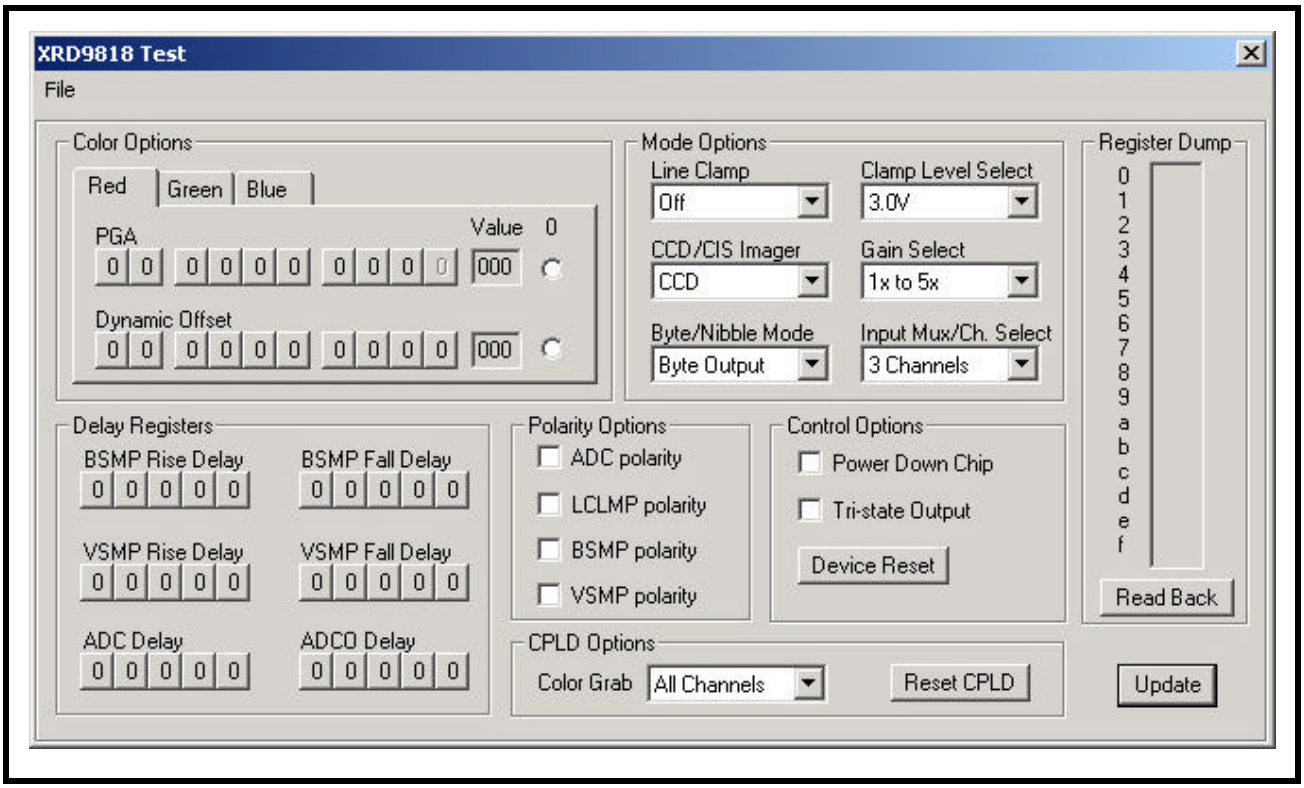
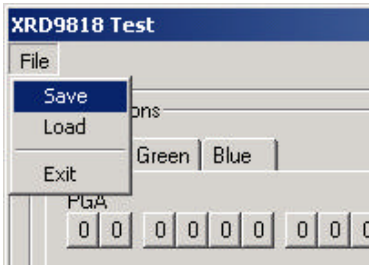


FIGURE 3. XRD9818 (GUI) GRAPHICAL USER INTERFACE

Configurations can be saved and reloaded via the "File" pull down control located in the upper left hand corner of the GUI display

FIGURE 4.



3.1.1 Color Options

The XRD9818's Gain and Offset controls for the individual channels: Red, Green and Blue (registers 0 thru 5), are controlled here. To modify the gain or offset values simply click on the bit you want to change. It will toggle between a "1" and a "0". The register value, in HEX, is shown just to the right. To zero out the register contents (reset to default value) simply set the "0" bit just to the right of the register value.

For the definition of the gain and offset registers see the XRD9818 data sheet.

3.1.2 Mode Options

This section sets the variables defined in the XRD9818's MODE 1 register. Channel selection, clamp level, output data format, gain range select, imager mode and line clamp operation are defined by the pull down tabs. Not only is the XRD9818's internal MODE 1 register is programmed but the FPGA will automatically adjust the system timing where needed to evaluate the device in the desired configuration.

For the definition of the MODE 1 register see the XRD9818 data sheet.

3.1.3 Delay Registers

They set the internal delays added to the BSAMP, VSAMP, ADCLK and ADCO (data output delay). Delays can be added to the sampling clocks (BSAMP, VSAMP & ADCLK) and data valid to help maximize performance of the XRD9818 and it's flexibility to externally applied timing.

For the definition of the delay registers see the XRD9818 data sheet.

3.1.4 Polarity Options & Control Options

This section sets the variables defined in the XRD9818's MODE 2 register. The polarity of the input timing to the XRD9818 can be individually set to be either active high (default) or active low. Power down and output enable are set via the Control Options interface.

3.1.5 Register Dump

The internal register configuration of the XRD9818 can be read back via the register dump. When the "ReadBack" button is hit the register configuration is read and displayed, in hex. The registers are listed from top to bottom by address.

A description of the readback operation is described in the XRD9818 data sheet.

3.1.6 CPLD options

The channel output sample clock is defined by the Color Grab. The Xilinx FPGA provides a data valid clock to the data header (S5) to be used to sample the output data. For example, if the XRD9818 is being operated in 3-CH mode all three channel's output data is sampled when the "Color Grab" is set to All Channels. Individual channel outputs can be sampled while in 3-CH operation by selecting the appropriate option. If "Red Channel" is selected, the CPLD supplies a sample clock only when the red channel data is available at S5.

The "Reset CPLD" button is for use upon initialization of the evaluation platform or if a system reset is needed.

3.2 Spartan II FPGA (XC2S50)

At the heart of the evaluation platform is the Spartan II. The FPGA provides the timing, control and pattern generation for the complete evaluation of the XRD9836. It reads the control information from the GUI and performs the appropriate write/read operation with the XRD9818. In addition to configuring the XRD9818 it will provide the appropriate timing signals to the evaluation system required to operate the XRD9818 in that mode. For example, if the XRD9818 is configured for 3-CH, CCD mode and nibble output operation the FPGA will provide the correct timing adjustments to the ADCLK, BSAMP, VSAMP, emulator clks, and 16bit out latch with sample clock so that the user does not need to adjust any of their equipment.

3.3 In-System PROM (XC18V01)

The FPGA can be programmed in two ways. A standard JTAG header is provided to allow programming each time the XRD9818EVAL is powered up. Or, an in-system PROM is provided to automatically program the FPGA upon power up. The JTAG header allows flexibility to provide verilog source codes for customer verification.

3.4 25-DIN Parallel Connector for PC Interface

The 25-DIN connector establishes the connection for the GUI control over the XRD9818EVAL through the parallel port of a PC. The GUI provides all serial port configurations XRD9818 plus options for controlling the XRD9818EVAL. When selecting options through the GUI, the program bursts the FPGA input with the pattern shown below in Figure 5. Please note that the pattern is not the same as the serial write pattern to the serial timing port of the XRD9818. The extra SCLK's after SCS goes back high are required for a readback operation from the 9818's internal registers. If the evaluation platforms is performing a readback operation the first clock after SCS goes high is required to latch the parallel data output from the 9818 and the next 10 clocks shift out the register content data, msb first.

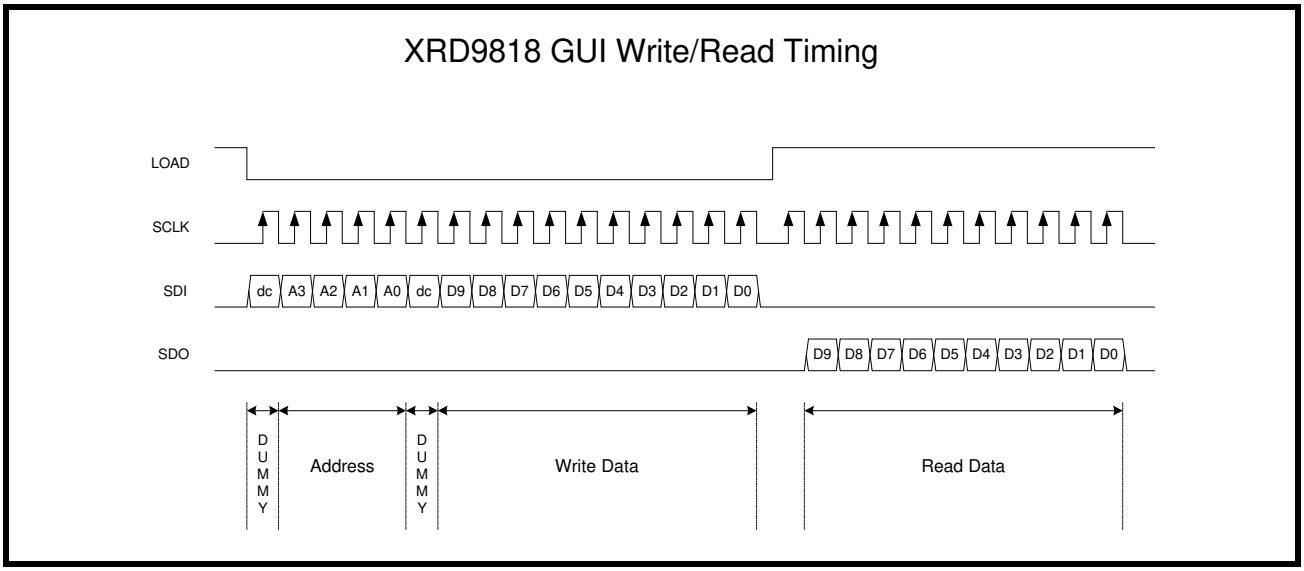


FIGURE 5. XRD9818EVAL GUI INTERFACE TIMING

3.5 CCD Emulator Circuitry

The emulation circuitry is intended to provide a pseudo CCD signal in order to evaluate the XRD9818 when configured for CCD operation. This is accomplished by the use of an analog switch (EL4331C) as seen in the evaluation board schematic . The basic function of the EL4331C (U5) is to switch each channels output between the its two inputs signals according to the polarity of the EMCLK timing signal. The inputs for each channel will be used to emulate the black reference level and video level of a CCD signal. If you look at the Figure 6 below you will see that the EMCLK connects the Black_Level (INxA - pins 3, 6, 12 of U5) input to the output when high and the Video input (INxB - pins 4, 5, 11 of U5) when the EMCLK is low. The resulting output signal as shown in the example timing for a Black Level=5V and a Video=4V is a signal toggling between 5V and 4V with the EMCLK.

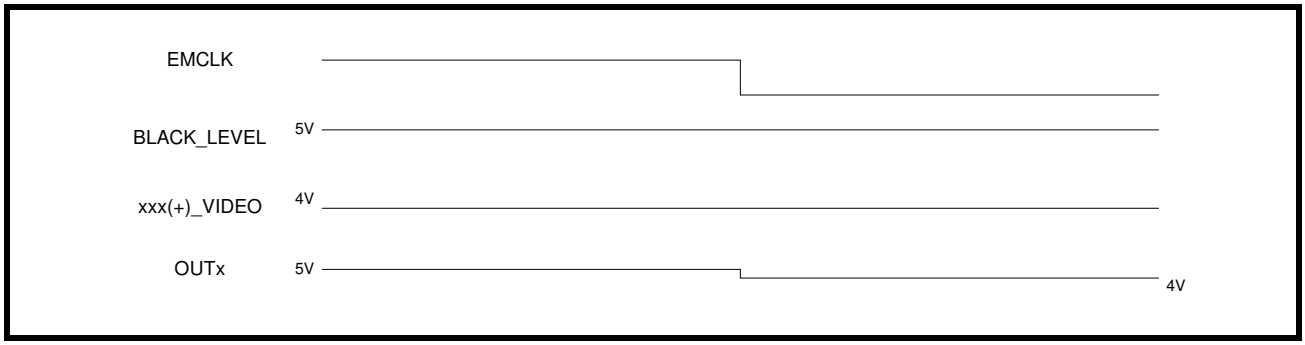


FIGURE 6. BASIC FUNCTION OF ANALOG SWITCH

To be able to test the XRD9818 for DNL & INL type specifications a sine wave generator can be connected to the Video input that has its peaks at 5V and 2V. This will cause the output of the XRD9818 to generate a digital sinewave that goes from zero code to full scale under the following conditions:CCD mode, GS=0, gain=1x, and offset reg adjusted to correct for any system offsets.

A reset pulse can be added to the emulated CCD signal by the use of the clamping amplifier (U8). It operates on the same principle as the EL4331 but has a faster settling time. The reset pulse can be adjusted by the input levels to the device. The clocking is done by the RSCLK provided from the FPGA. An example of an emulated CCD signal with reset pulse is shown below in Figure 7.

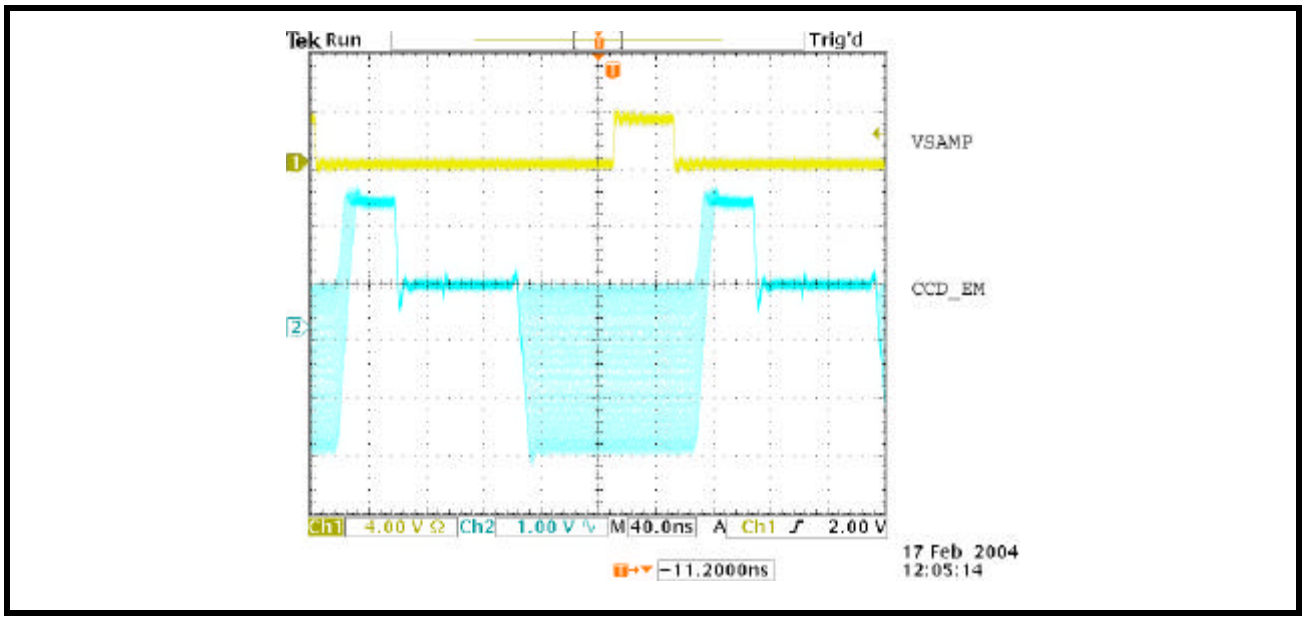


FIGURE 7. EXAMPLE OF CCD EMULTOR OUTPUT WITH RESET PULSE

3.6 Digital Output Interface

The interface to a Logic Analyzer is a 17x2 header (S5). It provides 16 bits of data, latch clock and individual ground for each signal. The rising edge of the latch clock is intended to identify when data is valid.

4.0 EVALUATION BOARD - POWER, JUMPER AND HEADER INFORMATION

TABLE 1:

IDENTIFIER	NAME	DESCRIPTION
B1	3V	Eval Board Power (3.3V typically)
B2	GND	Eval Board Ground
B3	5V_VCC	Positive Power Supply for Pixel Emulator
B4	-5V_VEE	Negative Power Supply for Pixel Emulator
J1 - J7	External Timing Jumpers	Used when external timing is applied and FPGA is not used to supply system timing.
J8, J9 & J10	Emulator Input Jumpers	Series jumpers to connect/isolate XRD9818 analog inputs.
J11	Emulator Reset Pulse Jumper	Used to create Reset pulse as part of emulated CCD pixel input
J12 & J13	XRD9818 Power Jumpers	Used to Isolate the XRD9818 from Eval Board for IDD measurements.
S1	Analog Input Header	Used to ground XRD9818 analog inputs
S2	Reference Header	Test points for CAPP, CAPN, & CMREF
S3	GPIO Header	General purpose pins that can be used for debug of FPGA
S4	JTAG Header	JTAG header used to program PROM & FPGA
S5	Data Output Header	Logic analyzer header for reconstructed 16bit digital outputs
P1	Parallel Port Interface	25-pin Din Connector standard parallel port interface for GUI control

5.0 REWORK INFORMATION

Jumper near U3 (PROM) to supply power (VDD3V) to pins 18, 19 & 20.

6.0 XRD9818EVAL SCHEMATICS

FIGURE 8. XRD9818 & SPARTAN II

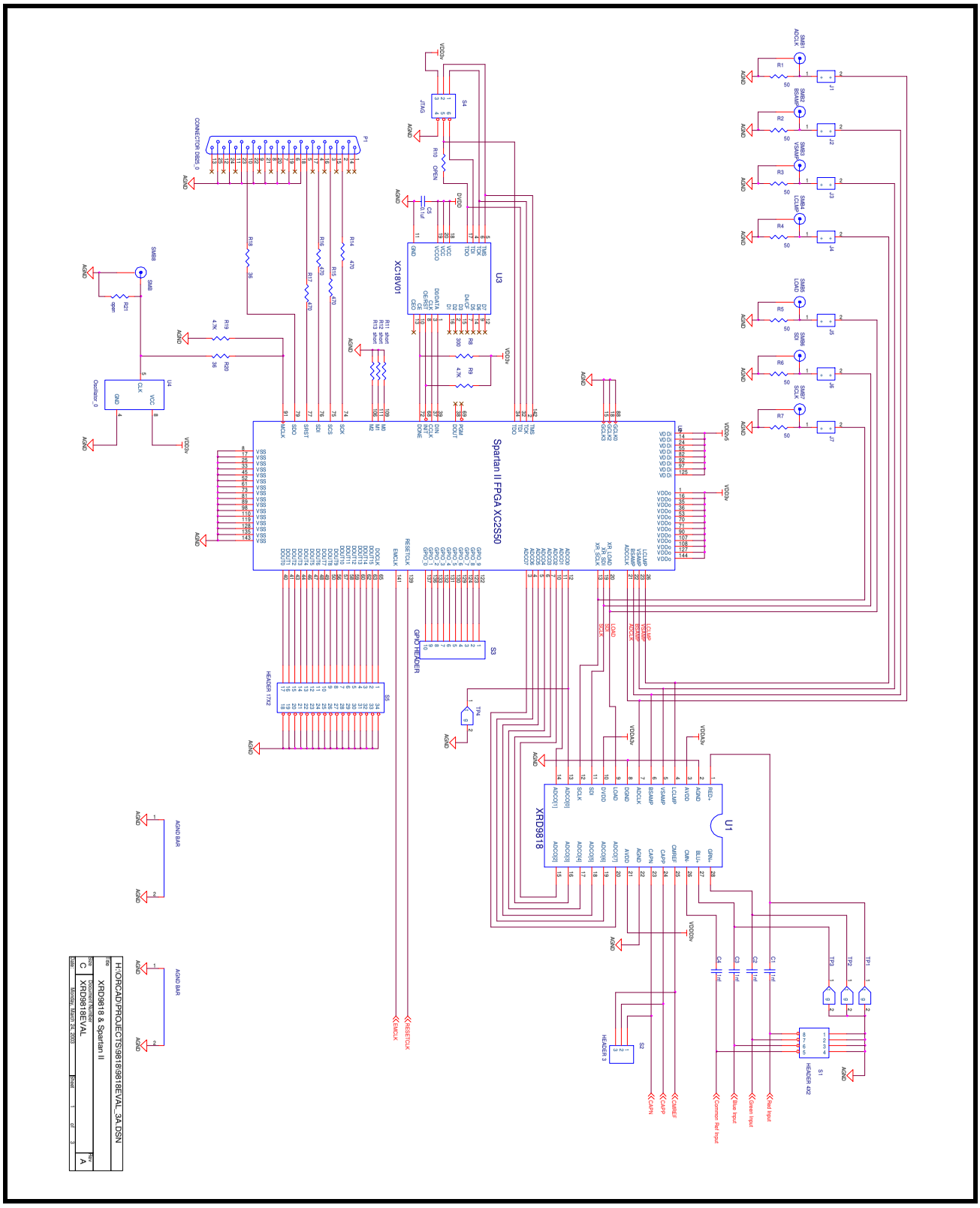


FIGURE 9. CCD EMULATOR

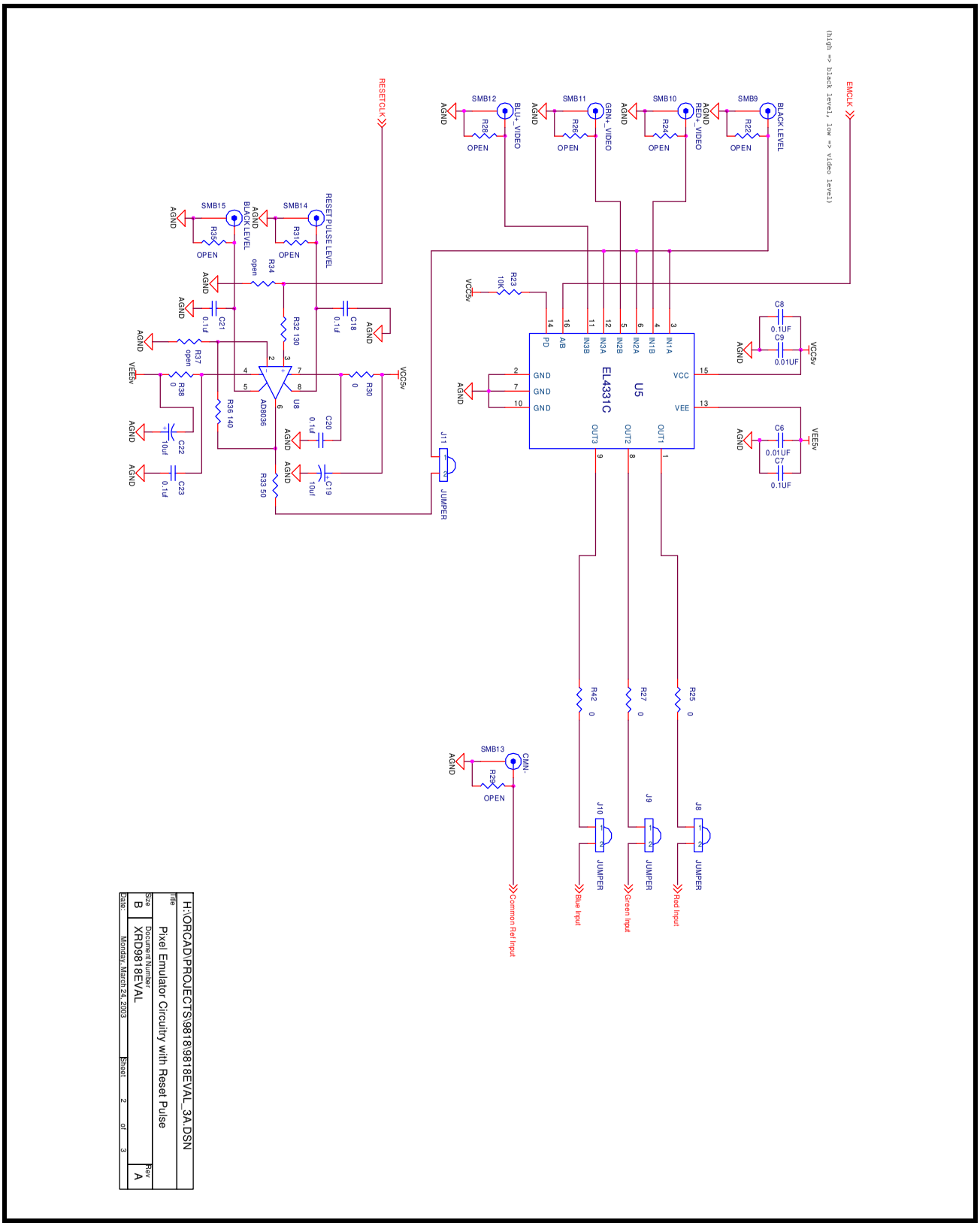


FIGURE 10. POWER AND BYPASS CIRCUITRY