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A New Direction in Mixed-Signal

January 2014

XRP6658

1A 1.5MHz PFM/PWM Synchronous Step-Down Converter

Rev. 1.6.0

GENERAL DESCRIPTION

The XRP6658 is a synchronous current mode PWM step down (buck) converter capable of delivering up to 1 Amp of current and optimized for portable battery-operated applications.

Based on a current mode 1.5MHz constant frequency PWM control scheme, the XRP6658 reduces the overall component count and solution footprint as well as provides a low output voltage ripple and excellent line and load regulation. It also implements a PFM mode to improve light load efficiency as well as a 100% duty cycle LDO mode. Output voltage is adjustable to as low as 0.6V with a better than 3% accuracy while a low quiescent current supports the most stringent battery operating conditions.

Built-in over temperature and under voltage lock-out protections insure safe operations under abnormal operating conditions.

The XRP6658 is offered in a RoHS compliant, "green"/halogen free 5-pin SOT23 package.

APPLICATIONS

- **Portable Equipments**
- **Battery Operated Equipments**
- **Audio-Video Equipments**
- **Networking & Telecom Equipments**

FEATURES

- **Guaranteed 1A Output Current**
 - Input Voltage: 2.5V to 5.5V
- **1.5MHz PWM Current Mode Control**
 - PFM Mode Operations at Light Load
 - 100% Duty Cycle LDO Mode Operations
 - Achieves 97% Efficiency
- **Adjustable Output Voltage Range**
 - As Low as 0.6V with $\pm 3\%$ Accuracy
- **Internal Compensation Network**
- **15 μ A Quiescent Current**
- **Over Temperature & UVLO Protections**
- **RoHS Compliant "Green"/Halogen Free 5-Pin SOT23 Package**

TYPICAL APPLICATION DIAGRAM

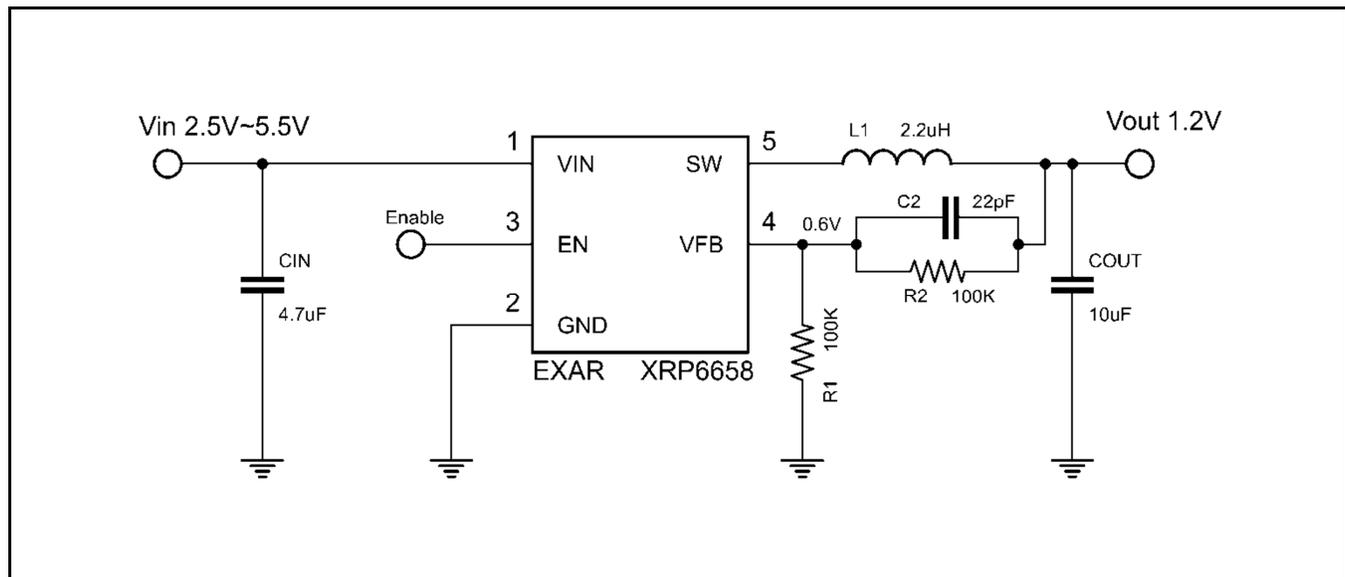


Fig. 1: XRP6658 Application Diagram

1A 1.5MHz PFM/PWM Synchronous Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Input Voltage V_{IN} -0.3V to 6.0V
 EN, V_{FB} Voltages -0.3V to V_{IN}
 SW Voltage -0.3V to ($V_{IN} + 0.3V$)
 Storage Temperature -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 260°C
 ESD Rating (HBM - Human Body Model) 2kV
 ESD Rating (MM - Machine Model) 200V
 Junction Temperature (Notes 1, 3) 150°C

OPERATING RATINGS

Input Voltage Range V_{IN} 2.5V to 5.5V
 Ambient Temperature Range T_A -40°C to 85°C
 Junction Temperature Range T_J -40°C to 125°C
 Thermal Resistance
 θ_{JA} (5 Pin SOT23) 134.5°C/W
 θ_{JC} (5 Pin SOT23) 81°C/W

ELECTRICAL SPECIFICATIONS

Specifications are for an Ambient Temperature of $T_A = 25^\circ\text{C}$ only; limits applying over the full Operating Temperature range are denoted by a “•”. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_A = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise indicated, $V_{IN} = 3.6V$, $T_A = 25^\circ\text{C}$.

Parameter	Min.	Typ.	Max.	Units	Conditions
Input Voltage Range	2.5		5.5	V	
Feedback Current			±100	nA	
Regulated Feedback Voltage	0.588	0.600	0.612	V	
Output Voltage Accuracy	-3		+3	%	$I_{OUT}=100\text{mA}$, $V_{IN} = 2.5V$ to $3.0V$
Output Voltage Accuracy	-3		+3	%	• $I_{OUT}=100\text{mA}$, $V_{IN} = 3.0V$ to $5.5V$
Reference Voltage Line Regulation			0.4	%/V	$V_{IN} = 2.5V$ to $3.0V$
Reference Voltage Line Regulation			0.4	%/V	• $V_{IN} = 3.0V$ to $5.5V$
Output Voltage Line Regulation			0.4	%/V	$V_{IN} = 2.5V$ to $3.0V$
Output Voltage Line Regulation			0.4	%/V	• $V_{IN} = 3.0V$ to $5.5V$
Peak Inductor Current	1.5	2.3		A	$V_{FB} = 0.5V$ or $V_{OUT} = 90\%$
PWM Quiescent Current (Note 2)		188		µA	$V_{FB} = 0.5V$ or $V_{OUT} = 90\%$
PFM Quiescent Current		15		µA	$V_{FB} = 0.65V$ or $V_{OUT} = 108\%$
Shutdown		0.1	1	µA	$V_{RUN} = 0V$, $V_{IN} = 4.2V$
Oscillator Frequency	1.2	1.5	1.8	MHz	• $V_{FB} = 0.6V$ or $V_{OUT} = 100\%$
Short-Circuit Oscillator Frequency		900		kHz	• $V_{FB} = 0V$ or $V_{OUT} = 0V$
$R_{DS(ON)}$ of PMOS		0.24		Ω	$I_{SW} = 100\text{mA}$
$R_{DS(ON)}$ of NMOS		0.21		Ω	$I_{SW} = -100\text{mA}$
Under Voltage Lock Out		1.8		V	
SW Leakage			±1	µA	$V_{RUN} = 0V$, $V_{SW} = 0V$ or $5V$, $V_{IN} = 5V$
Enable Threshold			1.2	V	•
Shutdown Threshold	0.4			V	•
EN Leakage Current			±1	µA	•

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D : ($T_J = T_A + (P_D * \theta_{JA})$)
 Note 2: Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.
 Note 3: This IC is built-in over-temperature protection to avoid damage from overload conditions.
 Note 4: θ_{JA} is measured in the natural convection at $T_A=25^\circ\text{C}$ on a high effective thermal conductivity test board (2 layers, 2S0P) of JEDEC 51-5 thermal measurement standard.
 Note 5: θ_{JC} represents the resistance to the heat flows the chip to package top case.

BLOCK DIAGRAM

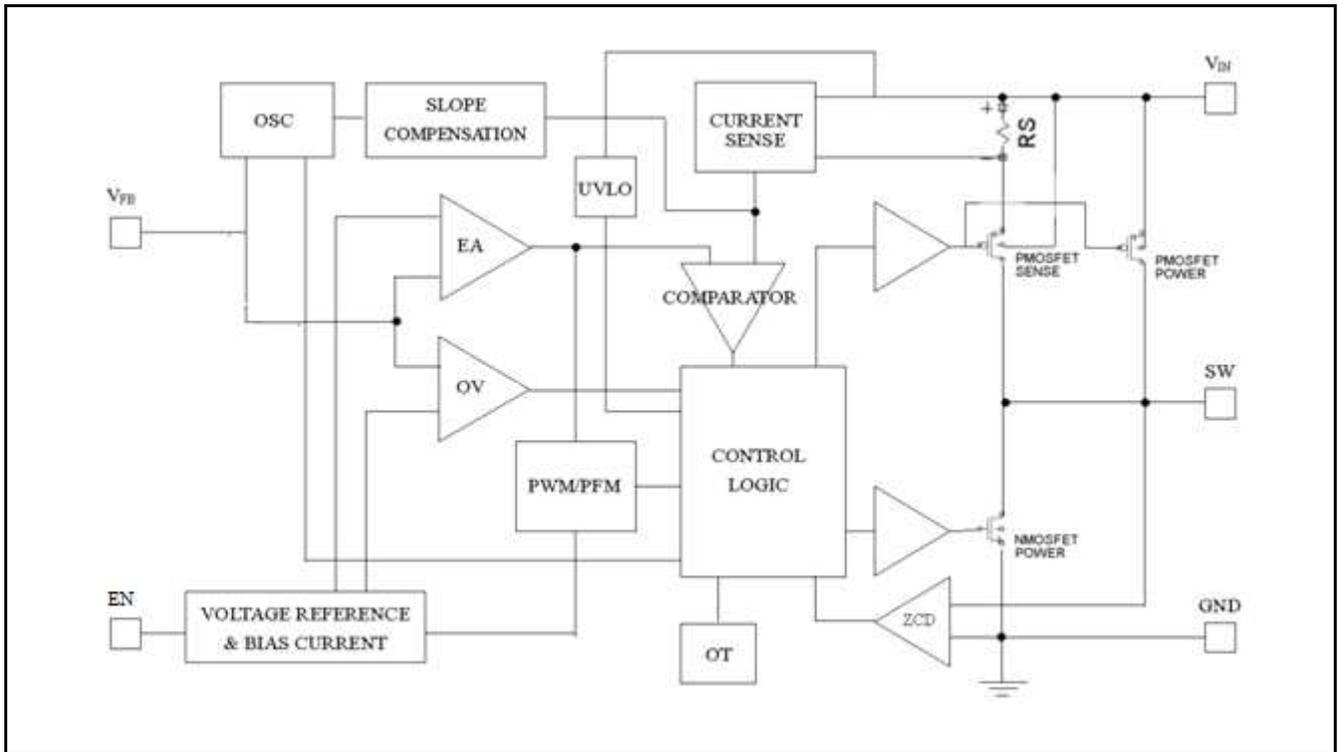


Fig. 2: XRP6658 Block Diagram

PIN ASSIGNMENT

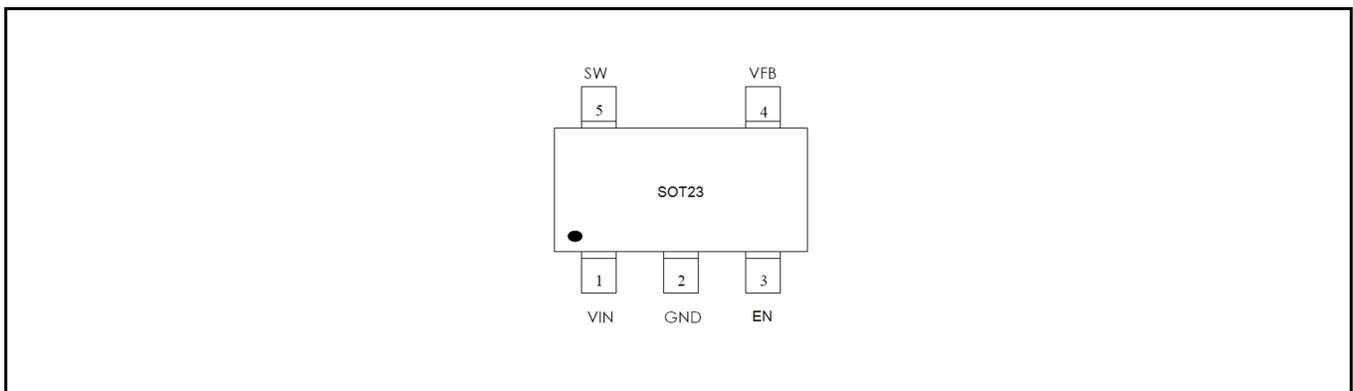


Fig. 3: XRP6658 Pin Assignment

PIN DESCRIPTION

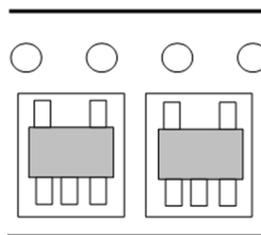
Name	Pin Number	Description
VIN	1	Power Input Pin. Must be closely decoupled to GND pin with a 4.7μF or greater ceramic capacitor.
GND	2	Ground Signal
EN	3	Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shutdown the device.
VFB	4	Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.
SW	5	Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
XRP6658ISTR-F	-40°C ≤ T _j ≤ +125°C	HCWW	5-Pin SOT23	3K/Tape & Reel	RoHS Compliant Halogen Free	
XRP6658EVB	XRP6658 Evaluation Board					

“WW” = Work Week

Note that the XRP6658 series is packaged in Tape and Reel with a reverse part orientation as per the following diagram



TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at $V_{IN} = 3.6V$, $T_J = T_A = 25^\circ C$, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

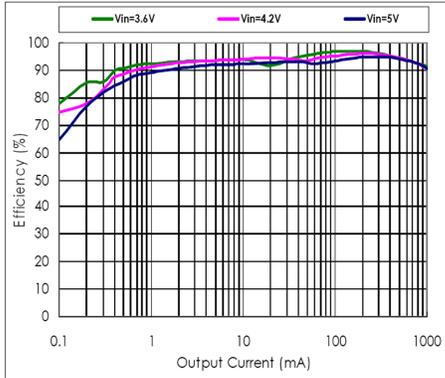


Fig. 4: Efficiency vs Output Current ($V_{OUT}=3.3V$)

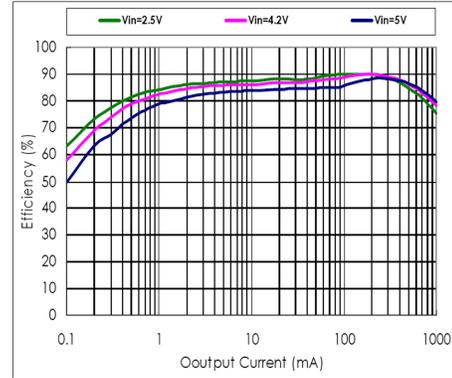


Fig. 5: Efficiency vs Output Current ($V_{OUT}=1.2V$)

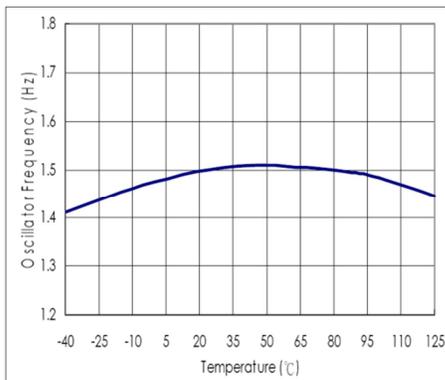


Fig. 6: Oscillator Frequency vs Temperature

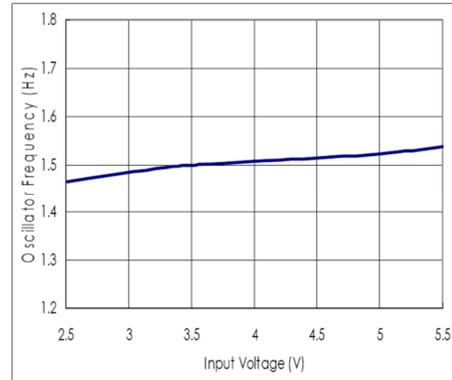


Fig. 7: Oscillator Frequency vs Supply Voltage

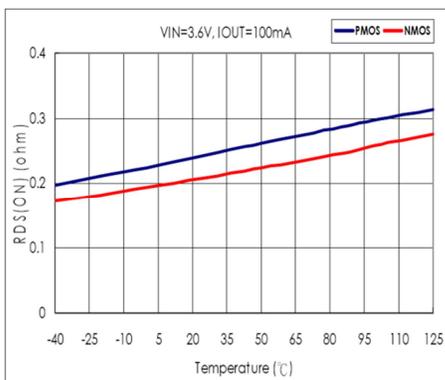


Fig. 8: $R_{DS(ON)}$ vs Temperature

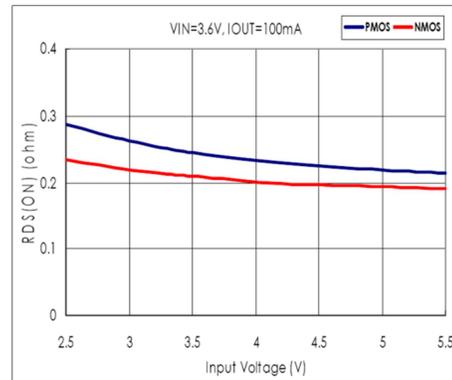


Fig. 9: $R_{DS(ON)}$ vs Input Voltage

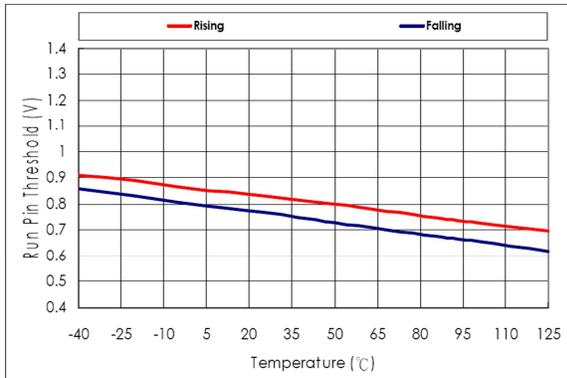


Fig. 10: EN Pin Threshold vs Temperature

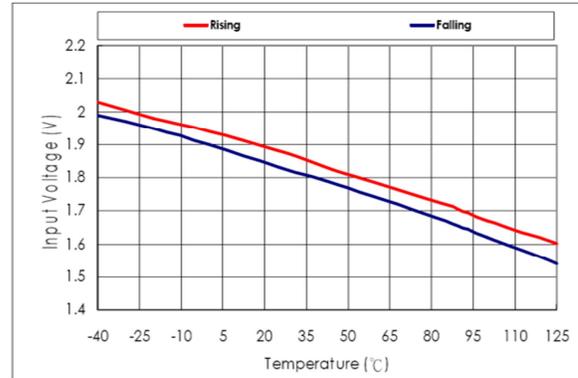


Fig. 11: UVLO Threshold vs Temperature

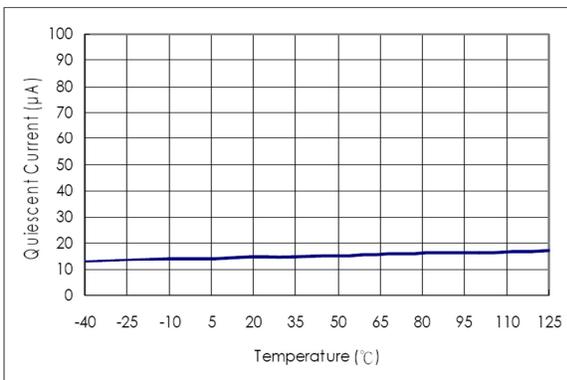


Fig. 12: Quiescent Current vs Temperature (PFM Mode)

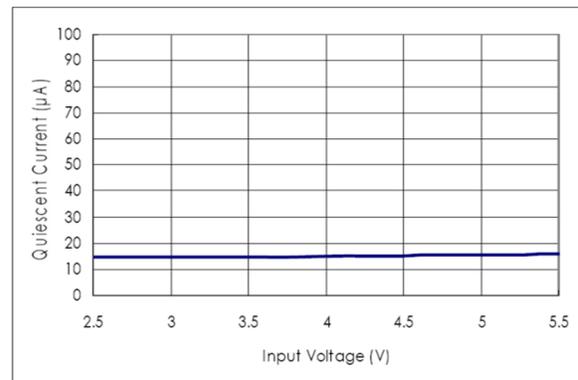


Fig. 13: Quiescent Current vs Input Voltage (PFM Mode)

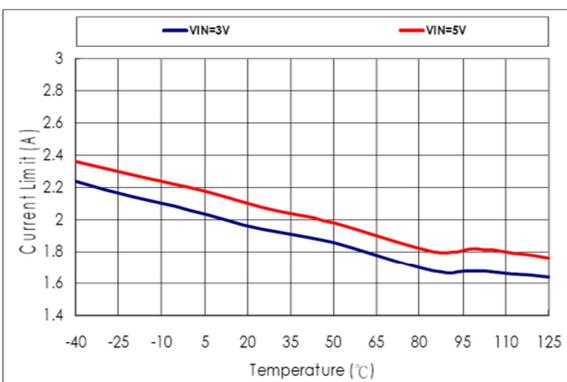


Fig. 14: Current Limit vs Temperature ($V_{OUT}=1.2V$)

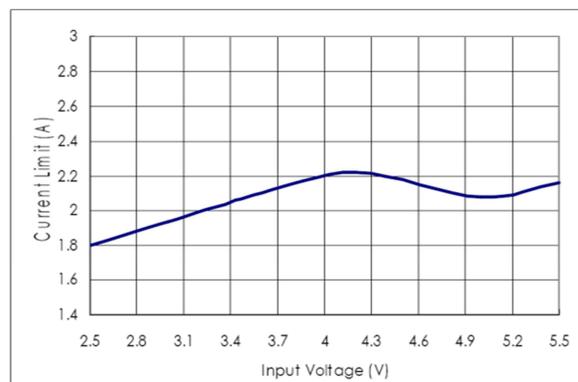


Fig. 15: Current Limit vs Input Voltage ($V_{OUT}=1.2V$)

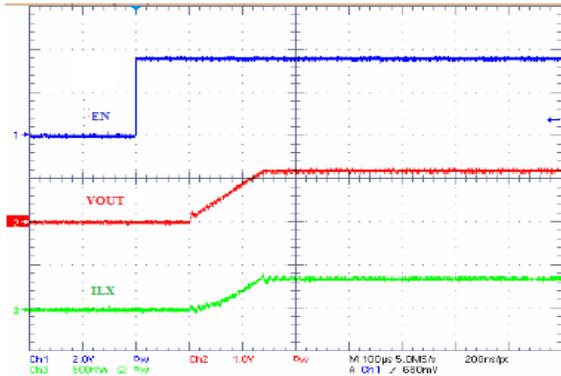


Fig. 16: Power On From EN Pin ($I_{OUT}=1A$)

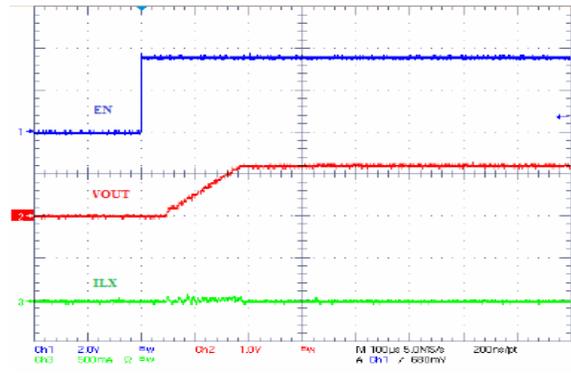


Fig. 17: Power On From EN Pin ($I_{OUT}=10mA$)

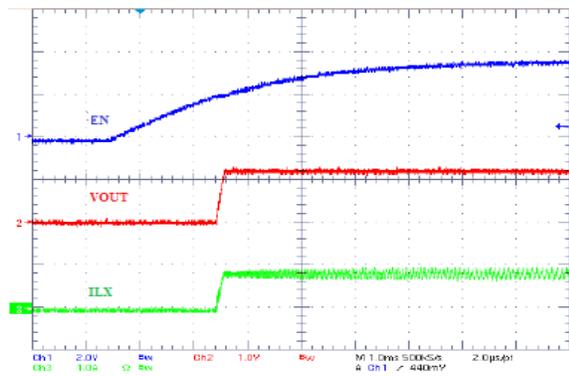


Fig. 18: Power On From V_{IN} ($I_{OUT}=1A$)

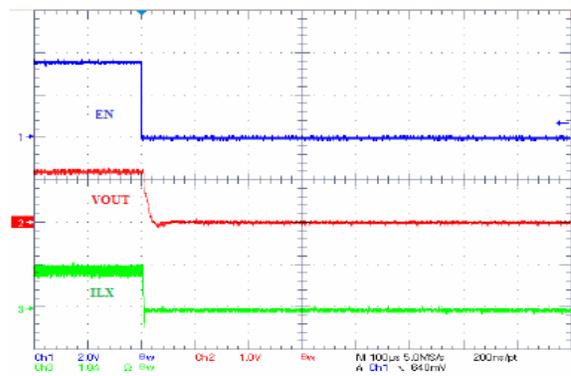


Fig. 19: Power Off From EN ($I_{OUT}=1A$)

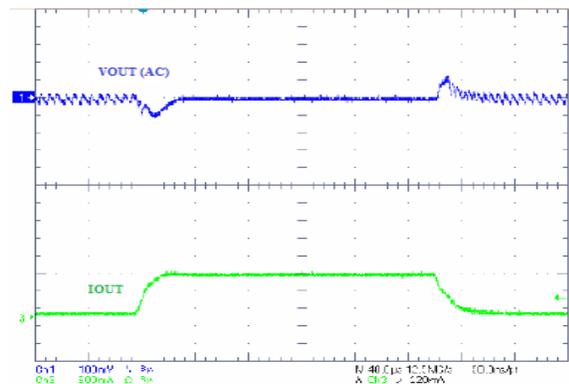


Fig. 20: Load Step Response
 $V_{OUT}=1.2V$, I_{OUT} From 50mA to 500mA

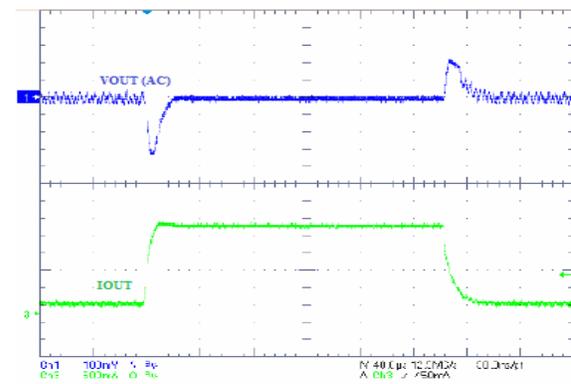


Fig. 21: Load Step Response
 $V_{OUT}=1.2V$, I_{OUT} From 50mA to 1A

THEORY OF OPERATION

The typical application circuit of adjustable version is shown in figure 22.

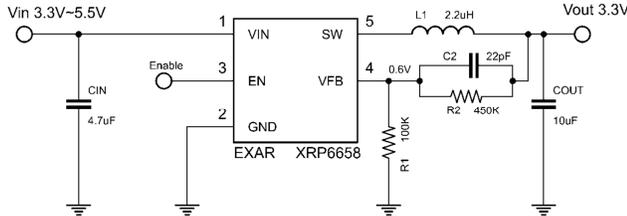


Fig. 22: Typical Application

INDUCTOR SELECTION

Inductor ripple current and saturation current rating are two factors to be considered when selecting the inductor value. A low DCR inductor is preferred.

The inductor value L can be calculated from the following equation:

$$L = (V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right) \times \left(\frac{1}{\Delta IL}\right)$$

C_{IN} AND C_{OUT} SELECTION

A low ESR input capacitor can minimize the input voltage ripple. Voltage rating of the capacitor should be at least 50% higher than the input voltage. The RMS current of the input capacitor is required to be larger than the I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}}$$

The ESR value is an important parameter to consider when selecting an output capacitor C_{OUT}. The output ripple V_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \times f \times C_{OUT}} \right)$$

The output capacitor's value can be optimized for very low output voltage ripple and small circuit size. Voltage rating of the capacitor should be at least 50% higher than the output voltage. Higher values, lower cost ceramic capacitors are now available in smaller sizes. These ceramic capacitors have high ripple currents, high voltage ratings and low ESR that make them ideal for switching regulator applications.

It is recommended to use X5R or X7R ceramic capacitors as they have the best temperature and voltage characteristics.

OUTPUT VOLTAGE SELECTION

The output voltage is adjustable via the external resistor network R1 and R2 as per the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1} \right)$$

where, V_{REF} is the reference voltage at 0.6V.

The feedback resistors must be chosen such that power dissipation of the network is minimal. R1 must be selected within the range of 80kΩ ≤ R1 ≤ 120kΩ. R2 is selected based on the above equation.

THERMAL CONSIDERATIONS

Although thermal shutdown is built-in in XRP6658 to protect the device from thermal damage, the total power dissipation that XRP6658 can sustain is based on the package thermal capability. The formula to ensure safe operation is shown in Note 1. To avoid XRP6658 from exceeding the maximum junction temperature, some thermal analysis is required.

GUIDELINES FOR PCB LAYOUT

To ensure proper operation of the XRP6658, please note the following PCB layout guidelines:

1. The GND, SW and VIN traces should be kept short, direct and wide.
2. VFB pin must be connected directly to the feedback resistors. Resistive divider R1/R2 must be connected in parallel to the output capacitor C_{OUT}.
3. The input capacitor C_{IN} must be as close as possible to pin VIN.
4. Keep SW node away from the sensitive VFB node since SW signal experiences high frequency voltage swings.

TYPICAL APPLICATIONS

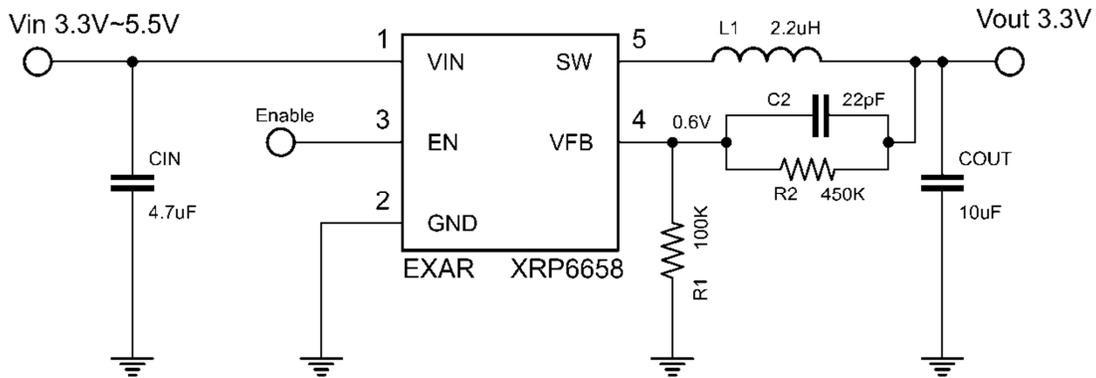


Fig. 23: 3.3V/5.5V to 3.3V Conversion

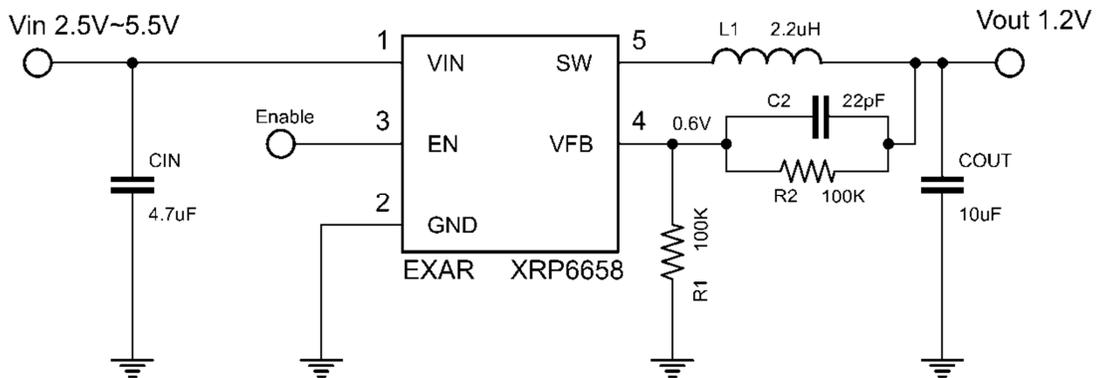
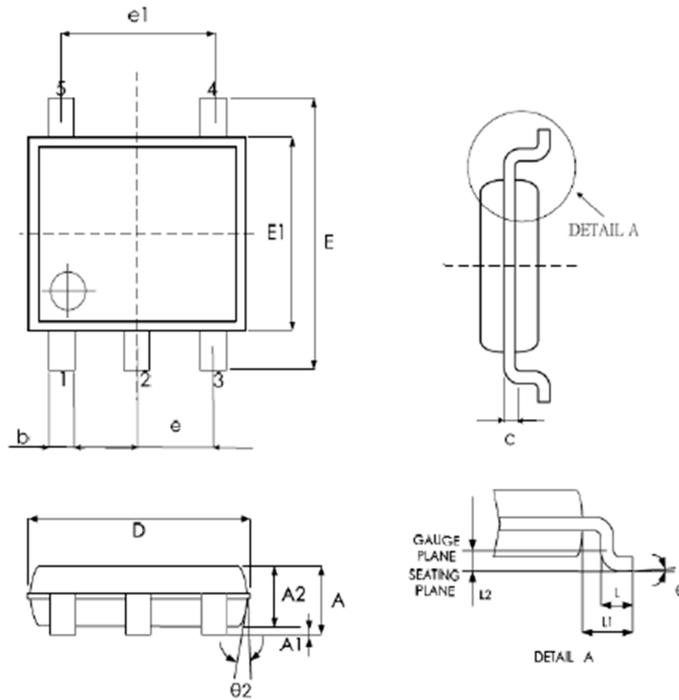


Fig. 24: 2.5V/5.5V to 1.2V Conversion

PACKAGE SPECIFICATION

5-PIN SOT23



SYMBPLS	MIN.	NOM.	MAX.
A	1.05	1.20	1.35
A1	0.05	0.10	0.15
A2	1.00	1.10	1.20
b	0.30	—	0.50
C	0.08	—	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.55
L1	0.60 REF		
θ°	0	5	10
$\theta2^\circ$	6	8	10

UNIT: MM

REVISION HISTORY

Revision	Date	Description
1.0.0	09/16/2010	Initial release of datasheet
1.1.0	09/30/2010	Corrected pin-out on schematics Figures 1, 23 and 24
1.2.0	11/15/2010	Corrected ΔV_{OUT} equation: changed V_{OUT} to C_{OUT} . Updated 'Output Voltage selection' section.
1.3.0	01/14/2011	Added specific test conditions and data in Electrical Specification Table for output voltage accuracy, reference voltage Line regulation and output voltage line regulation for operations below 3V.
1.4.0	07/19/2011	Corrected typographical errors on package specification table parameters "b" and "e"
1.5.0	0/15/2011	Added a range for the selection of lower feedback resistor.
1.6.0	1/13/2014	Added "Junction Temperature Range T_J-40°C to 125°C" to operating ratings; In "Ordering Information" changed the temperature range to " $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ " [ECN: 1403-04]

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