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XRP7713EVB-DEMO-1

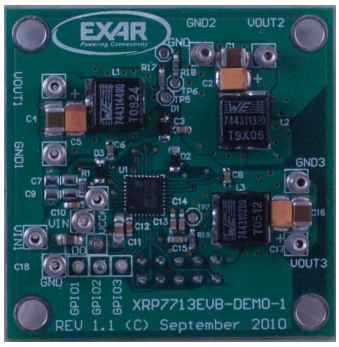
Three Channel Digital PWM Demo Board

April 2011 Rev. 1.0.0

EVALUATION BOARD MANUAL

GENERAL DESCRIPTION

The XRP7713EVB-DEMO-1 Demo board is a complete, working, 3 channel, power system measuring 1.75" x 1.75" capable of producing over 30 watts. It is optimized to provide 3.3V, 2.5V and 1V at a maximum of 5 amps per channel. However, using the PowerArchitect™ Configuration and Design software one can program the outputs as desired. An interface board, the Exar Communication Module (XRP77xxEVB-XCM) plugs directly in and provides an interface between your PC and the I^2C interface of the XRP7713. The order and ramp rates for each supply can be programmed to accommodate any sequencing requirement. All power supply operations can be controlled over an I^2C interface. Faults, output voltages and currents can also be monitored. Four GPIO signals are available and can be programmed to provide status of power good signals enables and faults. Unused GPIO pins can be programmed as I/O expansion for a microcontroller.



FEATURES

- **XRP7713 Programmable Controller**
- **3 Channel Power System**
- **Wide Input Voltage Range: 4.5V-25V**
- **Over 30W Capable**
- **Small Form Factor: 1.75" x 1.75"**
- **I^2C Interface**
  - Programming
  - Monitoring
  - Control

EVALUATION BOARD

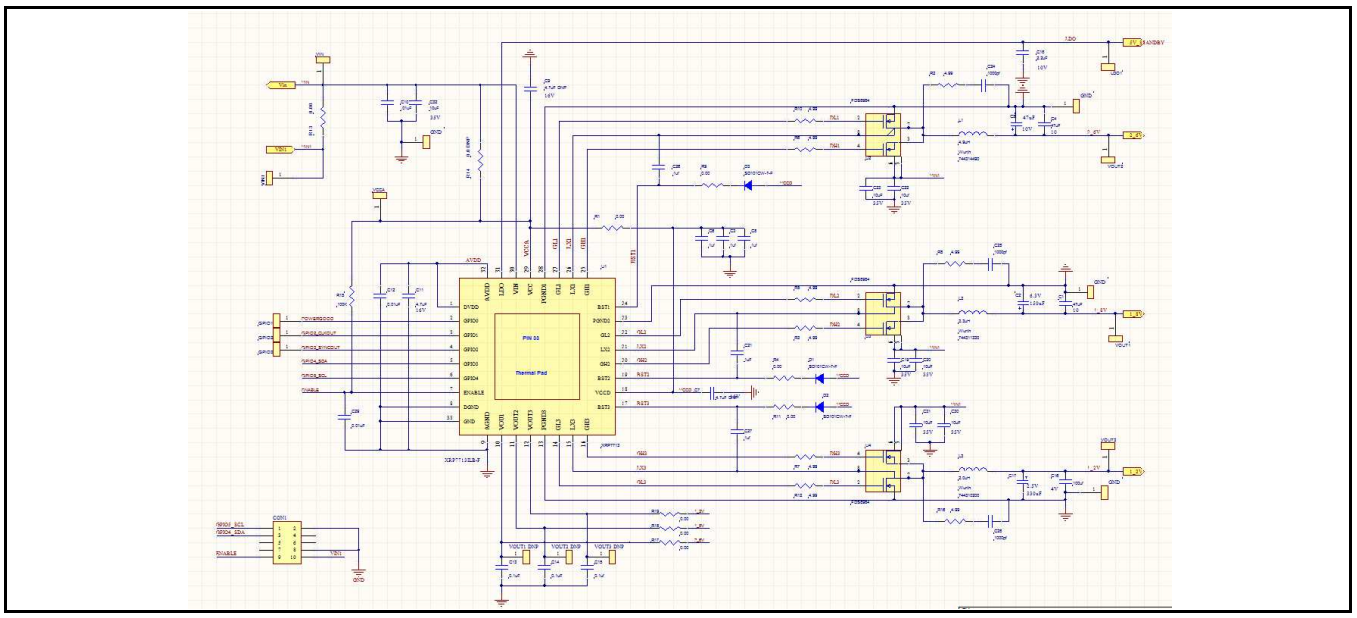


Fig. 1: XRP7713EVB-DEMO-1 Schematic

PIN ASSIGNMENT

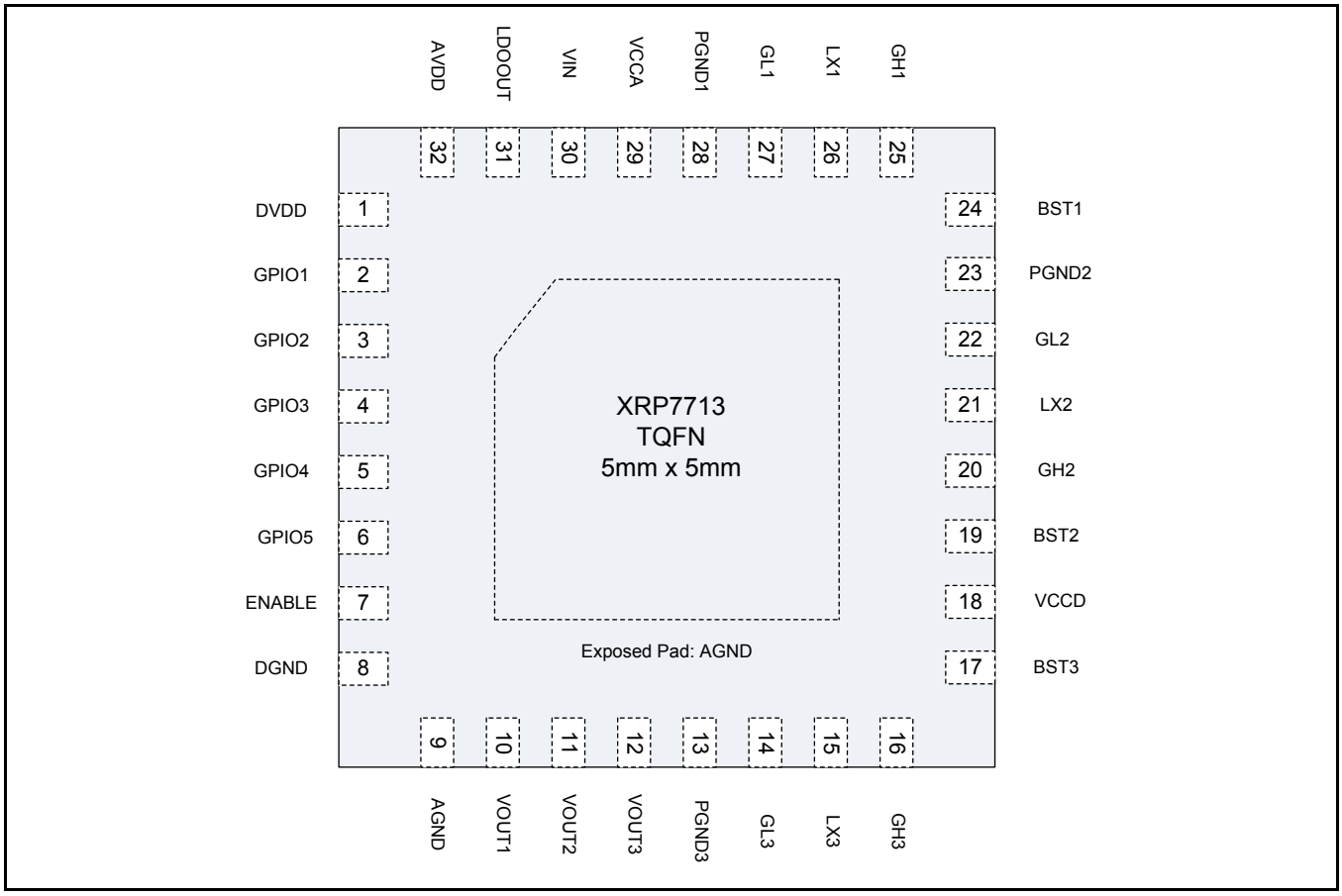


Fig. 2: XRP7713 Pin Assignment

PIN DESCRIPTION

QFN PIN #	PIN NAME	DESCRIPTION
30	*VIN*	Power source for the internal linear regulators to generate VCCA, AVDD and the Standby LDO (LDOOUT). Place a decoupling capacitor close to the controller IC. Also used in UVLO fault generation – if VIN falls below the user programmed limit, all channels are shut down.
29	*VCCA*	Output of the internal 5V LDO. This voltage is internally used to power analog blocks. Note that a compensation capacitor should be used on this pin [see Application Note].
18	*VCCD*	Gate Drive input voltage. This is not an output voltage. This pin can be connected to VCCA to provide power for the Gate Drive. VCCD should be connected to VCCA with the shortest possible trace and decouple with a minimum 1uF capacitor. Alternatively, VCCD could be connected to an external supply (not greater than 5V).
28, 23,13	*PGND1-PGND3*	Power Ground. Ground connection for the low side gate driver.
32	*AVDD*	Output of the internal 1.8V LDO. A decoupling capacitor should be placed between AVDD and AGND close to the chip (with short traces).
1	*DVDD*	Input for powering the internal digital logic. This pin should be connected to AVDD.

QFN PIN #	PIN NAME	DESCRIPTION
8	*DGND*	Digital Ground. This pin should be connected to the ground plane at the exposed pad with a separate trace.
9	*AGND*	Analog Ground. This pin should be connected to the ground plane at the exposed pad with a separate trace.
27, 22, 14	*GL1-GL3*	Output pin of the low side gate driver. Connect directly to the respective gate of an external N-channel MOSFET.
25, 20, 16	*GH1-GH3*	Output pin of the high side gate driver. Connect directly to the respective gate of an external N-channel MOSFET.
26, 21, 15	*LX1-LX3*	Lower supply rail for the high-side gate driver (GHx). Connect this pin to the switching node at the junction between the two external power MOSFETs and the inductor. These pins are also used to measure voltage drop across bottom MOSFETs in order to provide output current information to the control engine.
24, 19, 17	*BST1-BST3*	High side driver supply pin(s). Connect BST to an external boost diode and a capacitor as shown in the front page diagram. The high side driver is connected between the BST pin and LX pin.
2,3,4	GPIO1-GPIO3	These pins can be configured as inputs or outputs to implement custom flags, power good signals and enable/disable controls. A GPIO pin can also be programmed as an input clock synchronizing IC to external clock. Refer to the "GPIO Pins" Section and the "External Clock Synchronization" Section for more information.
5,6	GPIO4_SDA, GPIO5_SCL	I^2C serial interface communication pins. These pins can be re-programmed to perform GPIO functions in applications when I^2C bus is not used.
10, 11, 12	VOUT1-VOUT3	Voltage sense. Connect to the output of the corresponding power stage.
31	LDOOUT	Output of the Standby LDO. It can be configured as a 5V or 3.3V output. A compensation capacitor should be used on this pin [see Application Note].
7	ENABLE	If ENABLE is pulled high, the chip powers up (logic reset, registers configuration loaded, etc.). If pulled low for longer than 100us, the XRP7714 is placed into shutdown.
Exposed PAD	AGND	Analog Ground. Connect to analog ground (as noted above for Pin 9).

ORDERING INFORMATION

Refer to XRP7713's datasheet and/or www.exar.com for exact and up to date ordering information.

USING THE EVALUATION BOARD

INPUT VOLTAGE CONFIGURATION

The XRP7713EVB-DEMO-1 Board has several different input voltage options. The Input voltage components are rated at 35V. The power components have been optimized for a 12V input rail. When running the board at an input voltage other than 12V, use PowerArchitect™ to evaluate the system performance.

Single Wide Range, Input Voltage Rail

As shipped from the factory, the demo board is configured for single input voltage operation. The Input requirements are from 5.5V to 25V input.

Single 5V Voltage Rail

Installing a zero ohm resistor into position R14 connects VIN to VCCA. This allows operation down to 4.5V, but restricts the maximum input voltage to 5.5V.

Dual Voltage Rail Operation

The XRP7713EVB-DEMO1 board can be configured to operate from two separate rails.

The following modifications must be made:

- Remove 0 ohm resistor R13
- Connect power for the XRP7713 between pins VIN1 and GND
- Connect channel power between pins VIN and GND

Channel Design and Limitations

Channel 1 is designed to provide an output voltage from 3.3V to 5.0V. The default voltage is 3.3V.

Channel 2 is designed to provide an output voltage from 1.8V to 2.5V. The default voltage is 2.5V.

Channel 3 is designed to provide an output voltage from .9 to 1.2V. The default voltage is 1.0V. The Tantalum output capacitor is has a 4V rating. If modifying the channel 3 design, do not exceed four volts unless the cap is replaced.

I^2C INTERFACE

The XRP77XX family of controllers employs a standard I2C interface. Pull-ups for the I2C signals are not included on the demo board. If using the demo board with something other than the XRP77xxEVB-XCM, verify that the SDA and SCL lines are pulled up.

ENABLE PIN

The ENABLE pin connects to an RC network that delays turn on of the device. It is pulled up to AVDD with a 100K resistor and to ground through a .01uF capacitor. It appears on pin 9 of connector CON1. This pin can be used to turn on or turn off the device.

Operating the Evaluation Board

Make sure that the board is configured for the power supply(s) that you are using. Refer to the Input Voltage Configuration section if you require specific board modifications for your application.

Apply Power to the board: Please refer to Figure 3 for board connections.

If using a single supply, Connect the input supply between the VIN1 pin and the GND pin. If using a dual supply, Connect the chip power between VIN1 and GND, and connect Power Vin between the VIN pin and GND.

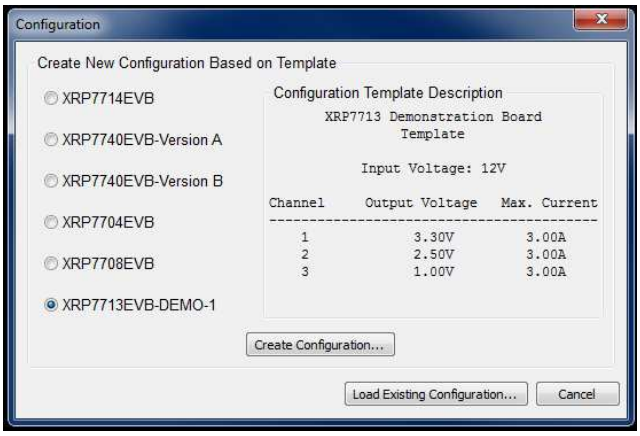
Plug the PowerXR evaluation board on to the XCM as shown below.

Insert the USB cable into the computer and the XCM board.

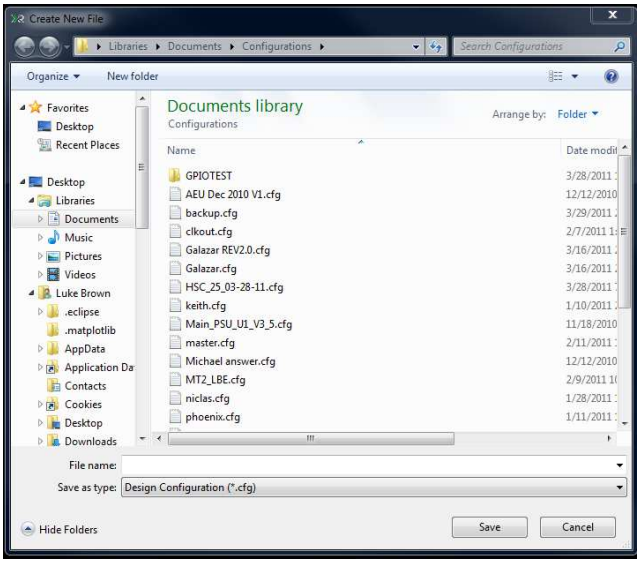
Turn on the Power supply

Load the PowerArchitect™ software.

Select the XRP7713EVB configuration and select create configuration..



You will be prompted for a filename by a Create New File Dialog box. Navigate to a location to save the configuration, enter a filename and select Save.



Refer to the Exar PowerArchitectTM Quick Start Guide for information on how to run the software.

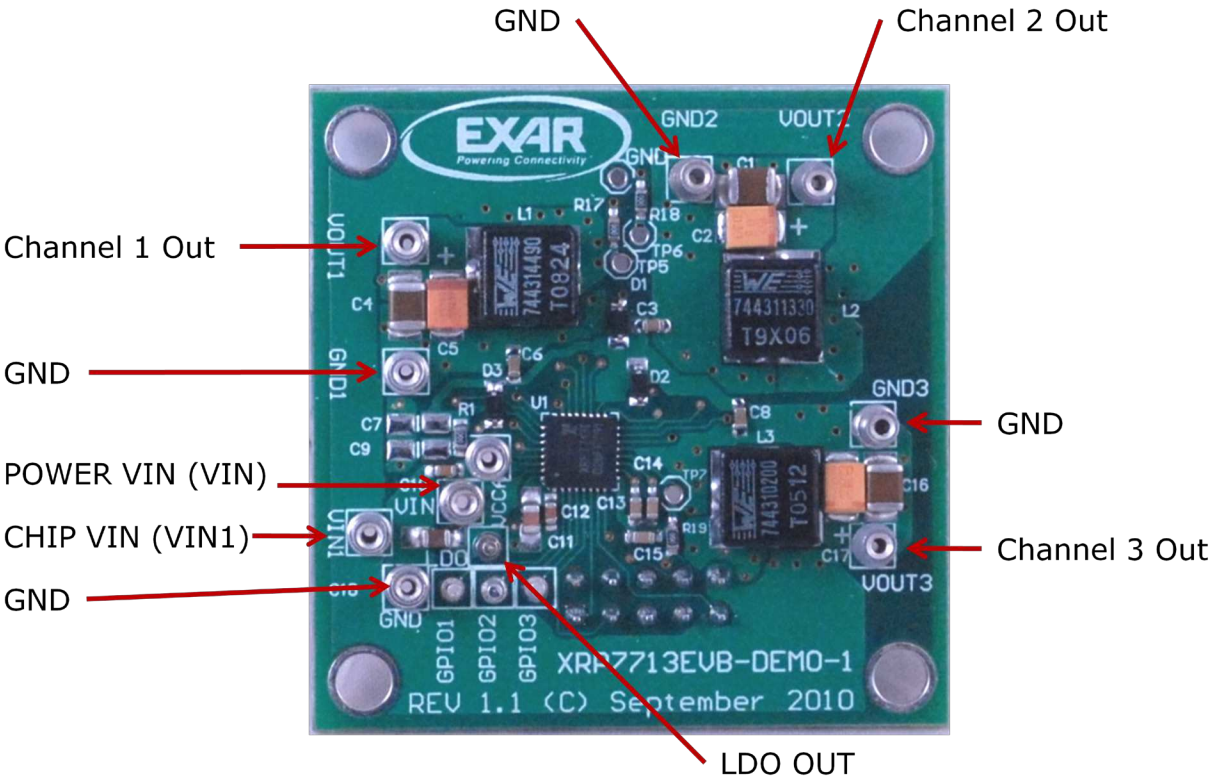
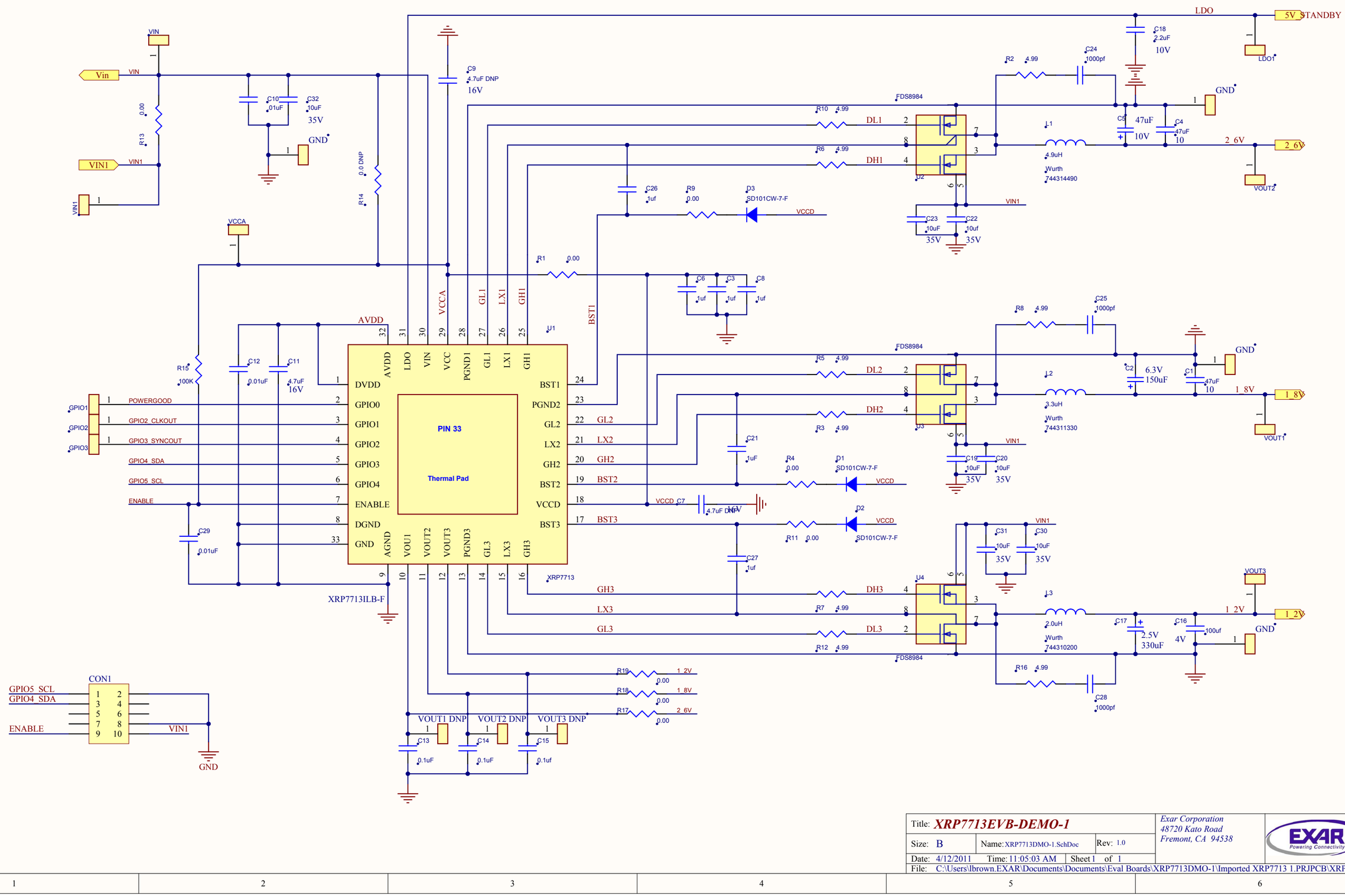


Figure 3: Board Connections



Title: ***XRP7713EVB-DEMO-1***			*Exar Corporation* *48720 Kato Road* *Fremont, CA 94538*
Size: B	Name: XRP7713DMO-1.SchDoc	Rev: 1.0	
Date: 4/12/2011	Time: 11:05:03 AM	Sheet 1 of 1	
File: C:\Users\lbrown.EXAR\Documents\Documents\Eval Boards\XRP7713DMO-1\Imported XRP7713 1.PRJPCB\XRP7713DMO-1.Sc			

BILL OF MATERIAL

Ref.	Qty	Manufacturer	Part Number	Size	Component
C1, C4	2	Murata	GRM32ER71A476KE15L	1210	Cap, Ceramic 47uF 16V X7R 1210
C2	1	AVX	T520B157M006ATE070	1210	Cap, Tantalum 150uF 10V LOW_ESR, CASE A
C3, C6, C8, C21, C26, C27	6	MURATA	GRM21BR71H105KA12L	0603	Cap, Ceramic 1uF 10V X7R 0603
C5	1	AVX	TCJB476M010R0070	1210	Cap, Tantalum 47uF 10V LOW_ESR, CASE A
C7, C9	2	Murata	GRM21BR71C475KA73	0805	Cap, Ceramic 4.7uF 10V X7R 0805
C10	1	Murata	GRM188R71H103KA01D	0603	Cap, Ceramic .01uF 50V X7R 0603
C11	1	Murata	GRM21BR71C475KA73	0805	Cap, Ceramic 4.7uF 10V X7R 0805
C12, C29	2	Murata	GRM188R71H103KA01D	0603	Cap, Ceramic .01uF 50V X7R 0603
C13, C14, C15	3	Murata	GRM21BR71H104KA01L	0603	Cap, Ceramic .1uF 50V X7R 0603
C16	1	Murata	GRM32EE70G107ME19L	1210	Cap, Ceramic 100uF 4V X7U 1210
C17	1	AVX	T520B337M2R5ATE045	1210	Cap, Tantalum 330uF 4V LOW_ESR, CASE A
C18	1	Murata	GRM21BR71A225KA01L	0805	Cap, Ceramic 2.2uF 10V X7R 0805
C19, C20, C22, C23, C30, C31, C32	7	Murata	GRM32ER6YA106KA12L	1210	Cap, Ceramic 10uF 35V X7R 0805, Cap, Ceramic 10uF 35V X7R 1210
C24, C25, C28	3	Murata	GRM188R71H102KA01D	0603	Cap, Ceramic 1000pF 50V X7R 0603
CON1	1	Wurth	613 010 218 21	HDR2X5F	CONN Header 5x2, 0.1 inch
D1, D2, D3	3	Diodes Inc	SD101CW-7-F	SOD123	Diode, Schottky, 40V 400mW SOD-1123
L1	1	Wurth	744314490	744314490	WURTH 744314490
L2	1	Wurth	744311330	744314490	WURTH 744314490
L3	1	Wurth	744310200	744314490	WURTH 744310200
R1, R4, R9, R11, R17, R18, R19	7	Vishay/Dale	CRCW02010000Z0ED	0603	Resistor, 0.00 .1W 0603
R2, R3, R5, R6, R7, R8, R10, R12, R16	9	Vishay/Dale	CRCW06034R99FKEA	0603	Resistor, 4.99 .1W 0603, Resistor, 4.99.1W 0603
R13	1	Vishay/Dale	CRCW12060000Z0EA	1206	Resistor 0.00 .25W 1206
R14	1	Vishay/Dale	CRCW02010000Z0ED	0603	Resistor, 0.00 .1W 0603
R15	1	Vishay/Dale	CRCW0603100KFKEA	0603	Resistor, .100K 1W 0603
U1	1	Exar Corporation	XRP7713ILB-F	QFN32_5X5	3 Channel 25 V PWM Step Down DC-DC Controller QFN-32
U2, U3, U4	3	Fairchild	FDS8984	SOIC - 8	MOSFET, N-Channel 7A SOIC-8
GPIO1, GPIO2, GPIO3, LDO	4	Keystone	1528-2	Keystone 1528-2	Test Point
TP1, TP2, TP3, TP4	4	Keystone	1562-2	Keystone 1562-2	Test Point
VCCA, VIN, VIN1, VOUT1, VOUT2, VOUT3	6	Keystone	1562-2	Keystone 1562-2	Test Point

EVALUATION BOARD LAYOUT

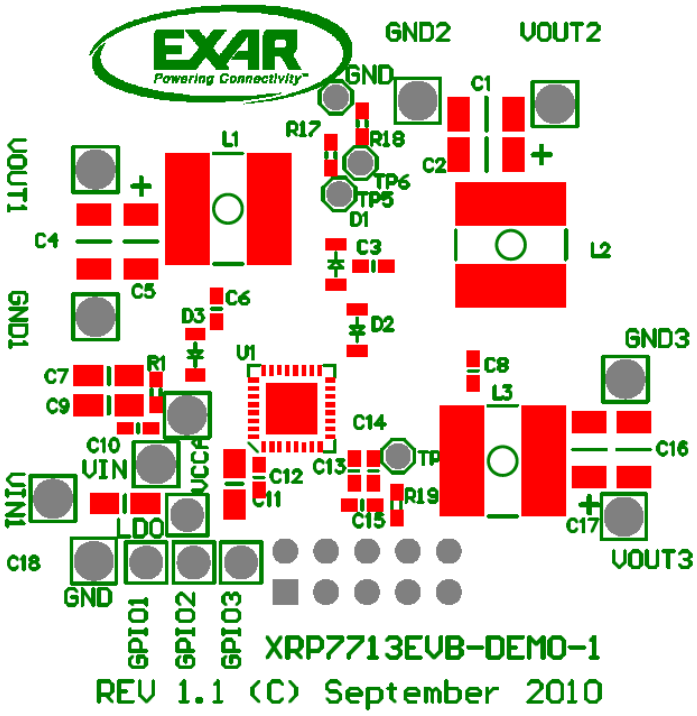


Fig. 3: Component Placement – Top Side

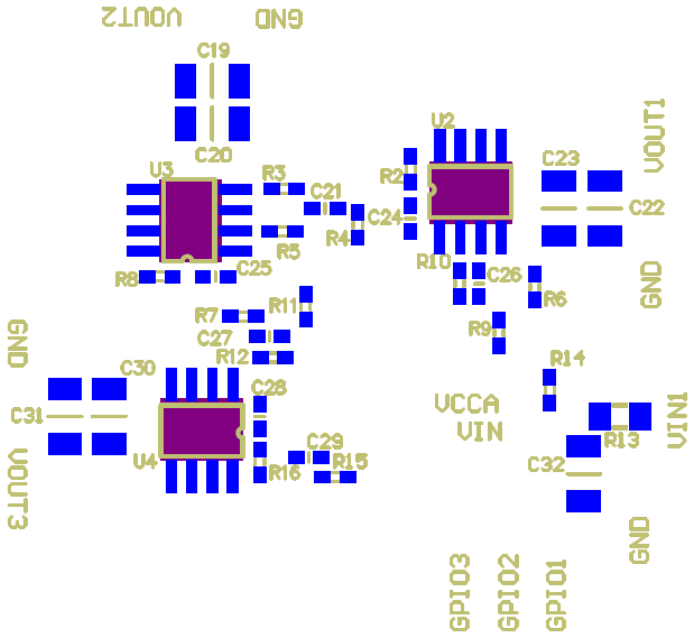


Fig. 4: Component Placement – Bottom Side

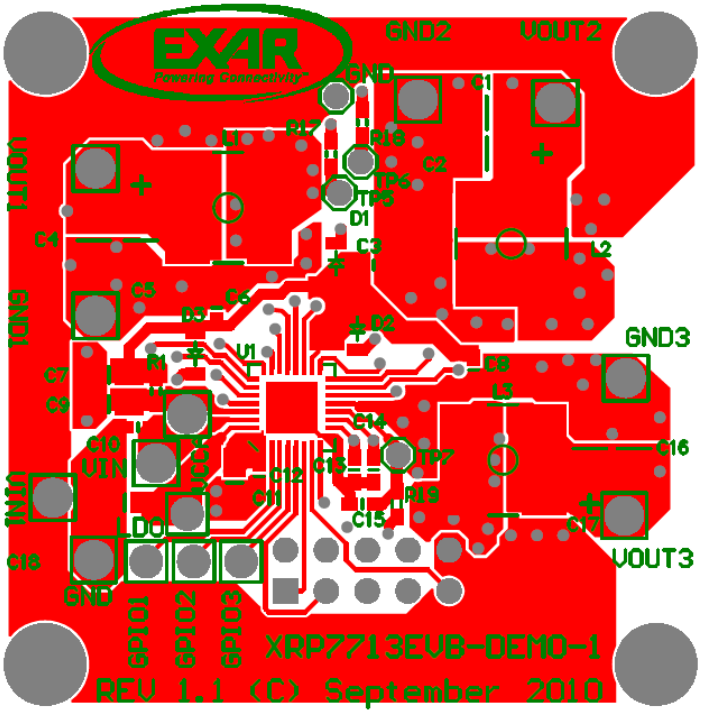


Fig. 5: Layout – Top Side

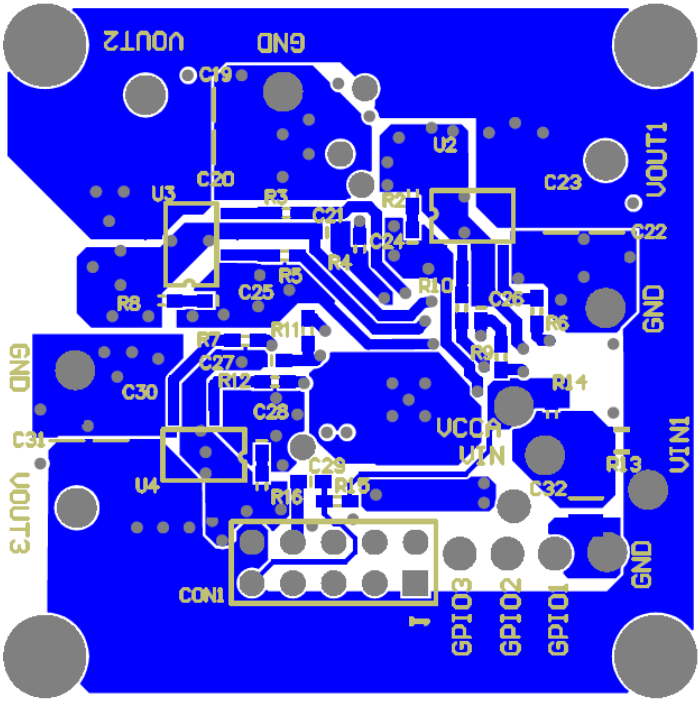


Fig. 6: Layout - Bottom

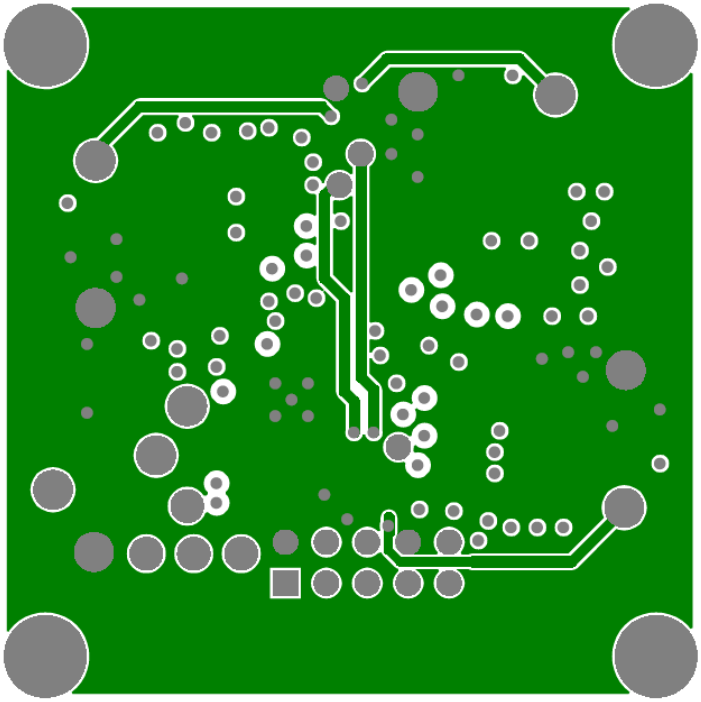


Fig. 7: Layout – Internal Plane

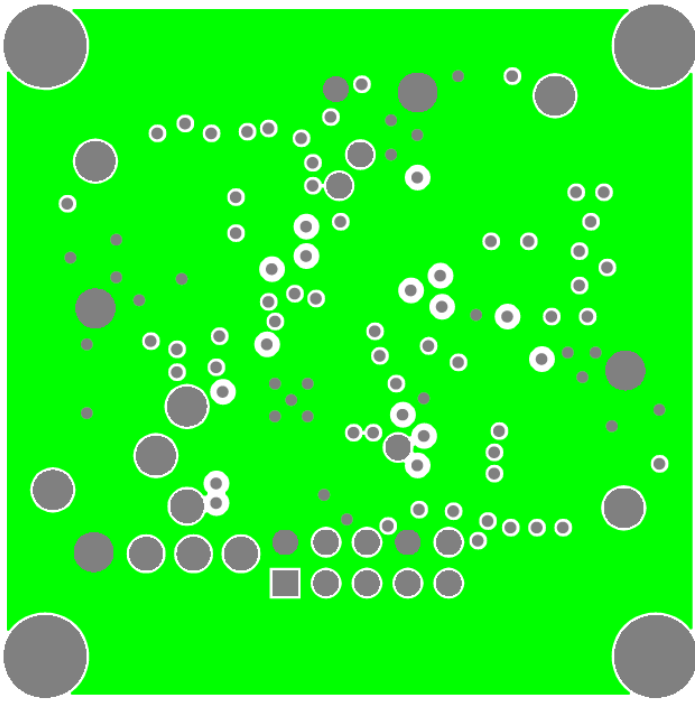


Fig. 8: Layout – Internal Plane

EVALUATION BOARD PERFORMANCE (EFFICIENCY)

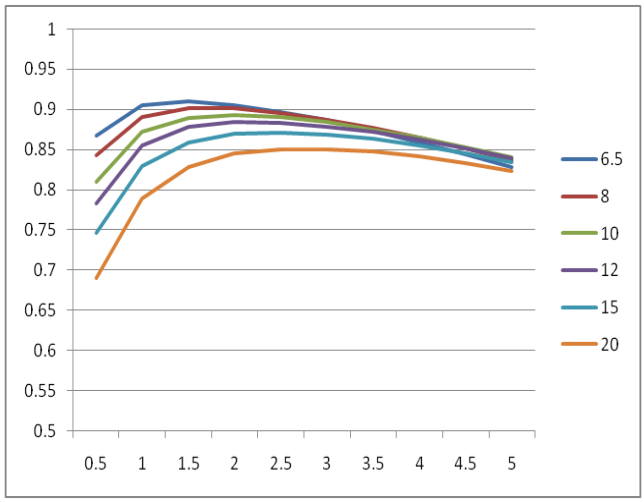


Fig. 9: All Channels Combined Efficiency

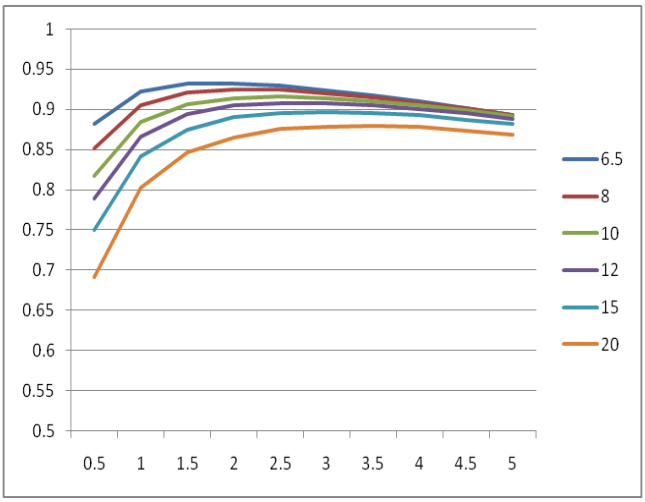


Fig. 10: Channel 1, 3.3V Efficiency

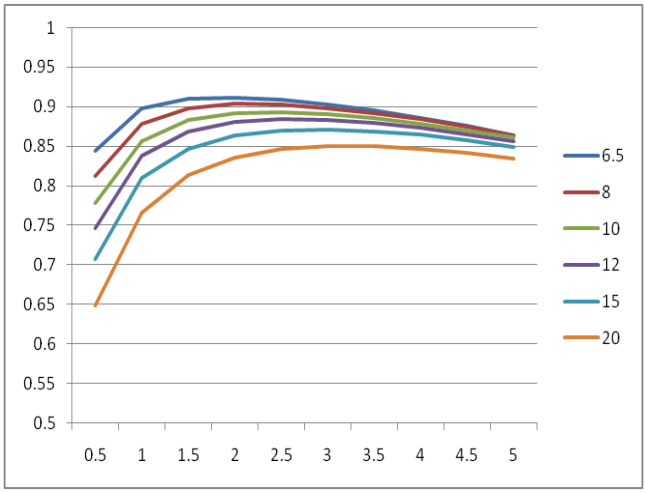


Fig. Channel 11: 2.5V Efficiency

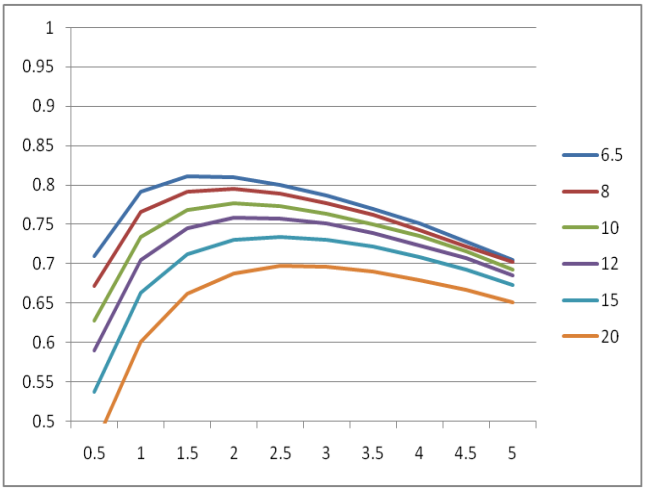


Fig. 12: Channel 3, 1V Efficiency

Fig. 13: 5V All Channels Combined Efficiency

Fig. 14: 5V Individual Channel Efficiencies

EVALUATION BOARD PERFORMANCE (LINE LOAD REGULATION)

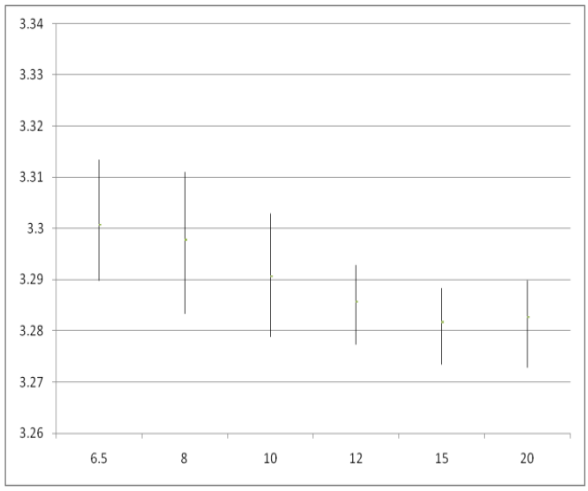


Fig. 15: Line Load Regulation 3.3V

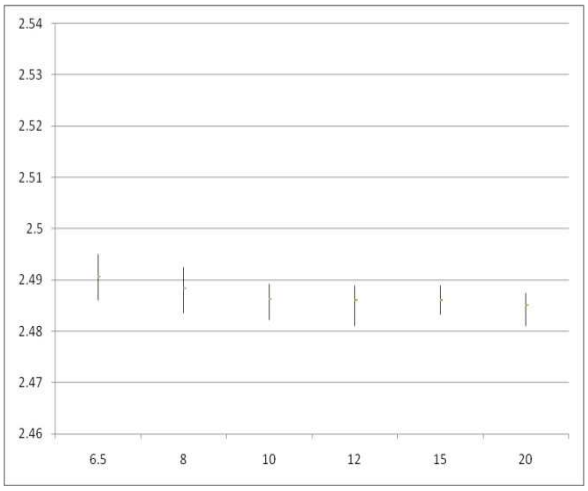


Fig. 16: Line Load Regulation 2.5V

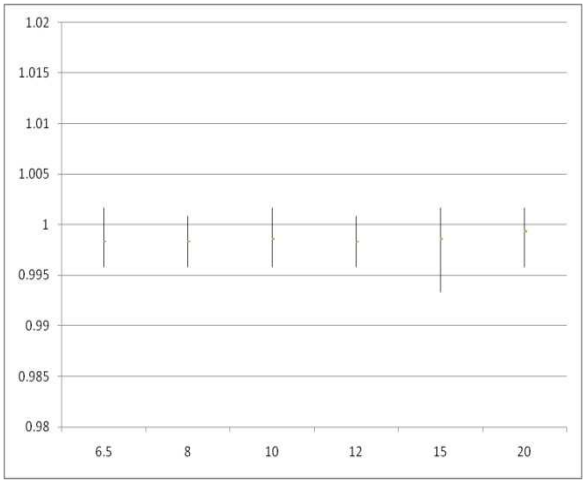


Fig. 17 Line Load Regulation 1V

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	04/14/2011	Initial release of document

BOARD REVISION HISTORY

Board Revision	Date	Description
Rev 1.1	09/2010	Initial release of evaluation board

FOR FURTHER ASSISTANCE

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Exar Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

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