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# XRP9710 and XRP9711

## Dual 6A Programmable Power Module

A New Direction in Mixed-Signal

January 2014 Rev. 1.0.1

## GENERAL DESCRIPTION

The XRP9710 and XRP9711 are programmable step down power modules providing two 6A outputs. The module package contains the switching controller, power MOSFETs, inductors and support components. As a result, external components are minimal. A wide input voltage range (4.75V to 5.5V or 5.5V to 22V) allows for single supply operation from standard power rails.

The modules measure only 12x12x2.75mm making it half the size of competing 12V capable 6Amp modules. The 2.75mm height allows them to be placed on the back of boards or under heat sinks where other solutions cannot, yet they contain two full 6A buck power stages and two Digital Pulse Width Modulator (DPWM) controllers with gate drivers. Designed to operate at a constant PWM switching frequency between 500kHz and 750kHz, the Digital Pulse Frequency Mode (DPFM) results in better than 80% efficiency at light load currents and low operating current allow for portable and Energy Star compliant applications. Each XRP9710 or XRP9711 output can be individually programmed to as low as 0.6V with a resolution as fine as 2.5mV, and configurable for precise soft start and soft stop sequencing, including delay and ramp control.

The XRP9710/1 is fully controlled via a SMBus-compliant $I^2C$ interface allowing for advanced local and/or remote reconfiguration, full performance monitoring and reporting as well as fault handling.

Built-in output over-voltage, over-temperature, over-current and under voltage lockout protections insure safe operation under abnormal operating conditions.

The XRP9710/1 is offered in a RoHS compliant, halogen-free LGA package.

## FEATURES

- **XRP9710 – Dual 6A Outputs with Differential Sensing**
- **XRP9711 – Dual 6A Outputs with Control for Two External Power Stages**
- **12 x 12 x 2.75mm LGA Package**
- **Wide Input Voltage Range: 4.75V to 22V**
  - Low Range: 4.75V to 5.5V
  - High Range: 5.5V-22V
- **Output Voltage Range: 0.6V to 5.5V**
- **SMBus Compliant - $I^2C$ Interface**
  - Full Power Monitoring and Reporting
- **3 x 15V Capable PSIOs + 2 x GPIOs**
- **Full Start/Stop Sequencing Support**
- **Built-in Thermal, Over-Current, UVLO and Output Over-Voltage Protections**
- **On-Board 5V Standby LDO**
- **On-Board Non-volatile Memory**
- **CISPR22 Level B radiated emissions**
- **PowerArchitect™ 5.1 or later Design Tool**

## APPLICATIONS

- **Servers**
- **Base Stations**
- **Switches/Routers**
- **Broadcast Equipment**
- **Industrial Control Systems**
- **Automatic Test Equipment**
- **Video Surveillance Systems**

## TYPICAL APPLICATION DIAGRAM

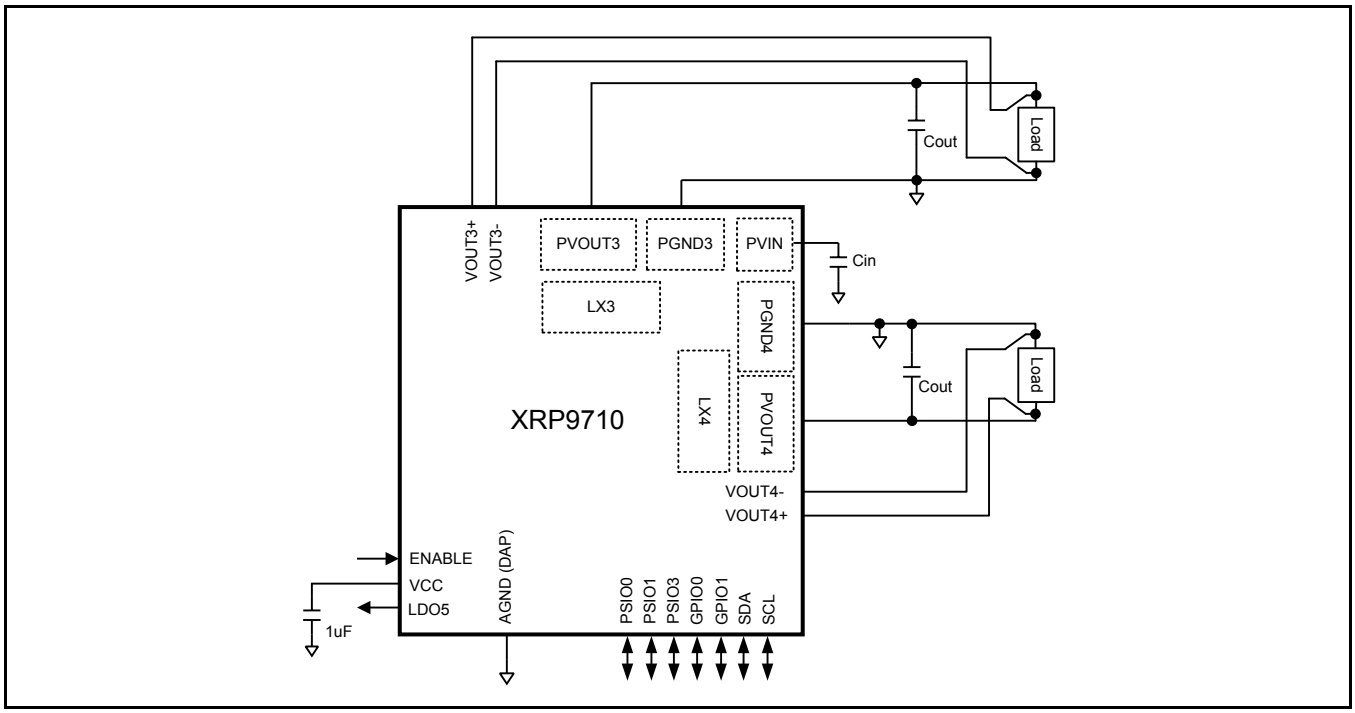



Figure 1 XRP9710 Application Diagram with differential voltage sensing

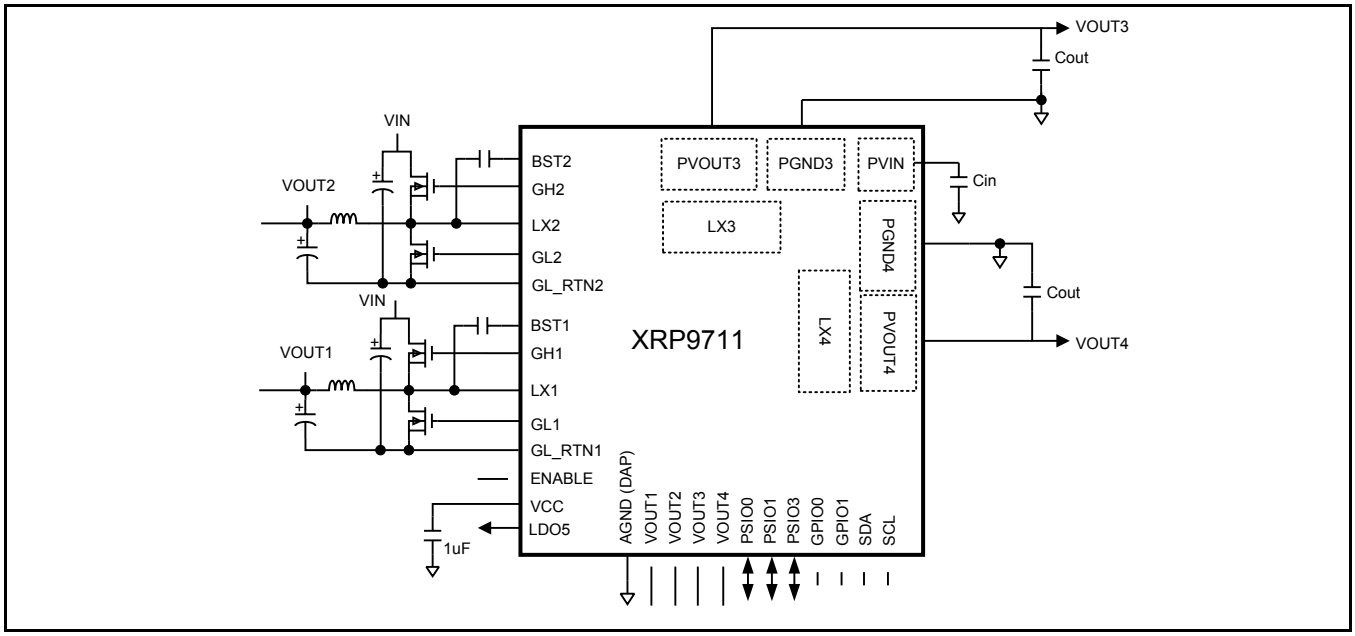



Figure 2 XRP9711 Application Diagram

## FEATURES AND BENEFITS

### World's smallest 12V capable dual 6A module at 12x12x2.75mm

### Programmable Power Benefits

- **Fully Configurable**
  - Output set point
  - Feedback compensation
  - Frequency set point
  - Under voltage lock out
  - Input voltage measurement
  - Gate drive dead time
- **Reduced Development Time**
  - Configurable and re-configurable for different Vout, Iout, Cout, and Inductor values
  - No need to change external passives for a new output specification.
- **Higher integration and Reliability**
  - Lowest component count for a fully configurable module

### PowerArchitect™ 5 Design and Configuration Software

- Wizard quickly generates a base design
- Calculates all configuration registers
- Projects can be saved and/or recalled
- GPIOs can be configured easily and intuitively
- "Dashboard" Interface can be used for real-time monitoring and debug

### System Benefits

- Reliability is enhanced via communication with the system controller which can obtain real-time data on an output voltage, input voltage and current.
- System processors can communicate with the XRP9710/1 directly to obtain data or make adjustments to react to circuit conditions
- System logging and history, diagnostics and remote reconfigurability.

### System Integration Capabilities

- **Single supply operation**
- **$I^2C$ interface allows:**
  - Communication with a System Controller or other Power Management devices for optimized system functionality
  - Access to modify or read internal registers that control or monitor:
    - Output Current
    - Input and Output Voltage
    - Soft-Start/Soft-Stop Time
    - 'Power Good'
    - Part Temperature
    - Enable/Disable Outputs
    - Over Current
    - Over Voltage
    - Temperature Faults
    - Adjusting fault limits and disabling/enabling faults
  - Packet Error Checking (PEC) on $I^2C$ communication
- **5 GPIO pins with a wide range of configurability**
  - Fault reporting (including UVLO Warn/Fault, OCP Warn/Fault, OVP, Temperature, Soft-Start in progress, Power Good, System Reset)
  - Allows a Logic Level interface with other non-digital IC's or as logic inputs to other devices
- **Frequency and Synchronization Capability**
  - Selectable switching frequency between 124kHz and 1.23MHz (500kHz to 750kHz internal power stages)
  - Main oscillator clock and DPWM clock can be synchronized to external sources
- **Internal MOSFET Drivers (XRP9711)**
  - Internal FET drivers (4Ω/2Ω) per channel
  - Built-In Automatic Dead-time adjustment
  - 17ns Rise and 11ns Fall times

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

LDO5, GLx, VOUTx ..... -0.3V to 7.0V
ENABLE ..... -0.3V to 7.0V
GPIO0/1, SCL, SDA ..... 6.0V
PSIO Inputs ..... 18V
Vcc ..... 28V
LXx ..... -1V to 28V
BSTx, GHx ..... VLXx + 6V
Storage Temperature ..... -65°C to 150°C
Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 10 sec) ..... 245°C
ESD Rating (HBM - Human Body Model) ..... 2kV

## OPERATING RATINGS

Input Voltage Range $V_{CC}$ ..... 5.5V to 25V
PVIN Voltage Range ..... 3.0 to 22V
Input Voltage Range $V_{CC}$ = LDO5 ..... 4.75V to 5.5V
VOUT1, 2, 3, 4 ..... 5.5V
Junction Temperature Range ..... -40°C to 125°C
Package Power Dissipation max at 25°C ..... 5.5W
JEDEC51-2A Package Thermal Resistance $\theta_{JA}$ ..... 18°C/W
Complies with CISPR22 ..... Level B

## ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of $T_J$ = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise indicated, $V_{CC}$ = 5.5V to 22V.

### QUIESCENT CURRENT

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| $V_{CC}$ Supply Current in SHUTDOWN | | 10 | 20 | µA | | EN = 0V, $V_{CC}$ = 12V |
| ENABLE Turn On Threshold | 0.82 | | 0.95 | V | | $V_{CC}$ = 12V Enable Rising |
| ENABLE Pin Leakage Current | | | 10 | uA | | EN=5V |
| | -10 | | | | | EN=0V |
| $V_{CC}$ Supply Current in STANDBY | | 440 | 600 | µA | | All channels disabled<br>GPIOs programmed as inputs<br>$V_{CC}$=12V,EN = 5V |
| $V_{CC}$ Supply Current 2ch PFM | | 3.1 | | mA | | 2 channels on set at 5V, VOUT forced to 5.1V, no load, non-switching, Ultra-sonic off, $V_{CC}$=12 V, No $I^2C$ activity. |
| $V_{CC}$ Supply Current 4ch PFM | | 4.0 | | mA | | 4 channels on set at 5V, VOUT forced to 5.1V, no load, non-switching, Ultra-sonic off, $V_{CC}$=12V, No $I^2C$ activity. |
| $V_{CC}$ Supply Current ON | | 18 | | mA | | All channels enabled, Fsw=600kHz, gate drivers unloaded, No $I^2C$ activity. |

### INPUT VOLTAGE RANGE AND UNDERVOLTAGE LOCKOUT

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| $V_{CC}$ Range | 5.5 | | 25 | V | • | |
| | 4.75 | | 5.5 | V | • | With $V_{CC}$ connected to LDO5 |
| PVIN Range | 3.0 | | 22 | V | • | |

## VOLTAGE FEEDBACK ACCURACY AND OUTPUT VOLTAGE SET POINT RESOLUTION

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| VOUT Regulation Accuracy Low Output Range 0.6V to 1.6V PWM Operation | -5 | | 5 | mV | | 0.6 ≤ VOUT ≤ 1.6V |
| | -20 | | 20 | mV | • | |
| | -7.5 | | 7.5 | mV | | 0.6 ≤ VOUT ≤ 1.6V |
| | -22.5 | | 22.5 | mV | • | $V_{CC}$=LDO5 |
| VOUT Regulation Accuracy Mid Output Range 0.6V to 3.2V PWM Operation | -15 | | 15 | mV | | 0.6 ≤ VOUT ≤ 3.2V |
| | -45 | | 45 | mV | • | |
| | -20 | | 20 | mV | | 0.6 ≤ VOUT ≤ 3.2V |
| | -50 | | 50 | mV | • | $V_{CC}$=LDO5 |
| VOUT Regulation Accuracy High Output Range 0.6V to 5.5V PWM Operation | -30 | | 30 | mV | | 0.6 ≤ VOUT ≤ 5.5V |
| | -90 | | 90 | mV | • | |
| | -40 | | 40 | mV | | 0.6 ≤ VOUT ≤ 4.2V |
| | -100 | | 100 | mV | • | $V_{CC}$=LDO5 |
| VOUT Regulation Range | 0.6 | | 5.5 | V | • | Without external divider network |
| VOUT Native Set Point Resolution | | 12.5<br>25<br>50 | | mV | | Low Range<br>Mid Range<br>High Range |
| VOUT Fine Set Point Resolution[1] | | 2.5<br>5<br>10 | | mV | | Low Range<br>Mid Range<br>High Range |
| VOUT Input Resistance | | 120<br>90<br>75 | | kΩ | | Low Range<br>Mid Range<br>High Range |
| VOUT Input Resistance in PFM Operation | | 10<br>1<br>0.67 | | MΩ | | Low Range<br>Mid Range<br>High Range |
| Power Good and OVP Set Point Range (from set point) | -155<br>-310<br>-620 | | 157.5<br>315<br>630 | mV | | Low Range<br>Mid Range<br>High Range |
| Power Good and OVP Set Point Accuracy | -5<br>-10<br>-20 | | 5<br>10<br>20 | mV | | Low Range<br>Mid Range<br>High Range |

Note 1: Fine Set Point Resolution not available in PFM

## CURRENT AND AUX ADC (MONITORING ADCS)

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| Current Sense Accuracy | -3.75 | ±1.25 | 3.75 | mV | | Low Range (≤120mV) |
| | -10 | | 10 | mV | • | -60mV applied |
| | -5 | ±2.5 | 5 | mV | | High Range (≤280mV) |
| | -12.5 | | +12.5 | mV | • | -150mV |
| Current Sense ADC INL | | ±0.4 | | LSB | | |
| DNL | | 0.27 | | | | |
| Current Limit Set Point Resolution and Current Sense ADC Resolution | | 1.25 | | mV | | Low Range (≤120mV) |
| | | 2.5 | | mV | | High Range (≤280mV) |
| Current Sense ADC Range | -120 | | 20 | mV | | Low Range (≤120mV) |
| | -280 | | 40 | | | High Range (≤280mV) |
| VOUT ADC Resolution | | 15<br>30<br>60 | | mV | | Low Range<br>Mid Range<br>High Range |
| VOUT ADC Accuracy | -1 | | 1 | LSB | | |
| $V_{CC}$ ADC Range | 4.6 | | 25 | V | | Note 2 |
| UVLO WARN SET | 4.4 | | 4.72 | V | | UVLO WARN set point 4.6V, $V_{CC}$=LDO5 |
| UVLO WARN CLEAR | 4.4 | | 4.72 | V | | UVLO WARN set point 4.6V, $V_{CC}$=LDO5 |
| | | | | | | |
| $V_{CC}$ ADC Resolution | | 200 | | mV | | |
| $V_{CC}$ ADC Accuracy | -1 | | 1 | LSB | | Vcc <= 20V |
| Die Temp ADC Resolution | | 5 | | °C | | |
| Die Temp ADC Range | -44 | | 156 | °C | | Output value is in Kelvin |

Note 2: Although Range of $V_{CC}$ ADC is technically 0V to 25V, below 4.55 the LDO5 hardware UVLO may have tripped.

## LINEAR REGULATOR

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| LDO5 Output Voltage | 4.85 | 5.0 | 5.15 | V | • | 5.5V ≤ $V_{CC}$ ≤ 25V<br>0mA < $I_{LDO5OUT}$ < 130mA |
| LDO5 Current Limit | 135 | 155 | 180 | mA | • | LDO5 Fault Set |
| LDO5 UVLO | 4.74 | | | V | • | $V_{CC}$ Rising |
| LDO5 PGOOD Hysteresis | | 375 | | mV | | $V_{CC}$ Falling |
| Maximum total LDO loading during ENABLE start-up | | | 30 | mA | | ENABLE transition from logic low to high. Once LDO5 in regulation above limits apply. |

## PWM GENERATORS AND OSCILLATOR

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| Switching Frequency (fsw) Range, Channels 1 and 2 | 124 | | 1230 | kHz | | See Applications Information |
| Switching Frequency (fsw) Range, Channels 3 and 4 | 500 | | 750 | kHz | | |
| fsw Accuracy | –5 | | 5 | % | | |
| CLOCK IN Synchronization Frequency | 20 | 25.7 | 31 | MHz | | When synchronizing to an external clock (Range 1) |
| CLOCK IN Synchronization Frequency | 10 | 12.8 | 15.5 | MHz | | When synchronizing to an external clock (Range 2) |

## GPIOs[3]

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| Input Pin Low Level | | | 0.8 | V | | |
| Input Pin High Level | 2.0 | | | V | | |
| Input Pin Leakage Current | | | 1 | µA | | |
| Output Pin Low Level | | | 0.4 | V | | $I_{SINK}$ = 1mA |
| Output Pin High Level | 2.4 | | | V | | $I_{SOURCE}$ = 1mA |
| Output Pin High Level | | 3.3 | 3.6 | V | | $I_{SOURCE}$ = 0mA |
| Output Pin High-Z leakage Current (GPIO pins only) | | | 10 | µA | | |
| Maximum Sink Current | | | 1 | mA | | Open Drain Mode |
| I/O Frequency | | | 30 | MHz | | I/O configured for clock synchronization input or output |

Note 3: 3.3V CMOS logic compatible, 5V tolerant.

## PSIOs[4]

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| Input Pin Low Level | | | 0.8 | V | | |
| Input Pin High Level | 2.0 | | | V | | |
| Input Pin Leakage Current | | | 1 | µA | | |
| Output Pin Low Level | | | 0.4 | V | | $I_{SINK}$ = 3mA |
| Output Pin High Level | | | 15 | V | | Open Drain. External pull-up resistor to user supply |
| Output Pin High-Z leakage Current (PSIO pins only) | | | 10 | µA | | |
| I/O Frequency | | | 5 | MHz | | |

Note 4: 3.3V/5.0V CMOS logic compatible, maximum rating of 15.0V

## SMBus ($I^2C$) Interface

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| Input Pin Low Level, $V_{IL}$ | | | 0.3 VIO | V | | VIO = 3.3 V ±10% |
| Input Pin High Level, $V_{IH}$ | 0.7 VIO | | | V | | VIO = 3.3 V±10% |
| Hysteresis of Schmitt Trigger inputs, $V_{hys}$ | 0.05 VIO | | | V | | VIO = 3.3 V±10% |
| Output Pin Low Level (open drain or collector), $V_{OL}$ | | | 0.4 | V | | $I_{SINK}$ = 3mA |
| Input leakage current | -10 | | 10 | µA | | Input is between 0.1 VIO and 0.9 VIO |
| Output fall time from $V_{IHmin}$ to $V_{ILmax}$ | 20 + 0.1 Cb | | 250 | ns | | With a bus capacitance (Cb) from 10 pF to 400 pF |
| Internal Pin Capacitance | | | 1 | pF | | |

## Gate Drivers

| Parameter | Min. | Typ. | Max. | Units | | Conditions |
|---|---|---|---|---|---|---|
| GH, GL Rise Time | | 17 | | ns | | At 10-90% of full scale, 1nF $C_{load}$ |
| GH, GL Fall Time | | 11 | | ns | | |
| GH, GL Pull-Up On-State Output Resistance | | 4 | 5 | Ω | | |
| GH, GL Pull-Down On-State Output Resistance | | 2 | 2.5 | Ω | | |
| GH, GL Pull-Down Resistance in Off-Mode | | 50 | | kΩ | | $V_{CC}$ = VCCD = 0V. |
| Bootstrap diode forward resistance | | 9 | | Ω | | @ 10mA |
| Minimum On Time | | 50 | | ns | | 1nF of gate capacitance. |
| Minimum Off Time | | 125 | | ns | | 1nF of gate capacitance |
| Minimum Programmable Dead Time | | 20 | | ns | | Does not include dead time variation from driver output stage<br>Tsw=switching period |
| Maximum Programmable Dead Time | | Tsw | | | | |
| Programmable Dead Time Adjustment Step | | 607 | | ps | | |

## BLOCK DIAGRAMS

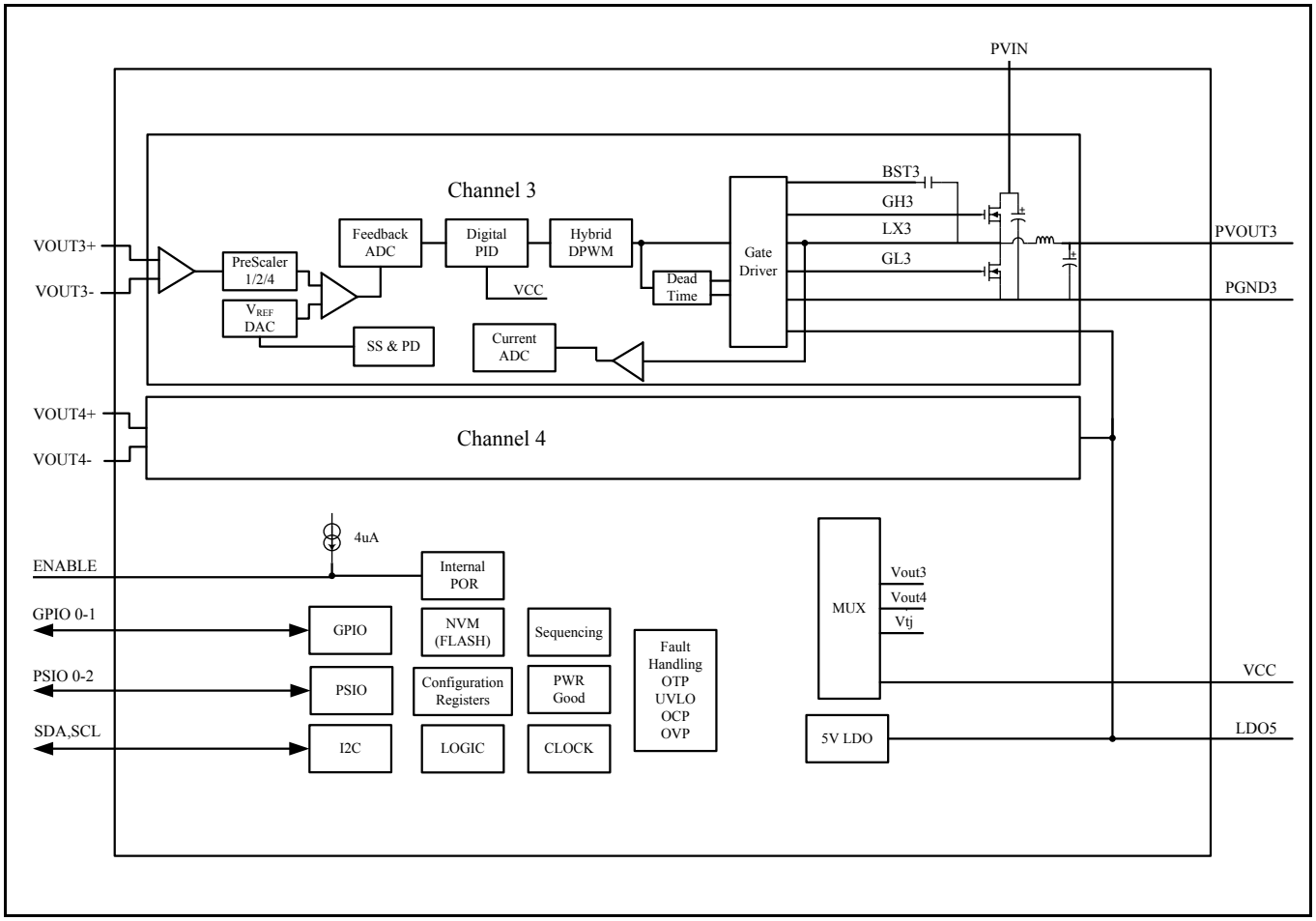



Figure 3 XRP9710 Block Diagram

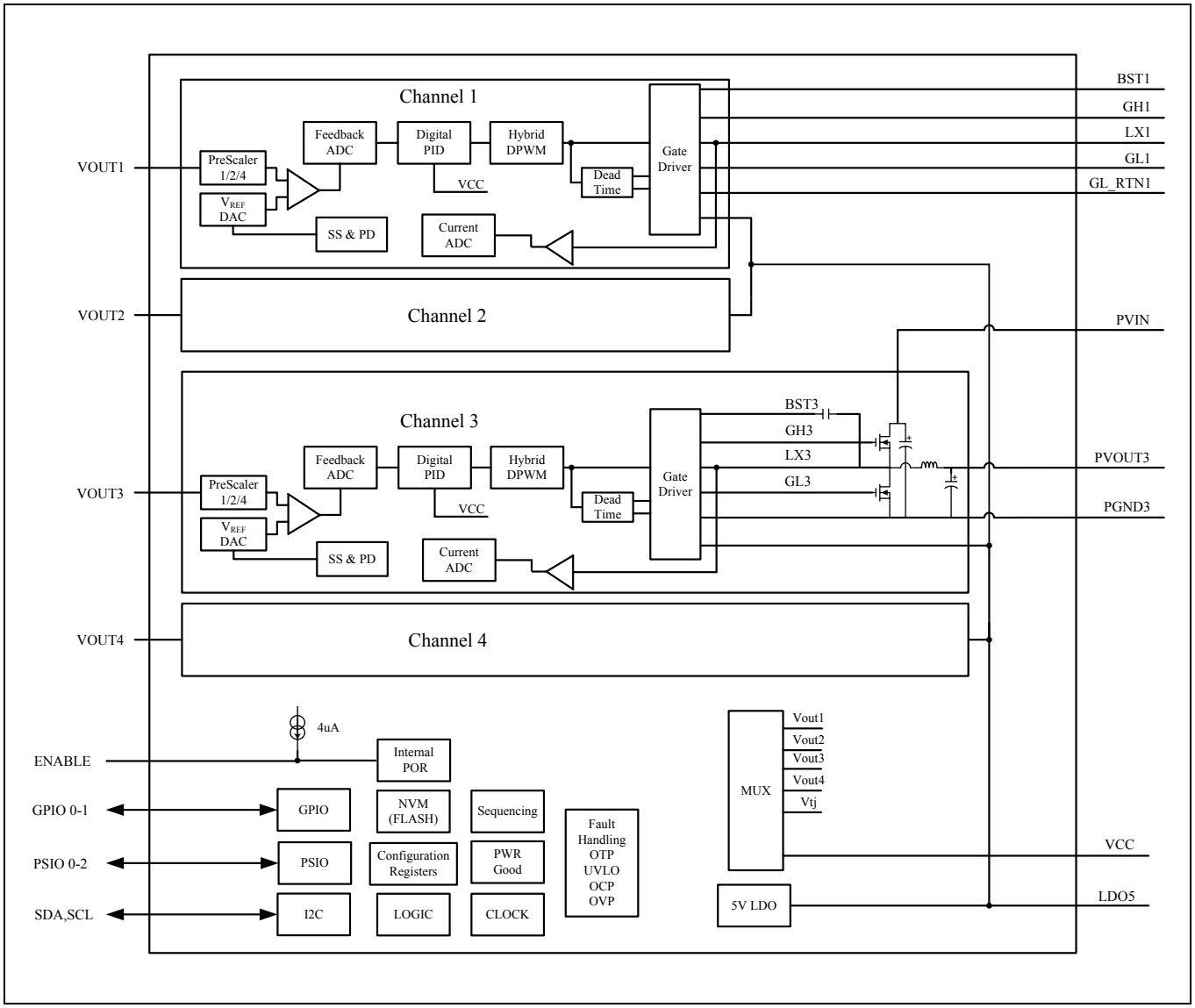



Figure 4 XRP9711 Block Diagram

## XRP9710 PIN ASSIGNMENT

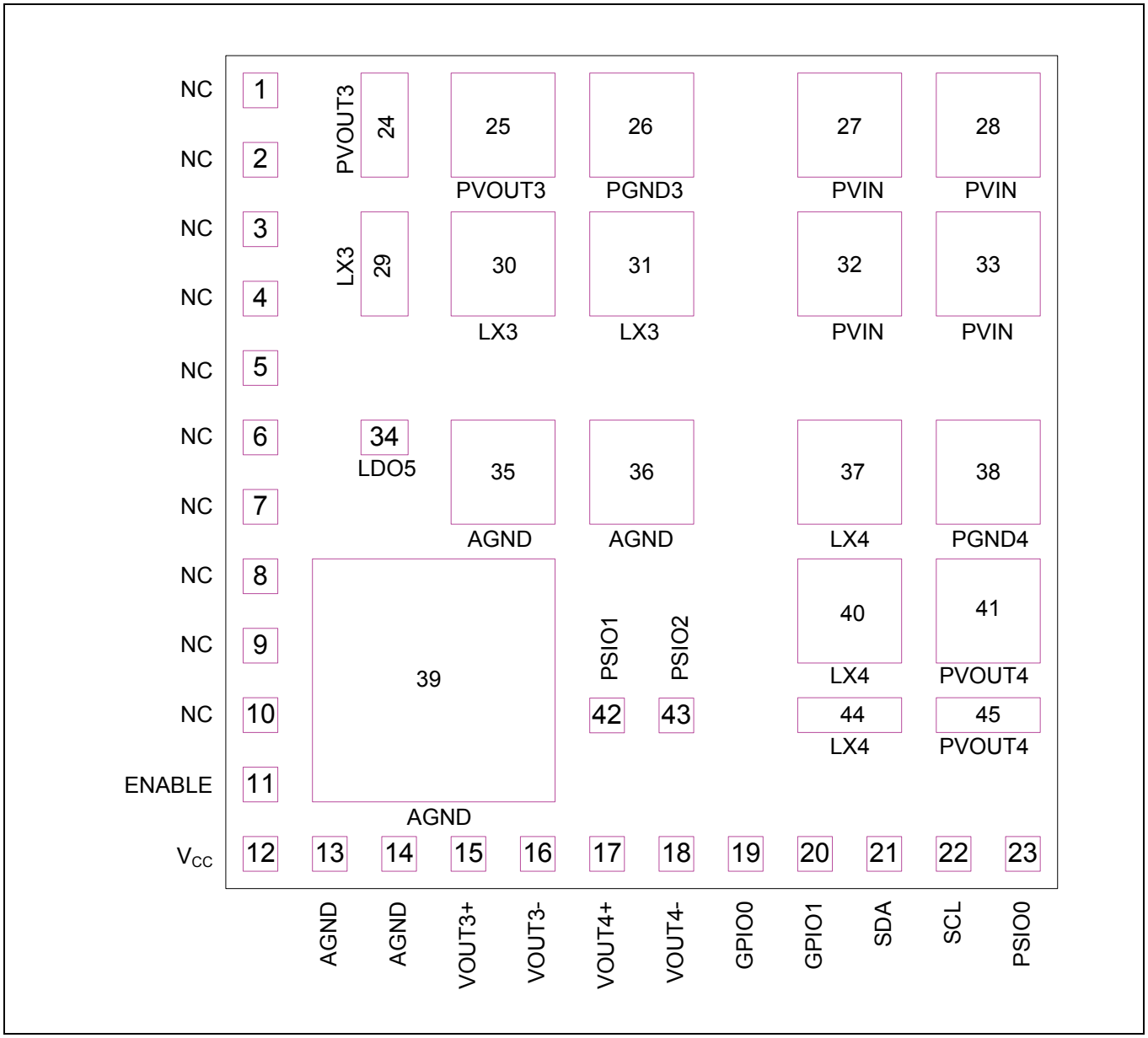



Figure 5 XRP9710 Pin Assignment, Top View

## XRP9710 PIN DESCRIPTION

| Pin # | Name | Description |
|---|---|---|
| 1-10 | NC | **No Connect** |
| 11 | ENABLE | **Enable.** If ENABLE is pulled high or allowed to float high, the chip is powered up. The pin must be held low for the XRP9710 to be placed into shutdown. |
| 12 | $V_{CC}$ | **Controller Supply Voltage.** Place a decoupling capacitor close to the controller IC. This input is used in UVLO fault generation. |
| 13 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 14 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 15 | VOUT3+ | **Feedback Pin.** Positive input of remote sensing differential amplifier. Connect to the remote voltage load, positive terminal. |
| 16 | VOUT3- | **Feedback Pin.** Negative input of remote sensing differential amplifier. Connect to the remote voltage load, negative terminal. |
| 17 | VOUT4+ | **Feedback Pin.** Positive input of remote sensing differential amplifier. Connect to the remote voltage load, positive terminal. |
| 18 | VOUT4- | **Feedback Pin.** Negative input of remote sensing differential amplifier. Connect to the remote voltage load, negative terminal. |
| 19 | GPIO0 | **I/O Logic Signal.** Can be configured as input or output. |
| 20 | GPIO1 | **I/O Logic Signal.** Can be configured as input or output. |
| 21 | SDA | **$I^2C$ Data**. SMBus/$I^2C$ serial interface communication. |
| 22 | SCL | **$I^2C$ Clock.** SMBus/$I^2C$ serial interface communication. |
| 23 | PSIO0 | **I/O Logic Signal, HV.** Open drain, high voltage compliant. Can be configured as input or output. |
| 24 | PVOUT3 | **Channel Output Power.** Output voltage for the internal channel. |
| 25 | PVOUT3 | **Channel Output Power.** Output voltage for the internal channel. |
| 26 | PGND3 | **Channel Output Ground.** Output ground for the internal channel. |
| 27 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 28 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 29 | LX3 | **Switch Node.** Switch node of the internal channel. |
| 30 | LX3 | **Switch Node.** Switch node of the internal channel. |
| 31 | LX3 | **Switch Node.** Switch node of the internal channel. |
| 32 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 33 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 34 | LDO5 | **5V LDO Output.** Used internally for power and may also be used for external power. LDO that can remain active while the rest of the IC is in standby mode. |
| 35 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 36 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 37 | LX4 | **Switch Node.** Switch node of the internal channel. |
| 38 | PGND4 | **Channel Output Ground.** Output ground for the internal channel. |
| 39 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 40 | LX4 | **Switch Node.** Switch node of the internal channel. |
| 41 | PVOUT4 | **Channel Output Power.** Output voltage for the internal channel. |
| 42 | PSIO1 | **I/O Logic Signal, HV.** Open drain, high voltage compliant. Can be configured as input or output. |
| 43 | PSIO2 | **I/O Logic Signal, HV.** Open drain, high voltage compliant. Can be configured as input or output. |
| 44 | LX4 | **Switch Node.** Switch node of the internal channel. |
| 45 | PVOUT4 | **Channel Output Power.** Output voltage for the internal channel. |

## XRP9711 PIN ASSIGNMENT

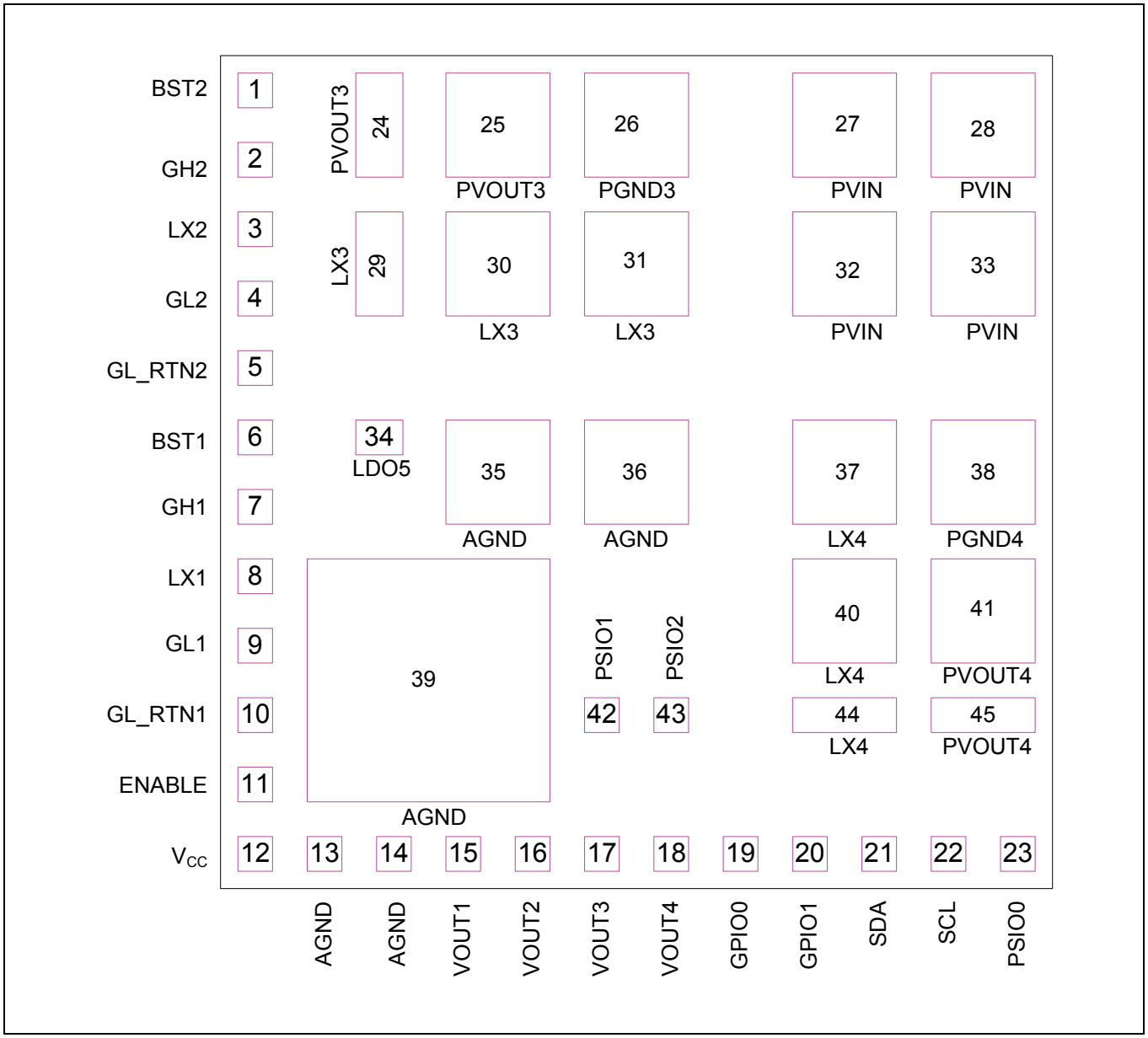



Figure 6 XRP9711 Pin Assignment, Top View

## XRP9711 PIN DESCRIPTION

| Pin # | Name | Description |
|---|---|---|
| 1 | BST2 | **Boost pin.** High side driver supply input. |
| 2 | GH2 | **High Side Gate Drive Out.** Connect directly to the gate of an external N-channel MOSFET. |
| 3 | LX2 | **Switch Node.** Return for the high-side gate driver. Connect directly to the drain of the lower FET. Also used to measure voltage drop across bottom MOSFETs |
| 4 | GL2 | **Low Side Gate Drive Out**. Connect directly to the gate of an external N-channel MOSFET. |
| 5 | GL_RTN2 | **Low Side Gate Drive Return**. This should be routed as a differential trace with GL. Connect to the source of the low side MOSFET. |
| 6 | BST1 | **Boost pin.** High side driver supply input. |
| 7 | GH1 | **High Side Gate Drive Out.** Connect directly to the gate of an external N-channel MOSFET. |
| 8 | LX1 | **Switch Node.** Return for the high-side gate driver. Connect directly to the drain of the lower FET. Also used to measure voltage drop across bottom MOSFETs |
| 9 | GL1 | **Low Side Gate Drive Out**. Connect directly to the gate of an external N-channel MOSFET. |
| 10 | GL_RTN1 | **Low Side Gate Drive Return**. This should be routed as a differential trace with GL. Connect to the source of the low side MOSFET. |
| 11 | ENABLE | **Enable.** If ENABLE is pulled high or allowed to float high, the chip is powered up. The pin must be held low for the XRP9711 to be placed into shutdown. |
| 12 | $V_{CC}$ | **Controller Supply Voltage.** Place a decoupling capacitor close to the controller IC. This input is used in UVLO fault generation. |
| 13 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 14 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 15 | VOUT1 | **Feedback Pin.** Connect to the output of the corresponding power stage |
| 16 | VOUT2 | **Feedback Pin.** Connect to the output of the corresponding power stage |
| 17 | VOUT3 | **Feedback Pin.** Connect to the output of the corresponding power stage |
| 18 | VOUT4 | **Feedback Pin.** Connect to the output of the corresponding power stage |
| 19 | GPIO0 | **I/O Logic Signal.** Can be configured as input or output. |
| 20 | GPIO1 | **I/O Logic Signal.** Can be configured as input or output. |
| 21 | SDA | **$I^2C$ Data**. SMBus/$I^2C$ serial interface communication. |
| 22 | SCL | **$I^2C$ Clock.** SMBus/$I^2C$ serial interface communication. |
| 23 | PSIO0 | **I/O Logic Signal, HV.** Open drain, high voltage compliant. Can be configured as input or output. |
| 24 | PVOUT3 | **Channel Output Power.** Output voltage for the internal channel. |
| 25 | PVOUT3 | **Channel Output Power.** Output voltage for the internal channel. |
| 26 | PGND3 | **Channel Output Ground.** Output ground for the internal channel. |
| 27 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 28 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 29 | LX3 | **Switch Node.** Switch node of the internal channel. |
| 30 | LX3 | **Switch Node.** Switch node of the internal channel. |
| 31 | LX3 | **Switch Node.** Switch node of the internal channel. |
| 32 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 33 | PVIN | **Channel Input Power.** Internally connected to drain of upper switching MOSFET |
| 34 | LDO5 | **5V LDO Output.** Used internally for power and may also be used for external power. LDO that can remain active while the rest of the IC is in standby mode. |
| 35 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 36 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 37 | LX4 | **Switch Node.** Switch node of the internal channel. |
| 38 | PGND4 | **Channel Output Ground.** Output ground for the internal channel. |
| 39 | AGND | **Analog Ground.** This is the small signal ground connection. |
| 40 | LX4 | **Switch Node.** Switch node of the internal channel. |
| 41 | PVOUT4 | **Channel Output Power.** Output voltage for the internal channel. |

| Pin # | Name | Description |
|---|---|---|
| 42 | PSIO1 | **I/O Logic Signal, HV.** Open drain, high voltage compliant. Can be configured as input or output. |
| 43 | PSIO2 | **I/O Logic Signal, HV.** Open drain, high voltage compliant. Can be configured as input or output. |
| 44 | LX4 | **Switch Node.** Switch node of the internal channel. |
| 45 | PVOUT4 | **Channel Output Power.** Output voltage for the internal channel. |

## ORDERING INFORMATION

| Part Number | Temperature Range | Marking | Package | Packing Quantity | Note 1 | $I^2C$ Default Address |
|---|---|---|---|---|---|---|
| XRP9710EY-F | -40°C≤$T_J$≤+125°C | 9710EY FWWYY Lot # | 12x12mm LGA | Tray | Halogen Free | 0x28 (7Bit) |
| XRP9710EYTR-F | | | | 2.5K/Tape & Reel | | |
| XRP9711EY-F | | 9711EY FWWYY Lot # | | Tray | | |
| XRP9711EYTR-F | | | | 2.5K/Tape & Reel | | |
| XRP9710EVB-DEMO-1-KIT | | Evaluation kit includes XRP9710EVB-DEMO-1 Evaluation Board with Power Architect software and controller board | | | | |
| XRP9711EVB-DEMO-1-KIT | | Evaluation kit includes XRP9711EVB-DEMO-1 Evaluation Board with Power Architect software and controller board | | | | |

"F" denotes "-F" part number suffix – "YY" = Year – "WW" = Work Week

## TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at $V_{CC}$ = 12V, $T_J$ = $T_A$ = 25°C, unless otherwise specified - Schematic and BOM from XRP9711EVB. See XRP9711EVB-DEMO-1 Manual.

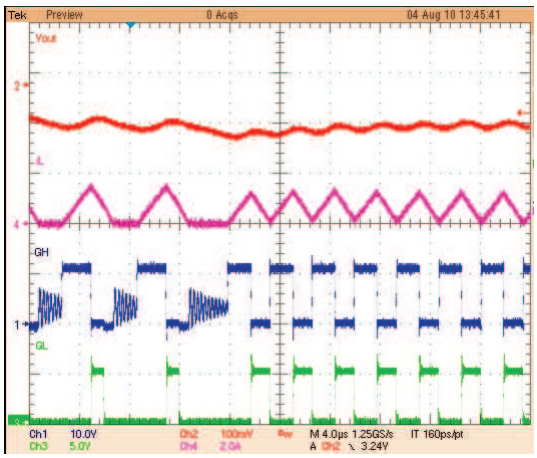



Figure 7 PFM to PWM Transition

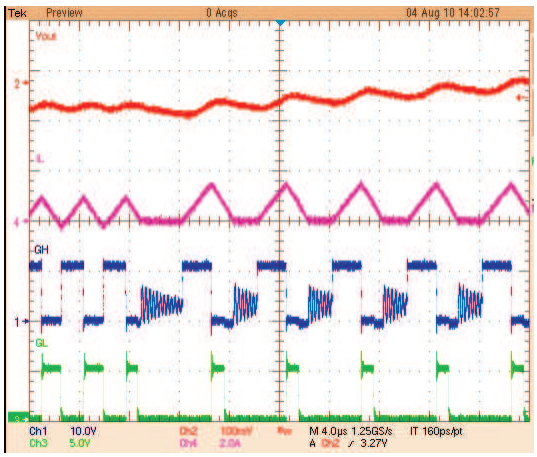



Figure 8 PWM to PFM Transition

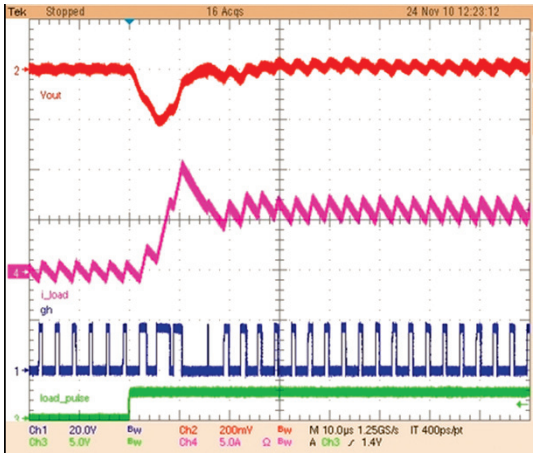



Figure 9 0-6A Transient 300kHz PWM only

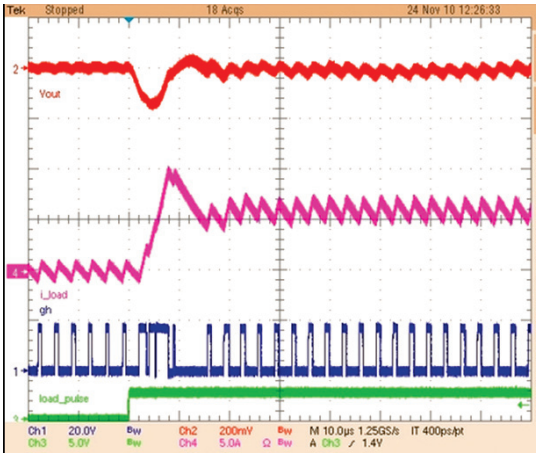



Figure 10 0-6A Transient 300kHz with OVS ±5.5%

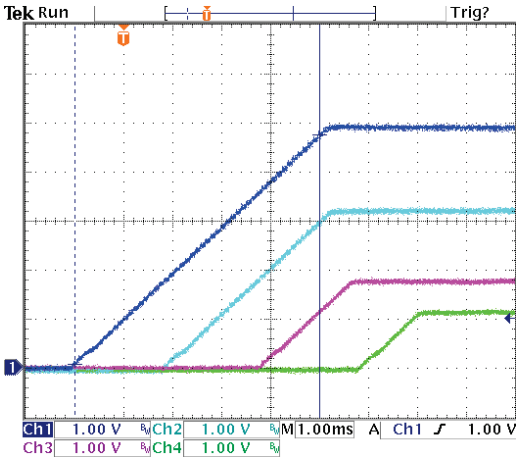



Figure 11 Sequential Start-up

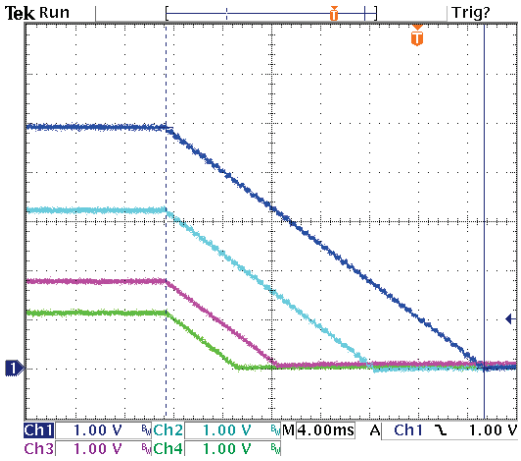



Figure 12 Sequential Shut Down

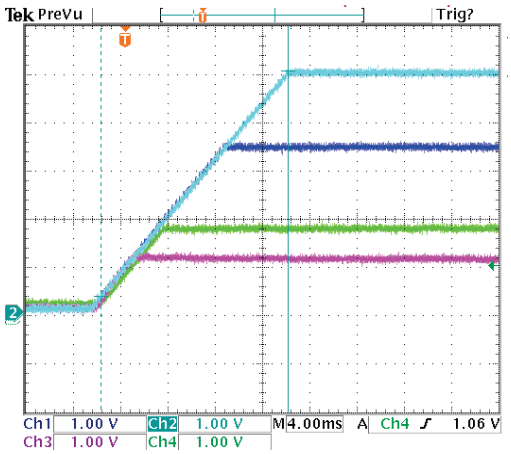



Figure 13 Simultaneous Start-up

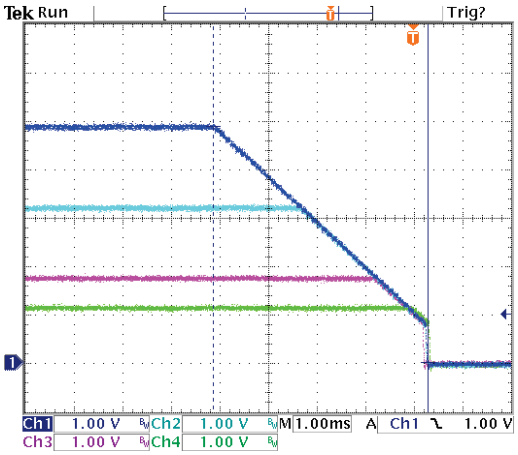



Figure14 Simultaneous Shut Down

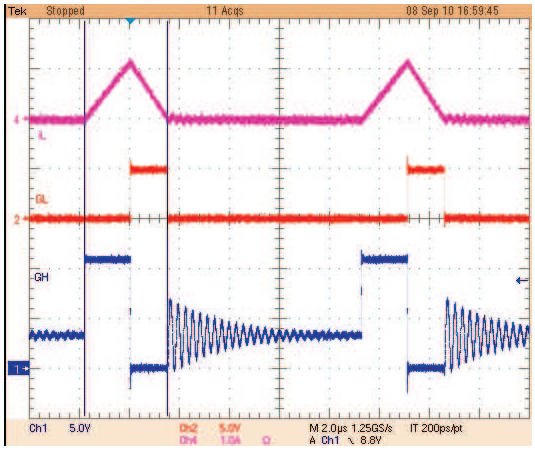



Figure15 PFM Zero Current Accuracy

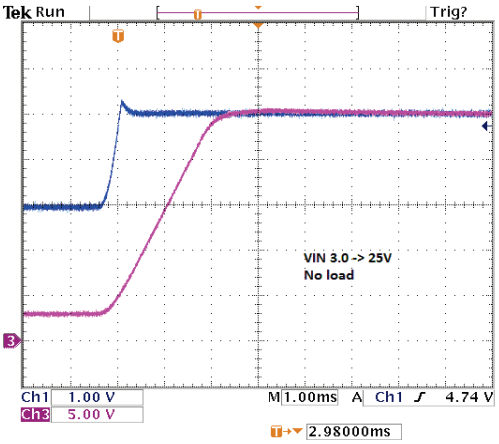



Figure16 LDO5 Brown Out Recovery, No Load

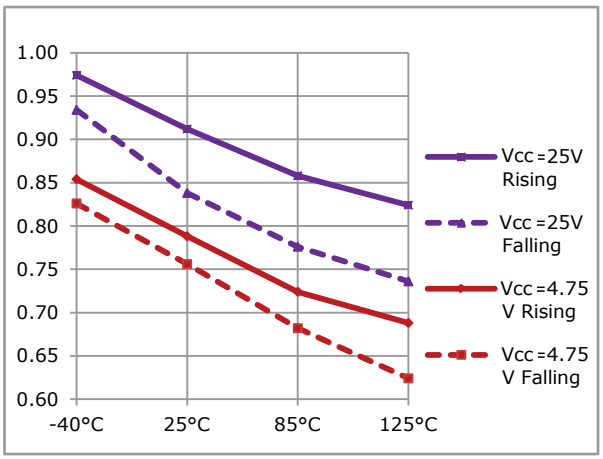



Figure 17 Enable Threshold Over Temp

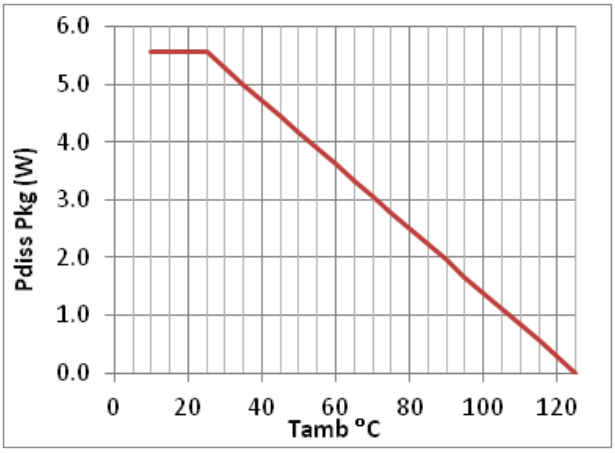



Figure 18 Package Thermal Derating

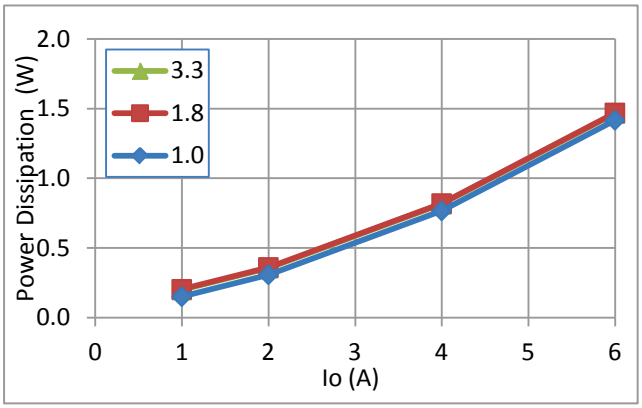



Figure 19 Vin = 5V Power Dissipation

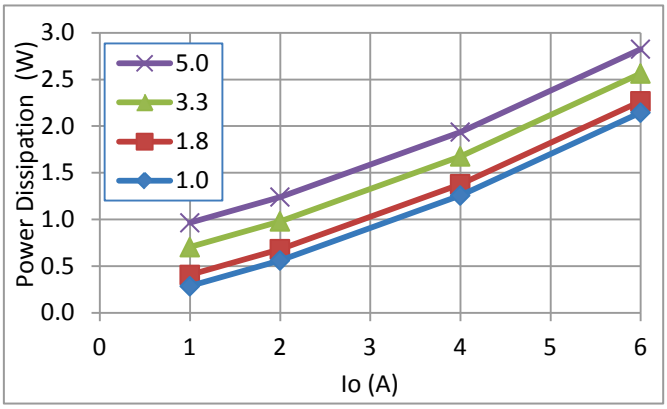



Figure 20 Vin = 12V Power Dissipation

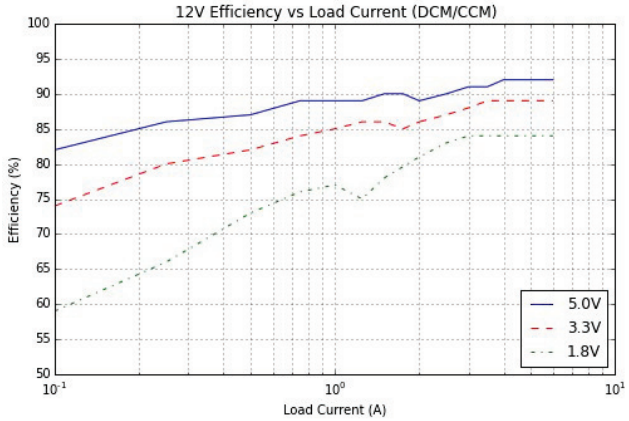



Figure 21 Efficiency, 12$V_{IN}$, 600kHz

## FUNCTIONAL OVERVIEW

The XRP9710 is a digital pulse width modulation (DPWM) power module with two 6A converters. In addition, the XRP9711 provides two additional PWM controller outputs which can directly drive external power stage. Each output voltage can be programmed from 0.6V to 5.5V without the need for an external voltage divider. The wide range of programmable DPWM switching frequencies (from 124 kHz to 1.23 MHz) enables the user to optimize for efficiency or component sizes. Since the digital regulation loop requires no external passive components, loop performance is not compromised due to external component variation or operating conditions.

The XRP9710/1 provides a number of critical safety features, such as Over-Current Protection (OCP), Over-Voltage Protection (OVP), Over-Temperature Protection (OTP) plus input Under-Voltage Lockout (UVLO). In addition, a number of key health monitoring features including warning level flags for the safety functions, Power Good (PGOOD), plus full monitoring of system voltages and currents. The above are all programmable and/or readable from the SMBus and many are steerable to the GPIOs for hardware monitoring.

For hardware communication, the XRP9710/1 has two logic level General Purpose Input-Output (GPIO) pins and three, 15V, open-drain, Power System Input-Output (PSIO) pins. Two pins are dedicated to the SMBus data (SDA) and clock (SCL).

The 5V LDO is used for internal power and is also optionally available to power external circuitry.

The primary benefit of these modules is the ultra small footprint and height, but these come with a full suite of advanced power management capabilities. All outputs are independently programmable which provides the user full control of the delay, ramp rate, and sequence during power up and power down. The user may also control how the outputs interact and power down in the event of a fault. This includes active ramp down of the output voltages to take down an output voltage as quickly as possible. Another useful feature is that the outputs can be defined and controlled as groups.

The XRP9710/1 has two main types of programmable memory. The first type is runtime registers that contain configuration, control and monitoring information for the chip. The second type is rewritable Non-Volatile Flash Memory (NVFM) that is used for permanent storage of the configuration data along with various chip internal functions. During power up, the run time registers are loaded from the NVFM allowing for standalone operation.

The XRP9710/1 brings an extremely high level of functionality and performance to a programmable power system. Ever decreasing product budgets require the designer to quickly analyze cost/performance tradeoffs to be truly successful. By incorporating four switching channels, a user LDO, and internal gate drivers, all in a single package, the XRP9710/1 allows for extremely cost effective power system designs. Another key cost factor that is often overlooked is the unanticipated Engineering Change Order (ECO). The programmable versatility of the XRP9710/1, along with the lack of hard wired, on board configuration components, allows for minor and major changes to be made on the board by simple reprogramming.

# THEORY OF OPERATION

## CHIP ARCHITECTURE

## REGULATION LOOPS

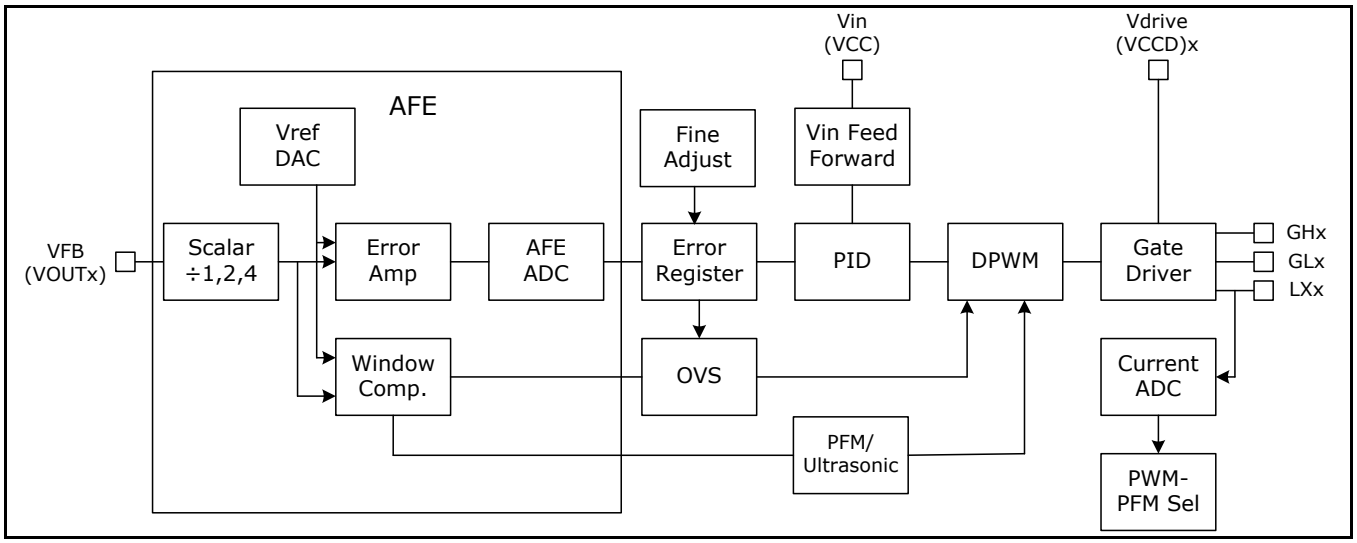



Figure 22 XRP9710 Regulation Loops

Figure 22 shows a functional block diagram of the regulation loops for an output channel. There are four separate parallel control loops; Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), Ultrasonic, and Over Sampling (OVS). Each of these loops is fed by the Analog Front End (AFE) as shown at the left of the diagram. The AFE consist of an input voltage scaler, a programmable Voltage Reference (Vref) DAC, Error Amplifier, and a window comparator. (Please note that the block diagram shown is simplified for ease of understanding. Some of the functional blocks are common and shared by each channel by means of a multiplexer.)

### PWM Loop

The PWM loop operates in Voltage Control Mode (VCM) with optional $V_{IN}$ feed forward based on the voltage at the $V_{CC}$ pin. The reference voltage (Vref) for the error amp is generated by a 0.15V to 1.6V DAC that has a 12.5mV resolution. In order to provide a full 0.6V to 5.5V output voltage range, an input scaler is used to reduce feedback voltages for higher output voltages to bring them within the 0.15V to 1.6V control range. So for output voltages up to 1.6V (low range) the scaler has a gain of 1. For output voltages from 1.6V to 3.2V (mid range) the scaler gain is 1/2 and for voltages greater than 3.2V (high range) the gain is 1/4. This results in the low range having a reference voltage resolution of 12.5mV, the mid range having a resolution of 25mV and the high range having a resolution of 50mV. The error amp has a gain of 4 and compares the output voltage of the scaler to Vref to create an error voltage on its output. This is converted to a digital error term by the AFE ADC and is stored in the error register. The error register has a fine adjust function that can be used to improve the output voltage set point resolution by a factor of 5 resulting in a low range resolution of 2.5mV, a mid range resolution of 5mV and a high range resolution of 10mV. The output of the error register is then used by the Proportional Integral Derivative (PID) controller to manage the loop dynamics.

The XRP9710/1 PID is a 17-bit five-coefficient control engine that calculates the required duty cycle under the various operating conditions and feeds it to the Digital Pulse Width Modulator (DPWM). Besides the normal

coefficients the PID also uses the $V_{IN}$ voltage to provide a feed forward function.

The XRP9710/1 DPWM includes a special delay timing loop that provides a timing resolution that is 16 times the master oscillator frequency (103MHz) for a timing resolution of 607ps for both the driver pulse width and dead time delays. The DWPM produces the Gate High (GH) and Gate Low (GL) signals for the driver. The maximum and minimum on-times and dead time delays are programmable by configuration resisters.

To provide current information, the output inductor current is measured by a differential amplifier that reads the voltage drop across the $R_{DS}$ of the lower FET during its on time. There are two selectable ranges, a low range with a gain of 8 for a +20mV to -120 mV range, and a high range with a gain of 4 for a +40mV to -280mV range. The optimum range to use will depend on the maximum output current and the $R_{DS}$ of the lower FET. The measured voltage is then converted to a digital value by the current ADC block. The resulting current value is stored in a readable register, and also used to determine when PWM to PFM transitions should occur.

### PFM mode loop

The XRP9710/1 has a PFM loop that can be enabled to improve efficiency at light loads. By reducing switching frequency and operating in the discontinuous conduction mode (DCM), both switching and $I^2R$ losses are minimized.

Figure 23 shows a functional diagram of the PFM logic.

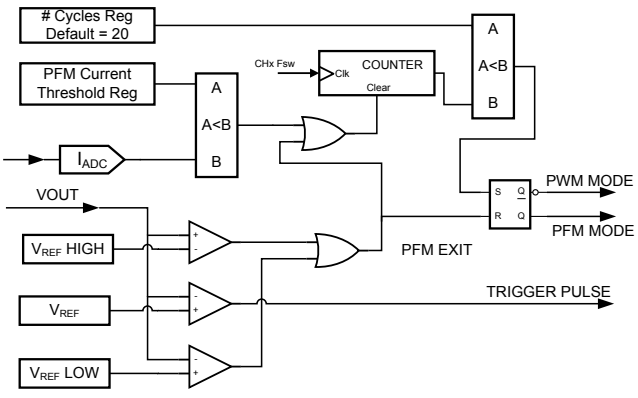



Figure 23 PFM Enter/Exit Functional Diagram

The PFM loop works in conjunction with the PWM loop and is entered when the output current falls below a programmed threshold level for a programmed number of cycles. When PFM mode is entered, the PWM loop is disabled and instead, the scaled output voltage is compared to Vref with a window comparator. The window comparator has three thresholds; normal (Vref), high (Vref + %high) and low (Vref - %low). The %high and %low values are programmable and track Vref.

In PFM mode, the normal comparator is used to regulate the output voltage. If the output voltage falls below the Vref level, the comparator is activated and triggers the DPWM to start a switching cycle. When the high side FET is turned on, the inductor current ramps up which charges up the output capacitors and increases their voltage. After the completion of the high side and low side on-times, the lower FET is turned off to inhibit any inductor reverse current flow. The load current then discharges the output capacitors until the output voltage falls below Vref and the normal comparator is activated. This triggers the DPWM to start the next switching cycle. The time from the end of the switching cycle to the next trigger is referred to as the dead zone. When PFM mode is initially entered the switching duty cycle is equal to the steady-state PWM duty cycle. This will cause the inductor ripple current to be the same level that it was in PWM mode. During operation the PFM duty cycle is calculated based on the ratio of the output voltage to $V_{CC}$. This method ensures that the output voltage ripple is well controlled and is much lower than other architectures which use a "burst" methodology.

If the output voltage goes outside the high/low windows, PFM mode is exited and the PWM loop is reactivated.

Although the PFM mode is effective at improving efficiency at light load, at very light loads the dead zone time can increase to the point where the switching frequency can enter the audio hearing range. When this happens some components, like the output inductor and ceramic capacitors, can emit audible

noise. The amplitude of the noise depends mainly on the board design and on the manufacturer and construction details of the components. Proper selection of components can reduce the sound to very low levels. In general Ultrasonic Mode is not used unless required as it reduces light load efficiency.

### Ultrasonic Mode

Ultrasonic mode is an extension of PFM to ensure that the switching frequency never enters the audible range. When this mode is entered, the switching frequency is set to 30kHz and the duty cycle of the upper and lower FETs, which are fixed in PFM mode, are decreased as required to keep the output voltage in regulation while maintaining the 30kHz switching frequency.

Under extremely light or zero load currents, the GH on time pulse width can decrease to its minimum width. When this happens, the lower FET on time is increased slightly to allow a small amount of reverse inductor current to flow back into $V_{IN}$ to keep the output voltage in regulation while maintaining the switching frequency above the audio range.

### Oversampling OVS Mode

Oversampling (OVS) mode is a feature added to the XRP9711 to improve transient response for the two external channels. This mode can only be enabled when the channel switching frequency is operating in 1x frequency mode. In OVS mode the output voltage is sampled four times per switching cycle and is monitored by the AFE window comparators. If the voltage goes outside the set high or low limits, the OVS control electronics can immediately modify the pulse width of the GH or GL drivers to respond accordingly, without having to wait for the next cycle to start. OVS has two types of response depending on whether the high limit is exceeded during an unloading transient (Over Voltage), or the low limit is exceeded during a loading transient (Under Voltage).

**Under Voltage OVS:** If there is an increasing current load step, the output voltage will drop until the regulator loop adapts to the new conditions to return the voltage to the correct level. Depending on where in the switching cycle the load step happens there can be a delay of up to one switching cycle before the control loop can respond. With OVS enabled if the output voltage drops below the lower level, an immediate GH pulse will be generated and sent to the driver to increase the output inductor current toward the new load level without having to wait for the next cycle to begin. If the output voltage is still below the lower limit at the beginning of the next cycle, OVS will work in conjunction with the PID to insert additional GH pulses to quickly return the output voltage back within its regulation band. The result of this system is transient response capabilities on par or exceeding those of a constant on-time control loop.

**Over Voltage OVS:** When there is a step load current decrease, the output voltage will increase (bump up) as the excess inductor current that is no longer used by the load flows into the output capacitors causing the output voltage to rise. The voltage will continue to rise until the inductor current decreases to the new load current. With OVS enabled, if the output voltage exceeds the high limit of the window comparator, a blanking pulse is generated to truncate the GH signal. This causes inductor current to immediately begin decreasing to the new load level. The GH signal will continue to be blanked until the output voltage falls below the high limit. Again, since the output voltage is sampled at four times the switching frequency, over shoot will be decreased and the time required to get back into the regulation band is also decreased.

OVS can be used in conjunction with both the PWM and PFM operating modes. When it is activated it can noticeably decrease output voltage excursions when transitioning between PWM and PFM modes.

## LDOs

The XRP9710/1 has an internal Low Drop-Out (LDO) linear regulator that generates 5.0V (LDO5) for both internal and external use. LDO5 is the main power input to the device and is supplied by an external 5.5V to 25V $V_{CC}$ supply. The 5V output is used by the XRP9710/1 as a standby power supply and supply power to the 5V gate drivers. The total output current that the 5V LDO can provide is 130mA. The XRP9710/1 consumes approximately 20mA and the rest is the gate drive currents. *During initial power up, the maximum external load should be limited to 30mA.*

For operation with a $V_{CC}$ of 4.75V to 5.5V, the LDO5 output needs to be connected directly to $V_{CC}$ on the board.

## CLOCKS AND TIMING

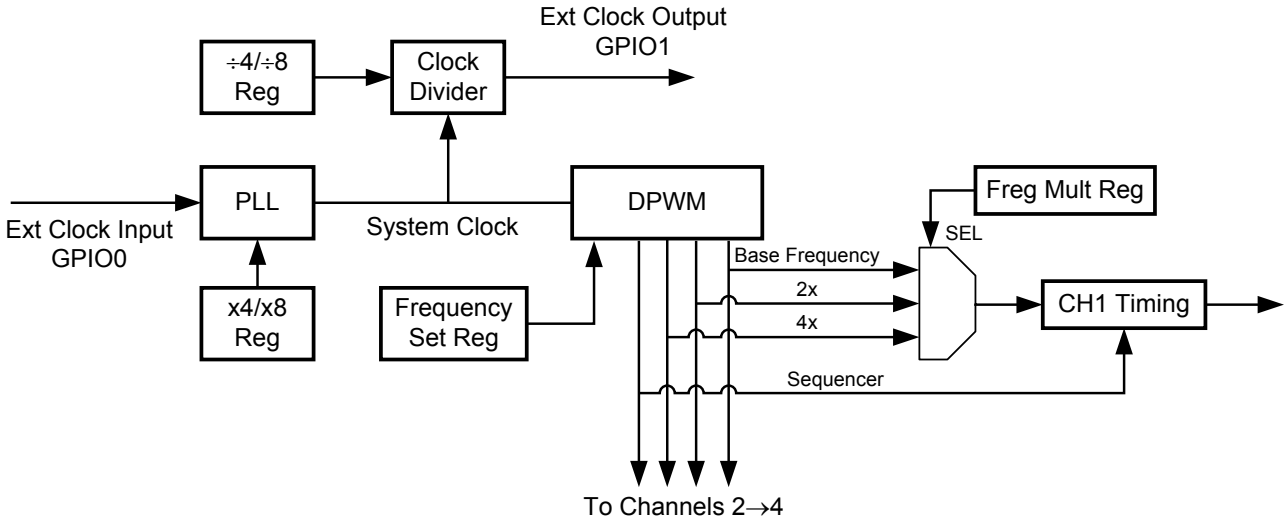



Figure 24 XRP9710 Timing Block Diagram

Figure 24 shows a simplified block diagram of the XRP9710/1 timing. Again, please note that the function blocks and signal names used are chosen for ease of understanding and do not necessarily reflect the actual design.

The system timing is generated by a 103MHz internal system clock (Sys_Clk). There are two ways that the 103MHz system clock can be generated. These include an internal oscillator and a Phase Locked Loop (PLL) that is synchronized to an external clock input. The basic timing architecture is to divide the Sys_Clk down to create a fundamental switching frequency (Fsw_Fund) for all the output channels that is settable from 124kHz to 306kHz. The switching frequency for a channel (Fsw_CHx) can then be selected as 1 time, 2 times or 4 times the fundamental switching frequency.

To set the base frequency for the output channels, an "Fsw_Set" value representing the base frequency shown in Table 1, is entered into the switching frequency configuration register. Note that Fsw_Set value is basically equal to the Sys_Clk divided by the base frequency. The system timing is then created by dividing down Sys_Clk to produce a base frequency clock, 2X and 4X times the base frequency clocks, and sequencing timing to position the output channels relative to each other. Each output channel then has its own frequency multiplier register that is used to select its final output switching frequency.

Table 1 shows the available channel switching frequencies for the XRP9710/1 device. The shaded areas show the allowable frequencies of the internal power stages. In practice the PowerArchitect™ 5.1 (PA 5.1) design tool

handles all the details and the user only has to enter the fundamental switching frequency and the 1x, 2x, 4x frequency multiplier for each channel.

If an external clock is used, the frequencies in this table will shift accordingly.

| Base Frequency kHz | Available 2x Frequencies kHz | Available 4x Frequencies kHz |
|---|---|---|
| 123.8 | 247.6 | 495.2 |
| 126.2 | 252.5 | 504.9 |
| 128.8 | 257.5 | 515.0 |
| 131.4 | 262.8 | 525.5 |
| 134.1 | 268.2 | 536.5 |
| 137.0 | 273.9 | 547.9 |
| 139.9 | 279.9 | 559.8 |
| 143.1 | 286.1 | 572.2 |
| 146.3 | 292.6 | 585.2 |
| 149.7 | 299.4 | 598.8 |
| 153.3 | 306.5 | 613.1 |
| 157.0 | 314.0 | 628.0 |
| 160.9 | 321.9 | 643.8 |
| 165.1 | 330.1 | 660.3 |
| 169.4 | 338.8 | 677.6 |
| 174.0 | 348.0 | 695.9 |
| 178.8 | 357.6 | 715.3 |
| 183.9 | 367.9 | 735.7 |
| 189.3 | 378.7 | 757.4 |
| 247.6 | 495.2 | 990.4 |
| 257.5 | 515.0 | 1030.0 |
| 268.2 | 536.5 | 1072.9 |
| 279.9 | 559.8 | 1119.6 |
| 292.6 | 585.2 | 1170.5 |
| 306.5 | 613.1 | 1226.2 |

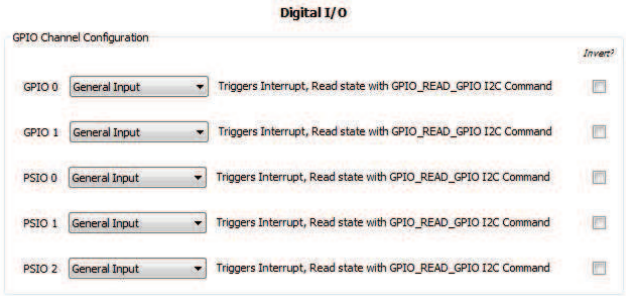
Table 1

## SUPERVISORY AND CONTROL

Power system design with XRP9710/1 is accomplished using PA 5.1 design tool. All figures referenced in the following sections are taken from PA 5.1. Furthermore, the following sections reference I²C commands. For more information on these commands, refer to ANP-38. XRP9710/1 is supported with the commands listed in ANP-38 with the exception of XRP9710 using only the channel 3 and 4 related commands.

## DIGITAL I/O

XRP9710/1 has two General Purpose Input Output (GPIO) and three Power System Input Output (PSIO) user configurable pins.

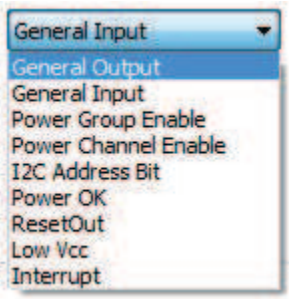



- GPIOs are 3.3V CMOS logic compatible and 5V tolerant.
- PSIOs which configured as outputs are open drain and require external pull-up resistors. These I/Os are 3.3V and 5V CMOS logic compatible, and up to 15V capable.

The polarity of the GPIO/PSIO pins is set in PA 5.1 or with an I²C command.

### Configuring GPIO/PSIOs

The following functions can be controlled from or forwarded to any GPIO/PSIO:




- **General Output** – set with an I²C command
- **General Input** – triggers an interrupt; state read with an I²C command
- **Power Group Enable** – controls enabling and disabling of Group 1 and Group 2.
- **Power Channel Enable** – controls enabling and disabling of an individual channel.
- **I²C Address Bit** – controls an I²C address bit.
- **Power OK** – indicates that selected channels have reached their target levels and have not faulted. Multiple channel selection is available, in which case the resulting signal is the AND logic function of all channels selected.
- **ResetOut** – is delayed Power OK. Delay is programmable in 1msec increments with the range of 0 to 255 msecs.
- **Low Vcc** – indicates when Vcc has fallen below the UVLO fault threshold and when the UVLO condition clears (Vcc voltage rises above the UVLO warning level).
- **Interrupt** – the controller generated interrupt selection and clearing is done through I²C commands.

Interrupt, Low Vcc, Power OK and ResetOut signals can only be forwarded to a single GPIO/PSIO.

In addition, the following are functions that are unique to GPIO0 and GPIO1.