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SINGLE CHANNEL DS3/E3 FRAMER IC WITH HDLC CONTROLLER

OCTOBER 2003 *REV. 1.2.1*

GENERAL DESCRIPTION

The XRT72L50, single Channel DS3/E3 Framer IC is designed to accept user data from the Terminal Equipment and insert this data into the payload bit-fields within an outbound DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an inbound DS3/E3 Data Stream from the Remote Terminal Equipment and extract out the user data.

The XRT72L50 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L50 DS3/E3 Framer IC consists of a Transmit section, Receiver section, Performance Monitor Section and a Microprocessor interface.

The Transmit Section includes a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Section consists of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of Reset-upon-Read and Read-Only registers that contain cumulative and one-second statistics that reflect the performance/health of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 1 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 100 Pin PQFP package
- 3.3V Power Supply with 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT72L50

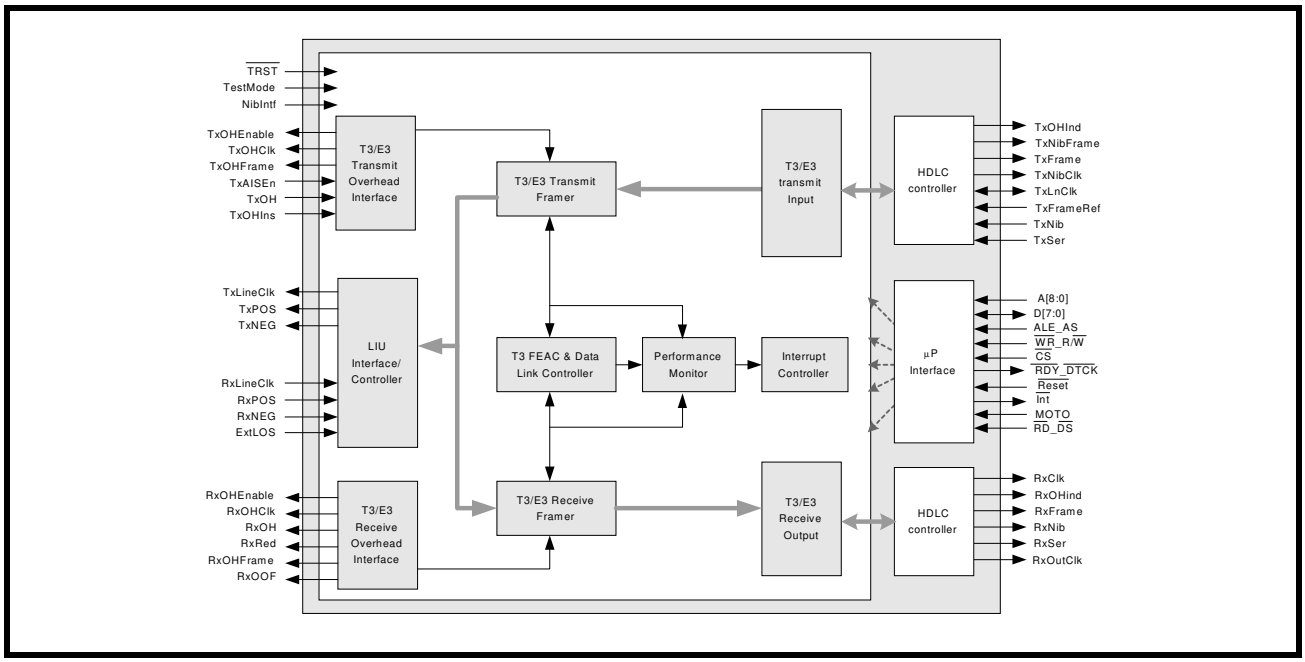
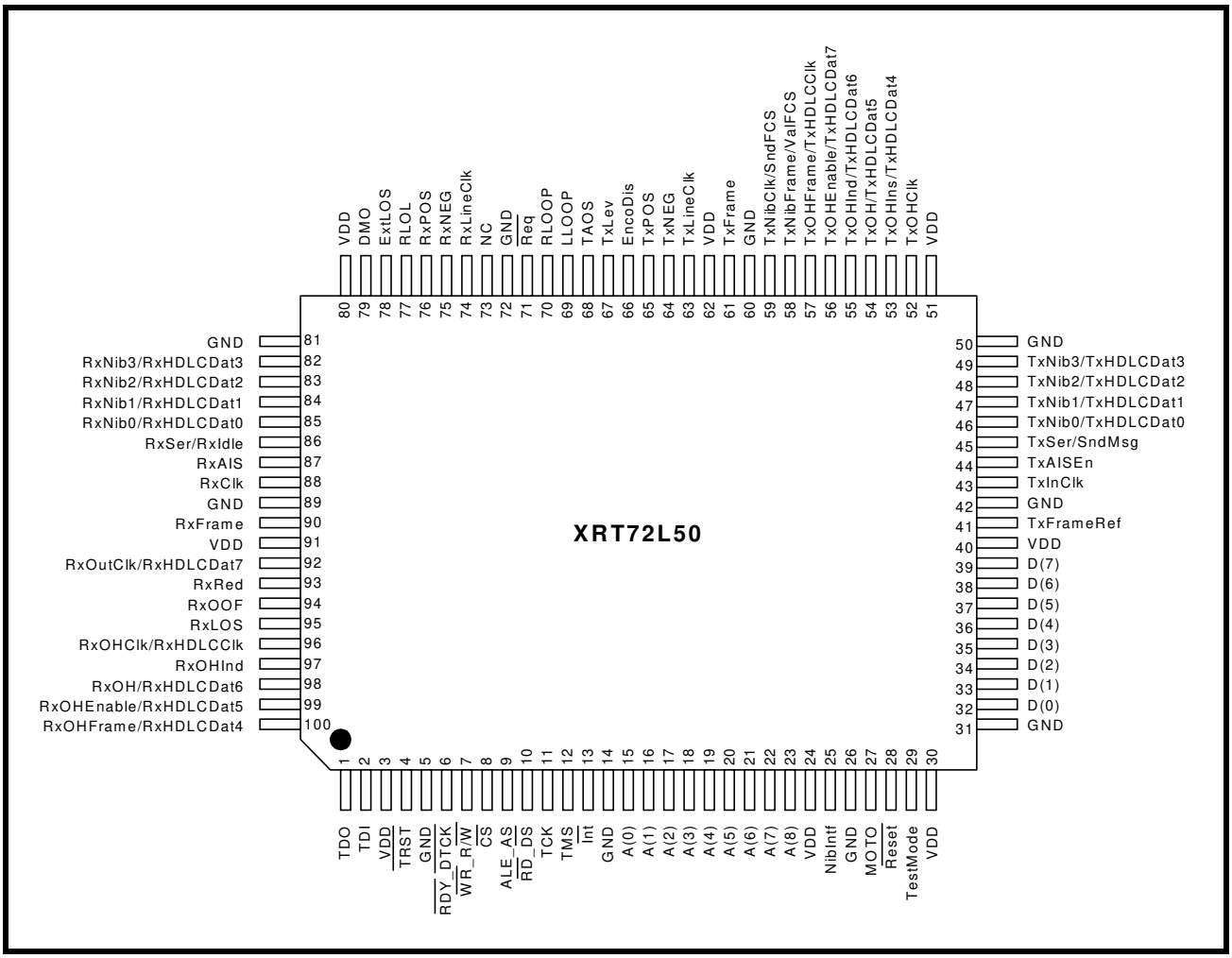


FIGURE 2. PIN OUT OF THE XRT72L50



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT72L50IQ	14x20mm, 100 Lead Plastic QFP	-40°C to +85°C

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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
1	TDO	O	**Test Data Out:** Boundary Scan test data output.
2	TDI	I	**Test Data In:** Boundary Scan Test data input.
3	VDD	****	**Power Supply 3.3V ± 5%**
4	$\overline{TRST}$	I	**JTAG Reset Pin:** Resets Boundary Scan Logic.
5	GND	****	**Ground**
6	$\overline{RDY}$_$\overline{DTCK}$	O	**READY or DTACK:** This active-low output pin will function as the READY output, when the microprocessor interface is running in the Intel Mode; and will function as the DTACK output, when the microprocessor interface is running in the Motorola Mode. **Intel Mode - READY Output:** When the Framer negates this output pin (e.g., toggles it "Low"), it indicates (to the µP) that the current READ or WRITE cycle is completed. **Motorola Mode - DTACK (Data Transfer Acknowledge) Output:** The Framer device will assert this pin in order to inform the local microprocessor that the present READ or WRITE cycle is nearly complete. If the Framer device requires that the current READ or WRITE cycle be extended, then the Framer will delay its assertion of this signal. The 68000 family of µPs requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.
7	$\overline{WR}$_R/$\overline{W}$	I	**Write Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this active-low input pin functions as the $\overline{WR}$ (Write Strobe) input signal from the µP. Once this active-low signal is asserted, then the Framer will latch the contents of the µP Data Bus, into the addressed register (or RAM location) within the Framer IC. In the Intel Mode, data gets latched on the rising edge of $\overline{WR}$ **R/W Input Pin (Motorola Mode):** When the Microprocessor Interface is operating in the Motorola Mode, this pin is functionally equivalent to the R/$\overline{W}$ pin. In the Motorola Mode, a READ operation occurs if this pin is at a logic "1". Similarly, a WRITE operation occurs if this pin is at a logic "0".
8	$\overline{CS}$	I	**Chip Select Input:** This active-low input signal selects the Microprocessor Interface Section of the Framer device and enables READ/WRITE operations between the Local Microprocessor and the Framer on-chip registers and RAM locations.
9	ALE_AS	I	**Address Latch Enable/Address Strobe:** This input is used to latch the address (present at the Microprocessor Interface Address Bus, A(8:0)) into the Framer Microprocessor Interface circuitry and to indicate the start of a READ/WRITE cycle. This input is active-high in the Intel Mode (MOTO = "Low") and active-low in the Motorola Mode (MOTO = "High").

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
10	$\overline{RD}\_\overline{DS}$	I	**Read Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this input will function as the $\overline{RD}$ (READ STROBE) input signal from the local µP. Once this active-low signal is asserted, then the Framer will place the contents of the addressed registers (within the Framer) on the Microprocessor Data Bus (D(7:0)). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe (Motorola Mode):** If the microprocessor interface is operating in the Motorola mode, then this pin will function as the active-low Data Strobe signal.
11	TCK	I	**Test Clock:** Boundary Scan clock input.
12	TMS	I	**Test Mode Select:** Boundary Scan Mode Select input.
13	$\overline{Int}$	O	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Framer device is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the Interrupt Request input of the local microprocessor.
14	GND	****	**Ground**
15	A(0)	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit):** (Please see description for A(8) pin 23)
16	A(1)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
17	A(2)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
18	A(3)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
19	A(4)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
20	A(5)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
21	A(6)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
22	A(7)	I	**Address Bus Input (Microprocessor Interface) - Bit 7** See description of pin 23
23	A(8)	I	**Address Bus Input (Microprocessor Interface) - MSB (Most Significant Bit):** This input pin, along with inputs A0 - A7 are used to select the on-chip Framer register and RAM space for READ/WRITE operations with the local microprocessor.
24	VDD	****	**Power Supply 3.3V ± 5%**

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
25	NibIntf	I	**Nibble Interface Select Input Pin:** This input pin allows the user to configure the Transmit Payload Data Input Interface and the Receive Payload Data Output Interface to operate in either the Serial-Mode or the Nibble/Parallel-Mode. Setting this input pin "High" configures the Transmit and Receive Terminal Interfaces to operate in the Nibble/Parallel-Mode. In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data (from the Terminal Equipment) in a nibble-parallel manner via the TxNib[3:0] input pins. Further, the Receive Payload Data Output Interface block will output the inbound payload data (to the Terminal Equipment) in a nibble-parallel manner via the RxNib[3:0] output pin. HDLC mode of operation requires Nibble/Parallel mode setup. Setting this input pin "Low" configures the Transmit and Receive Terminal Interfaces to operate in the Serial Mode. In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data (from the Terminal Equipment) in a serial manner via the TxSer input pin. Further, the Receive Payload Data Output Interface block will output the inbound payload data (to the Terminal Equipment) in a serial manner via the RxSer output pin.
26	GND	****	**Ground**
27	MOTO	I	**Motorola/Intel Processor Interface Select Mode:** This input pin allows the user to configure the Microprocessor Interface to interface with either a Motorola-type or Intel-type microprocessor/microcontroller. Tying this input pin to VCC, configures the microprocessor interface to operate in the Motorola mode (e.g., the Framer device can be readily interfaced to a Motorola type local microprocessor). Tying this input pin to GND configures the Microprocessor Interface to operate in the Intel Mode (e.g., the Framer device can be readily interfaced to a Intel type local microprocessor).
28	$\overline{\text{Reset}}$	I	**Reset Input:** When this active-low signal is asserted, the Framer device will be asynchronously reset. Additionally, all outputs will be tri-stated, and all on-chip registers will be reset to their default values.
29	TestMode	***	**Factory Test Pin:** The user should tie this pin to Ground.
30	VDD	****	**Power Supply 3.3V ± 5%**
31	GND	****	**Ground**
32	D(0)	I/O	**Bit 0 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
33	D(1)	I/O	**Bit 1 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
34	D(2)	I/O	**Bit 2 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
35	D(3)	I/O	**Bit 3 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
36	D(4)	I/O	**Bit 4 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
37	D(5)	I/O	**Bit 5 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
38	D(6)	I/O	**Bit 6 of Bi-Directional Data Bus (Microprocessor Interface Section):** See description of pin 39 D(7)
39	D(7)	I/O	**MSB of Bi-Directional Data Bus (Microprocessor Interface Section):** This pin, along with pins D0 - D6, function as the Microprocessor Interface bi-directional data bus, and is intended to be interfaced to the local microprocessor.
40	VDD	****	**Power Supply 3.3V ± 5%**
41	TxFrameRef	I	**Transmit Framer Reference Input:** This input pin functions as the Transmit Frame Generation reference signal, if the XRT72L50 has been configured to operate in the Local-Time/Frame Slave Mode. If the XRT72L50 has been configured to operate in the Local-Time/Frame-Slave Mode, then the user's terminal equipment is expected to apply a pulse (to this input pin) once every 106.4 microseconds (for DS3 applications); once every 125 microseconds (for E3, ITU-T G.832 applications) or once every 44.7 microseconds (for E3, ITU-T G.751 applications). In the Local-Time/Frame-Slave Mode, the Transmit Section of the XRT72L50 Framer IC will initiate its generation of a new outbound DS3 or E3 frame, upon the rising edge of this signal. ***NOTE:*** *The user can configure the XRT72L50 Framer IC to operate in the Local Time/Frame Slave Mode by writing xxxx xx01 into the Framer Operating Mode Register (Address = 0x00).*
42	GND	****	**Ground**
43	TxInClk	I	**Transmit Framer Reference Clock Input:** This input pin functions as the Timing Reference for the Transmit Section of the XRT72L50 Framer IC; if the device has been configured to operate in the Local-Time Mode. Further, if the XRT72L50 Framer IC has been configured to operate in the Local-Time Mode, the Transmit Payload Data Input Interface will sample the data at the TxSer input pin, upon the rising edge of TxInClk. For E3 applications, the user should apply a 34.368MHz clock signal. For DS3 applications, the user should apply a 44.736MHz clock signal. The user can configure the XRT72L50 Framer IC to operate in the Local-Time mode by writing xxxx xx01 or xxxx xx1x into the Framer Operating Mode register (Address = 0x00)
44	TxAISEn	I	**Transmit AIS Command Input:** Setting this input pin "High" configures the Transmit Section to generate and transmit an AIS Pattern. Setting this input pin "Low" configures the Transmit Section to generate E3 or DS3 traffic in a normal manner.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
45	TxSer/	I	**Transmit Serial Payload Data Input Pin:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. If the XRT72L50 Framer IC has been configured to operate in the Local Time Mode, then it will sample the data (on this pin) upon the rising edge of TxInClk. If the XRT72L50 Framer IC has been configured to operate in the Loop-Time Mode, then it will sample the data (on this pin) upon the rising edge of RxOutClk. ***NOTE:*** *This input pin is active only if the Serial Mode has been selected.* **Send Message:** This input is to remain "High" during the entire duration of the HDLC packet (including FCS bytes) to be transmitted, when the HDLC controller is turned on.
	SndMsg		
46	TxNib0/	I	**Transmit Nibble-Parallel Payload Data Input -0:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - 0:** This pin accepts bit 0 TxHDLC data when the HDLC controller is turned on.
	TxHDLCDat0		
47	TxNib1/	I	**Transmit Nibble-Parallel Payload Data Input -1:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - 1:** This pin accepts bit 1 TxHDLC data when the HDLC controller is turned on.
	TxHDLCDat1		
48	TxNib2/	I	**Transmit Nibble-Parallel Payload Data Input -2:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - 2:** This pin accepts bit 2 TxHDLC data when the HDLC controller is turned on.
	TxHDLCDat2		

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
49	TxNib3/ TxHDLCDat3	I	**Transmit Nibble-Parallel Payload Data Input -3:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound E3 or DS3 frame. The XRT72L50 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - 3:** This pin accepts bit 3 TxHDLC data when the HDLC controller is turned on.
50	GND	****	**Ground**
51	VDD	****	**Power Supply 3.3V ± 5%**
52	TxOHClk	O	**Transmit Overhead Clock:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface block will provide a rising clock edge on this signal, one bit-period prior to the start to the instant that the Transmit Overhead Data Input Interface block is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of this clock signal (provided that the TxOHIns input pin is "High"). ***NOTE:*** *The Transmit Overhead Data Input Interface block will supply a clock edge for all overhead bits within the DS3 or E3 frame (via the TxOHClk output signal). This includes those overhead bits that the Transmit Overhead Data Input Interface will not accept from the Terminal Equipment.*
53	TxOHIns/ TxHDLCDat4	I	**Transmit Overhead Data Insert Input:** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface will sample the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. Conversely, setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH input pin, on the falling edge of the TxOHClk output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal, at a time when one of these non-insertable overhead bits are being processed); that particular insertion effort will be ignored.* **Transmit HDLC Data Input - 4:** This pin accepts bit 4 TxHDLC data when the HDLC controller is turned on.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
54	TxOH/	I	**Transmit Overhead Input Pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the overhead bit position within the very next outbound DS3 or E3 frame. If the TxOHIns pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the TxOHClk output pin. Conversely, if the TxOHIns pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
	TxHDLCDat5		**Transmit HDLC Data Input - 5:** This pin accepts bit 5 TxHDLC data when the HDLC controller is turned on.
55	TxOHInd/	O	**Transmit Overhead Data Indicator:** This output pin will pulse "High" one-bit period prior to the time that the Transmit Section of the XRT72L50 will be processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that, during the very next bit-period, the XRT72L50 is going to be processing an Overhead bit and will be ignoring any data that is applied to the TxSer input pin. ***NOTE:*** *For DS3 applications, this output pin is only active if the XRT72L50 is operating in the Serial Mode. This output pin will be pulled "Low" if the device is operating in the Nibble-Parallel Mode.*
	TxHDLCDat6	I	**Transmit HDLC Data Input - 6:** This pin accepts bit 6 TxHDLC data when the HDLC controller is turned on.
56	TxOHEnable/	O	**Transmit Overhead Input Enable:** The XRT72L50 will assert this signal, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the Terminal Equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 frame, it is expected to sample the state of this signal, upon the falling edge of TxInClk. Upon sampling the TxOHEnable "High", the Terminal Equipment should (1) place the desired value of the overhead bit, onto the TxOH input pin and (2) assert the TxOHIns input pin. The Transmit Overhead Data Input Interface" block will sample and latch the data on the TxOH signal, upon the rising edge of the very next TxInClk input signal.
	TxHDLCDat7	I	**Transmit HDLC Data Input - 7:** This pin accepts bit 7 TxHDLC data when the HDLC controller is turned on.
57	TxOHFrame/	O	**Transmit Overhead Framing Pulse:** This output pin pulses "High" when the Transmit Overhead Data Input Interface block is expecting the first Overhead bit, within a DS3 or E3 frame to be applied to the TxOH input pin. This pin is "High" for one clock period of TxOHClk.
	TxHDLCClk		**Transmit HDLC Output Clock:** When the HDLC controller is on, TxHDLCDat is updated by the 72L53 by this clock signal.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
58	TxNibFrame/ ValFCS	O	**Transmit Frame Boundary Indicator - Nibble/Parallel Interface:** This output pin pulses "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNib[3:0] input pins. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to the XRT72L50. **Valid Frame Check Sequence:** When the HDLC is on, this pin will go "High" at the end of a valid Frame Check Sequence.
59	TxNibClk/ SndFCS	O I	**Transmit Nibble Clock Signal:** If the user opts to operate the XRT72L50 in the Nibble-Parallel mode, then the XRT72L50 will derive this clock signal from either the TxInClk or the RxLineClk signal (depending upon which signal is selected as the timing reference). The user is advised to configure the Terminal Equipment to output the outbound payload data (to the XRT72L50 Framer IC) onto the Tx-Nib[3:0] input pins, upon the rising edge of this clock signal. ***NOTES:*** *1. For DS3 applications, the XRT72L50 Framer IC will output 1176 clock edges (to the Terminal Equipment) for each outbound DS3 frame.* *2. For E3, ITU-T G.832 applications, the XRT72L50 Framer IC will output 1074 clock edges (to the Terminal Equipment) for each outbound E3 frame.* *3. For E3, ITU-T G.751 applications, the XRT72L50 Framer IC will output 384 clock edges (fo the Terminal Equipment) for each outbound E3 frame.* **Send Frame Check Sequence:** When the HDLC controller is turned on, this pin is driven "High" during the time when FCS bytes are being sent after a valid HDLC message.
60	GND	****	**Ground**
61	TxFrame	O	**Transmit End of DS3 or E3 Frame Indicator:** The Transmit Section of the XRT72l50 will pulse this output pin "High" (for one bit-period), when the Transmit Payload Data Input Interface is processing the last bit of a given DS3 or E3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to the XRT72l50 (e.g., to permit the XRT72l50 to maintain Transmit DS3/E3 framing alignment control over the Terminal Equipment).
62	VDD	****	**Power Supply 3.3V ± 5%**
63	TxLineClk	O	**Transmit Line Interface Clock:** This clock signal is output to the Line Interface Framer, along with the TxPOS and TxNEG signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The user can configure the source of this clock to be either the RxLineClk (from the Receiver portion of the Framer) or the TxInClk input. The nominal frequency of this clock signal is 34.368 MHz.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
64	TxNEG	O	**Transmit Negative Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output signal pulses "High" for one bit period, at the end of each outbound DS3 or E3 frame. This output signal is at a logic "Low" for all of the remaining bit-periods of the outbound DS3 or E3 frames **Bipolar Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNDATA input of the external DS3/E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.
65	TxPOS	O	**Transmit Positive Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. Unipolar Mode: This output pin functions as the Single-Rail output signal for the outbound DS3 or E3 data stream. The signal, at this output pin, will be updated on the user-selected edge of the TxLineClk signal. Bipolar Mode: This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPDATA input of the external DS3 or E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line
66	ENCODIS	O	**Encoder (HDB3) Disable Output pin (intended to be connected to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the ENDECDIS input pin of the XRT73L00 DS3/E3 Line Interface Unit IC when the device is being used in Hardware mode. The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (Encodis) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "High" then it will disable the B3ZS/HDB3 encoder circuitry within the XRT73L00 IC. Conversely, if the user commands this output signal to toggle "Low", then the B3ZS/HDB3 Encoder circuitry, within the XRT73L00 IC will be enabled. The user is advised to disable the B3ZS/HDB3 encoder (within the XRT73L00 IC) if the XRT72L50 Framer IC has been configured to operate in the B3ZS/HDB3 line code. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
67	TxLEV	O	**Transmit Line Build-Out Enable/Disable Select Output (to be connected to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the TxLev input pin of the XRT73L00 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 0x80). **For DS3 Application:** If the user commands this signal to toggle "High" then the Transmit Line Build-Out circuit (within the XRT73L00) will be disabled. In this mode, the XRT73L00 will output unshaped (e.g., square) pulses onto the line (via the TTIP and TRING output pins). Conversely, if the user commands this signal to toggle "Low" then the Transmit Line Build-Out circuit (within the XRT73L00) will be disabled. In this mode, the XRT73L00 will output shaped (e.g., more rounded) pulses onto the line (via the TTIP and TRING output pins). In order to comply with the DSX-3 Isolated Pulse Template Requirement (per Bellcore GR-499-CORE), the user is advised to command this output pin to be "High" if the cable length (between the transmit output of the XRT73L00 and the DSX-3 Cross-Connect System) is greater than 225 feet. Conversely, the user is advised to command this output pin to be "Low" if the cable length (between the transmit output of the XRT73L00 and the DSX-3Cross Connect System) is less than 225 feet. **For E3 Applications:** This pin can be used as a General Purpose Output pin. The Transmit Line Build-Out circuitry (within the XRT73L00) is not active for E3 applications. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*
68	TAOS	O	**Transmit All Ones Signal (TAOS) Command (for the XRT73L00 Line Interface Unit IC):** This output pin is intended to be connected to the TAOS input pin of the XRT73L00 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 4 (TAOS) of the Line Interface Drive Register (Address = 0x80). If the user commands this signal to toggle "High" then it will force the XRT73L00 Line Interface Unit IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "Low" then the XRT73L00 DS3/E3 Line Interface Unit IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins. ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*
69	LLOOP	O	**Local Loopback Output Pin (to the XRT73L00 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the LLOOP input pin of the XRT73L00 LIU IC. The user can command this signal to toggle "High" and, in turn, force the LIU into the Local Loop-back mode. (For a detailed description of the XRT73L00 DS3/E3 Line Interface Unit IC's operation during Local Loopback, please see the XRT73L00 DS3/STS-1/E3 Line Interface Unit IC's Data Sheet). ***NOTE:*** *If the customer is not using the XRT73L00 DS3/E3 Line Interface Unit IC, then this output pin may be used for other purposes.*