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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

GENERAL DESCRIPTION

The XRT72L52, Two Channel DS3/E3 Framer IC is designed to accept user data from the Terminal Equipment and insert this data into the payload bit-fields within an outbound DS3/E3 Data Stream. Further, the Framer is also designed to receive an inbound DS3/E3 Data Stream from the Remote Terminal Equipment and extract out the user data.

The XRT72L52 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L52 DS3/E3 Framer IC consists of a Transmit section, Receiver section, Performance Monitor Section and a Microprocessor interface.

The Transmit Section includes a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Section consists of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of Reset-upon-Read and Read-Only registers that contain cumulative and one-second statistics that reflect the performance/health of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 1 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 160 Pin PQFP package
- 3.3V Power Supply with 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT72L52

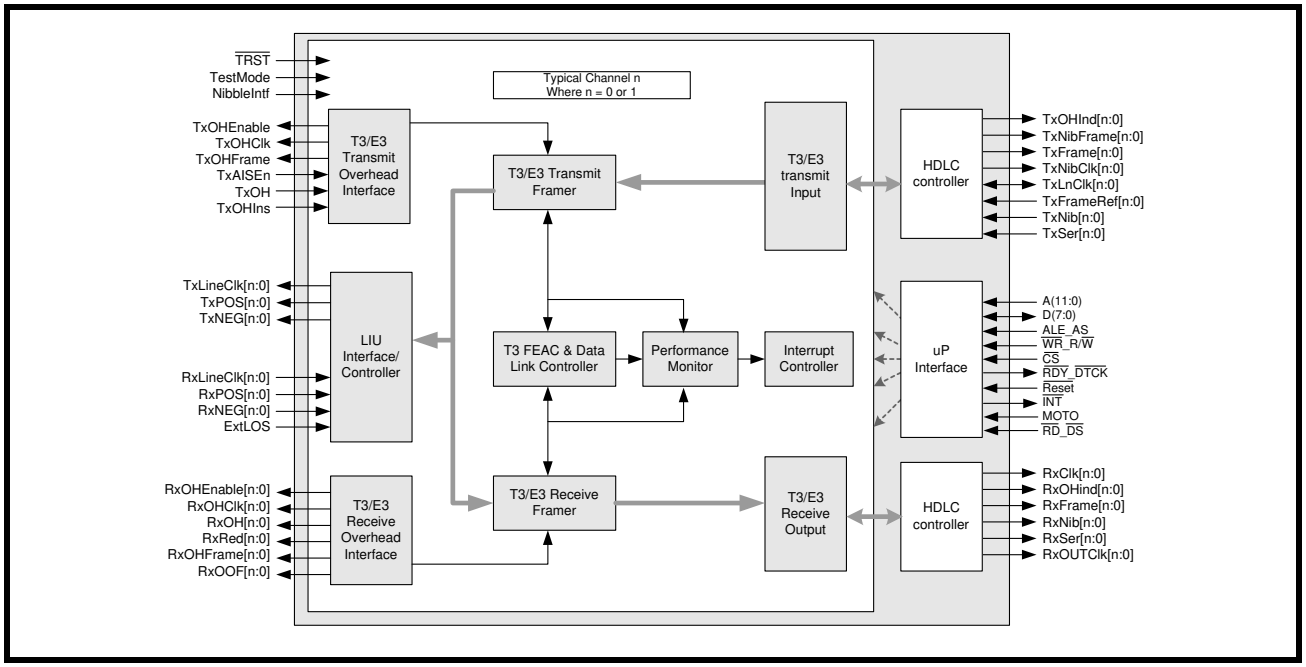
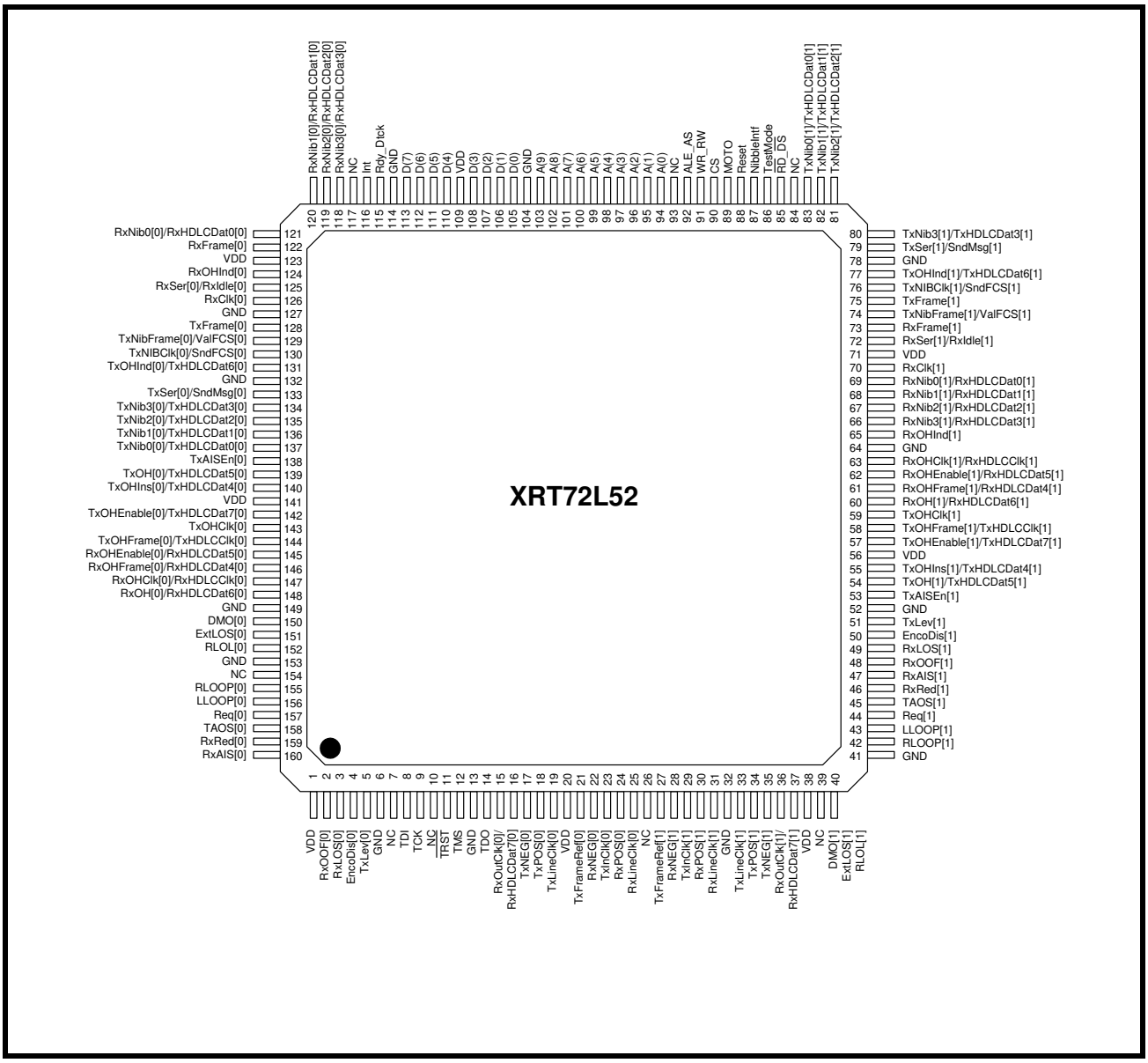


FIGURE 2. PIN OUT OF THE XRT72L52



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT72L52IQ	28x28mm 160 lead plastic QFP	-40°C to +85°C

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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDD	****	**Power Supply 3.3V ± 5%**
2	RxOOF[0]	O	**Receiver Out of Frame Indicator:** The Receive Section of the XRT72L52 Framer asserts this output signal whenever it has declared an Out of Frame (OOF) condition with the incoming DS3 or E3 frames. This signal is negated when the framer locates the framing alignment bits or bytes and correctly aligns itself with the incoming DS3 or E3 frames.
3	RxLOS[0]	O	**Receive Section - Loss of Signal Output Indicator:** This pin is asserted when the Receive Section encounters a string of 180 consecutive “0’s” for DS3 operation or 32 consecutive “0's” for E3 operation via the RxPOS and RxNEG pins. This pin is negated once the Receive Section has detected at least 60 pulses within 180 bit-periods for DS3 operation or the Receive Section has detected a string of 32 consecutive bits that does not contain a string of 4 consecutive 0’s, for E3 operation.
4	EncoDis[0]	O	**Encoder (HDB3) Disable Output pin (intended to be connected to the XRT73L0x DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the ENDECDIS input pin of the XRT73L0x DS3/E3 Line Interface Unit IC when the device is being used in Hardware mode. The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (Encodis) within the Line Interface Driver Register (Address = 0x80). If this signal is toggled "High" then it disables the B3ZS/HDB3 encoder circuitry within the XRT73L0x IC. If this output signal is toggled "Low", then the B3ZS/HDB3 Encoder circuitry within the XRT73L0x IC is enabled. If the XRT72L52 Framer has been configured to operate in the B3ZS/HDB3 line code, disable the B3ZS/HDB3 encoder within the XRT73L0x IC. ***NOTE:*** *If the XRT73L0x DS3/E3 Line Interface Unit IC is not used, this output pin may be used for other purposes.*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
5	TxLev[0]	O	**Transmit Line Build-Out Enable/Disable Select Output (to be connected to the XRT73L0x DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the TxLev input pin of the XRT73L0x DS3/E3 Line Interface Unit IC. To control the state of this output pin, write a "0" or "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 0x80). **For DS3 Application:** If the user toggleds this signal"High", then the Transmit Line Build-Out circuit within the XRT73L0x is disabled. In this mode, the XRT73L0x outputs unshaped (e.g., square) pulses onto the line via the TTIP and TRING output pins. If the user toggleds this signal "Low", then the Transmit Line Build-Out circuit within the XRT73L0x is disabled. In this mode, the XRT73L0x outputs shaped (e.g., more rounded) pulses onto the line via the TTIP and TRING output pins. In order to comply with the DSX-3 Isolated Pulse Template Requirement per Bellcore GR-499-CORE, command this output pin to be "High" if the cable length between the transmit output of the XRT73L0x and the DSX-3 Cross-Connect System is greater than 225 feet. If the cable length is less than 225 feet, command this output pin to be "Low". **For E3 Applications:** This pin can be used as a General Purpose Output pin. The Transmit Line Build-Out circuitry within the XRT73L0x is not active for E3 applications. ***NOTE:*** *If the XRT73L0x DS3/E3 Line Interface Unit IC is not used, this output pin may be used for other purposes.*
6	GND	****	**Ground**
7	NC		
8	TDI	I	**Test Data In:** Boundary Scan Test data input.
9	TCK	I	**Test Clock:** Boundary Scan clock input.
10	NC		
11	$\overline{\text{TRST}}$	I	**JTAG Reset Pin:** Resets Boundary Scan Logic.
12	TMS	I	**Test Mode Select:** Boundary Scan Mode Select input.
13	GND	****	**Ground**
14	TDO	O	**Test Data Out:** Boundary Scan test data output.
15	RxOutClk[0]/ RxHDLCDat7[0]	O	**Receive Out Clock - Transmit Terminal Interface Clock for Loop-Timing:** This clock signal functions as the Terminal Interface clock source if the XRT72L52 Framer is operating in the loop-timing mode. In this mode, the Transmitting Terminal Equipment is expected to input data to the Framer, via the TxSer input pin, upon the rising edge of this clock signal. The XRT72L52 uses the rising edge of this clock signal to sample the data at the TxSer input. This clock signal is a buffered version of the RxLineClk signal. **Receive HDLC Data Output - 7:** This pin contains bit 7 RxHDLC data when the HDLC controller is on.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
16	TxNEG[0]	O	**Transmit Negative Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output signal pulses "High" for one bit period at the end of each outbound DS3 or E3 frame. This output signal is at a logic "Low" for all of the remaining bit-periods of the outbound DS3 or E3 frames **Bipolar Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNDATA input of the external DS3/E3 Line Interface Unit IC. When this output is asserted, it commands the LIU to generate a negative polarity pulse on the line.
17	TxPOS[0]	O	**Transmit Positive Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output pin functions as the Single-Rail output signal for the outbound DS3 or E3 data stream. The signal at this output pin is updated on the user-selected edge of the TxLineClk signal. **Bipolar Mode:** This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPDATA input of the external DS3 or E3 Line Interface Unit IC. When this output is asserted, it commands the LIU to generate a positive polarity pulse on the line
18	TxLineClk[0]	O	**Transmit Line Interface Clock:** This clock signal is output to the Line Interface Framer along with the TxPOS and TxNEG signals. This output clock signal provides the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The source of this clock can be configured to be either the RxLineClk from the Receiver portion of the Framer or the TxInClk input. The nominal frequency of this clock signal is 34.368 MHz.
19	VDD	****	**Power Supply 3.3V ± 5%**
20	TxFrameRef[0]	I	**Transmit Framer Reference Input:** This input pin functions as the Transmit Frame Generation reference signal if the XRT72L52 has been configured to operate in the Local-Time/Frame Slave Mode. If the XRT72L52 has been configured to operate in the Local-Time/Frame-Slave Mode, then the user's terminal equipment is expected to apply a pulse to this input pin once every 106.4 microseconds for DS3 applications, once every 125 microseconds for E3, ITU-T G.832 applications or once every 44.7 microseconds for E3, ITU-T G.751 applications. In the Local-Time/Frame-Slave Mode, the Transmit Section of the XRT72L52 Framer initiates its generation of a new outbound DS3 or E3 frame upon the rising edge of this signal. ***NOTE:*** *To configure the XRT72L52 Framer to operate in the Local Time/Frame Slave Mode, write "xxxx xx01" into the Framer Operating Mode Register (Address = 0x00).*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
21	RxNEG[0]	I	**Receive Negative Data Input:** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin is inactive and should be pulled "Low" or "High" when the Framer is operating in the Unipolar Mode. **Bipolar Mode:** This input pin functions as one of the dual rail inputs for the incoming AMI/HDB3 encoded DS3 or E3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS functions as the other dual rail input for the Framer. When this input pin is asserted, the LIU has received a negative polarity pulse from the line.
22	TxInClk[0]	I	**Transmit Framer Reference Clock Input:** This input pin functions as the Timing Reference for the Transmit Section of the XRT72L52 Framer if the device has been configured to operate in the Local-Time Mode. If the XRT72L52 Framer has been configured to operate in the Local-Time Mode, the Transmit Payload Data Input Interface samples the data at the TxSer input pin upon the rising edge of TxInClk. For E3 applications, apply a 34.368MHz clock signal. For DS3 applications, apply a 44.736MHz clock signal. ***NOTE:*** *To configure the XRT72L52 Framer to operate in the Local-Time mode, write "xxxx xx01" or "xxxx xx1x" into the Framer Operating Mode register (Address = 0x00).*
23	RxPOS[0]	I	**Receive Positive Data Input:** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin functions as the Single-Rail input for the incoming E3 data stream. The signal at this input pin is sampled and latched into the Receive DS3/E3 Framer on the user-selected edge of the RxLineClk signal. **Bipolar Mode:** This input functions as one of the dual rail inputs for the incoming AMI/HDB3 encoded DS3 or E3 data that has been received from an external Line Interface Unit (LIU) IC. RxNEG functions as the other dual rail input for the Framer. When this input pin is asserted, the LIU has received a positive polarity pulse from the line.
24	RxLineClk[0]	I	**Receiver LIU (Recovered) Clock:** This input signal serves three purposes: 1. The Receive Framer uses it to sample and latch the signals at the RxPOS and RxNEG input pins into the Receive Framer circuitry. 2. This input signal functions as the timing reference for the Receive Framer block. 3. The Transmit Framer block can be configured to use this input signal as its timing reference. This signal is the recovered clock from the external DS3/E3 LIU (Line Interface Unit) IC, which is derived from the incoming DS3/E3 data.
25	NC		
26	TxFrameRef[1]	I	See Description for Pin 20

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
27	RxNEG[1]	I	See Description for Pin 21
28	TxInClk[1]	I	See Description for Pin 22
29	RxPOS[1]	I	See Description for Pin 23
30	RxLineClk[1]	I	See Description for Pin 24
31	GND	****	**Ground**
32	TxLineClk[1]	O	See Description for Pin 18
33	TxPOS[1]	O	See Description for Pin 17
34	TxNEG[1]	O	See Description for Pin 16
35	RxOutClk[1]/ RxHDLCDat7[1]	O	See Description for Pin 15
36	VDD	****	**Power Supply 3.3V ± 5%**
37	NC		
38	DMO[1]	I	See Description for Pin 150
39	ExtLOS[1]	I	See Description for Pin 151
40	RLOL[1]	I	**Receive Loss of Lock Indicator - from the XRT73L0x DS3/E3 Line Interface Unit IC:** This input pin is intended to be connected to the RLOL output pin of the XRT73L0x Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 0x81). If this input pin is "Low", then the clock recovery phase-locked-loop circuitry within the XRT73L0x is properly locked onto the incoming DS3 E3 data-stream and is properly recovering clock and data from this DS3/E3 data-stream. If this input pin is "High", then the phase-locked-loop circuitry within the XRT73L0x has lost lock with the incoming DS3 or E3 data-stream and is not properly recovering clock and data. For more information on the operation of the XRT73L0x DS3/E3 Line Interface Unit IC, please consult the XRT73L0x DS3/E3 Line Interface Unit data sheet. ***NOTE:*** *If the XRT73L0x DS3/E3 Line Interface Unit IC is not used, this input pin can be used for other purposes.*
41	GND	****	**Ground**
42	RLOOP[1]	O	See Description for Pin 155
43	LLOOP[1]	O	See Description for Pin 156
44	$\overline{\text{Req}}$[1]	O	See Description for Pin 157
45	TAOS[1]	O	See Description for Pin 158
46	RxRed[1]	O	See Description for Pin 159
47	RxAIS[1]	O	See Description for Pin 160
48	RxOOF[1]	O	See Description for Pin 2
49	RxLOS[1]	O	See Description for Pin 3

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
50	EncoDis[1]	O	See Description for Pin 4
51	TxLev[1]	O	See Description for Pin 5
52	GND	****	**Ground**
53	TxAISEn[1]	I	See Description for Pin 138
54	TxOH[1]/ TxHDLCDat5[1]	I	See Description for Pin 139
55	TxOHIns[1]/ TxHDLCDat4[1]	I	See Description for Pin 140
56	VDD	****	**Power Supply 3.3V ± 5%**
57	TxOHEnable[1]/ TxHDLCDat7[1]	O I	See Description for Pin 142
58	TxOHFrame[1]/ TxHDLCClk[1]	O	See Description for Pin 144
59	TxOHClk[1]	O	See Description for Pin 143
60	RxOH[1]/ RxHDLCDat6[1]	O	See Description for Pin 148
61	RxOHFrame[1]/ RxHDLCDat4[1]	O	See Description for Pin 146
62	RxOHEnable[1]/ RxHDLCDat5[1]	O	See Description for Pin 145
63	RxOHClk[1]/ RxHDLCClk[1]	O	See Description for Pin 147
64	GND	****	**Ground**
65	RxOHInd[1]	O	See Description for Pin 124
66	RxNib3[1]/ RxHDLCDat3[1]	O	See Description for Pin 118
67	RxNib2[1]/ RxHDLCDat2[1]	O	See Description for Pin 119
68	RxNib1[1]/ RxHDLCDat1[1]	O	See Description for Pin 120
69	RxNib0[1]/ RxHDLCDat0[1]	O	See Description for Pin 121
70	RxClk[1]	O	See Description for Pin 126
71	VDD	****	**Power Supply 3.3V ± 5%**
72	RxSer[1]/ RxIdle[1]	O	See Description for Pin 125
73	RxFrame[1]	O	See Description for Pin 122

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
74	TxNibFrame[1]/ ValFCS[1]	O	See Description for Pin 129
75	TxFrame[1]	O	See Description for Pin 128
76	TxNIBClk[1]/ SndFCS[1]	O I	See Description for Pin 130
77	TxOHInd[1]/ TxHDLCDat6[1]	O I	See Description for Pin 131
78	GND	****	**Ground**
79	TxSer[1]/ SndMsg[1]	I	See Description for Pin 133
80	TxNib3[1]/ TxHDLCDat3[1]	I	See Description for Pin 134
81	TxNib2[1]/ TxHDLCDat2[1]	I	See Description for Pin 135
82	TxNib1[1]/ TxHDLCDat1[1]	I	See Description for Pin 136
83	TxNib0[1]/ TxHDLCDat0[1]	I	See Description for Pin 137
84	NC		
85	$\overline{RD}$_$\overline{DS}$	I	**Read Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this input functions as the $\overline{RD}$ (READ STROBE) input signal from the local µP. Once this active-low signal is asserted, then the Framer places the contents of the addressed registers within the Framer on the Microprocessor Data Bus (D(7:0). When this signal is negated, the Data Bus is tri-stated. **Data Strobe (Motorola Mode):** If the microprocessor interface is operating in the Motorola mode, then this pin functions as the active-low Data Strobe signal.
86	TestMode	***	**Factory Test Pin:** This pin should be tied to Ground.