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THREE CHANNEL DS3/E3 FRAMER IC WITH HDLC CONTROLLER

MAY 2001 REV. P1.1.8

GENERAL DESCRIPTION

The XRT72L53, 3 Channel DS3/E3 Framer IC is designed to accept User Data from the Terminal Equipment and insert this data into the Payload bit-fields within an Outbound DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an Inbound DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the User Data.

The XRT72L53 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 (November 1995 and October 1998 Revisions) Framing Formats.

The XRT72L53 DS3/E3 Framer IC consists of three Transmit sections, three Receiver sections, three Performance Monitor Sections and a Microprocessor interface.

The Transmit Sections, include a Transmit Payload Data Input Interface block, a Transmit Overhead Data Input Interface block, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which allows the Terminal Equipment to transmit data to a remote terminal.

The Receive Sections, consist of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of Reset-upon-Read and Read-Only registers that contain cumulative and One-Second statistics that reflect the performance/health of the three channels of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 3 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 272 Ball PBGA package
- 3.3V Power Supply, 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT72L53

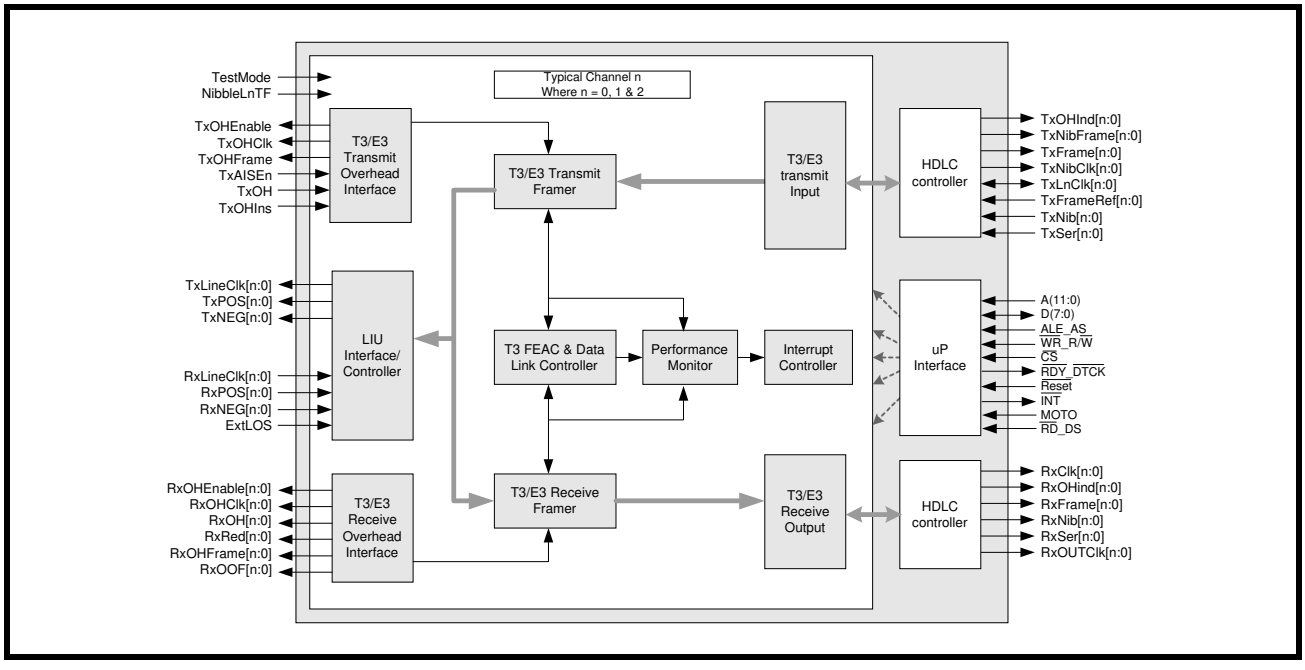
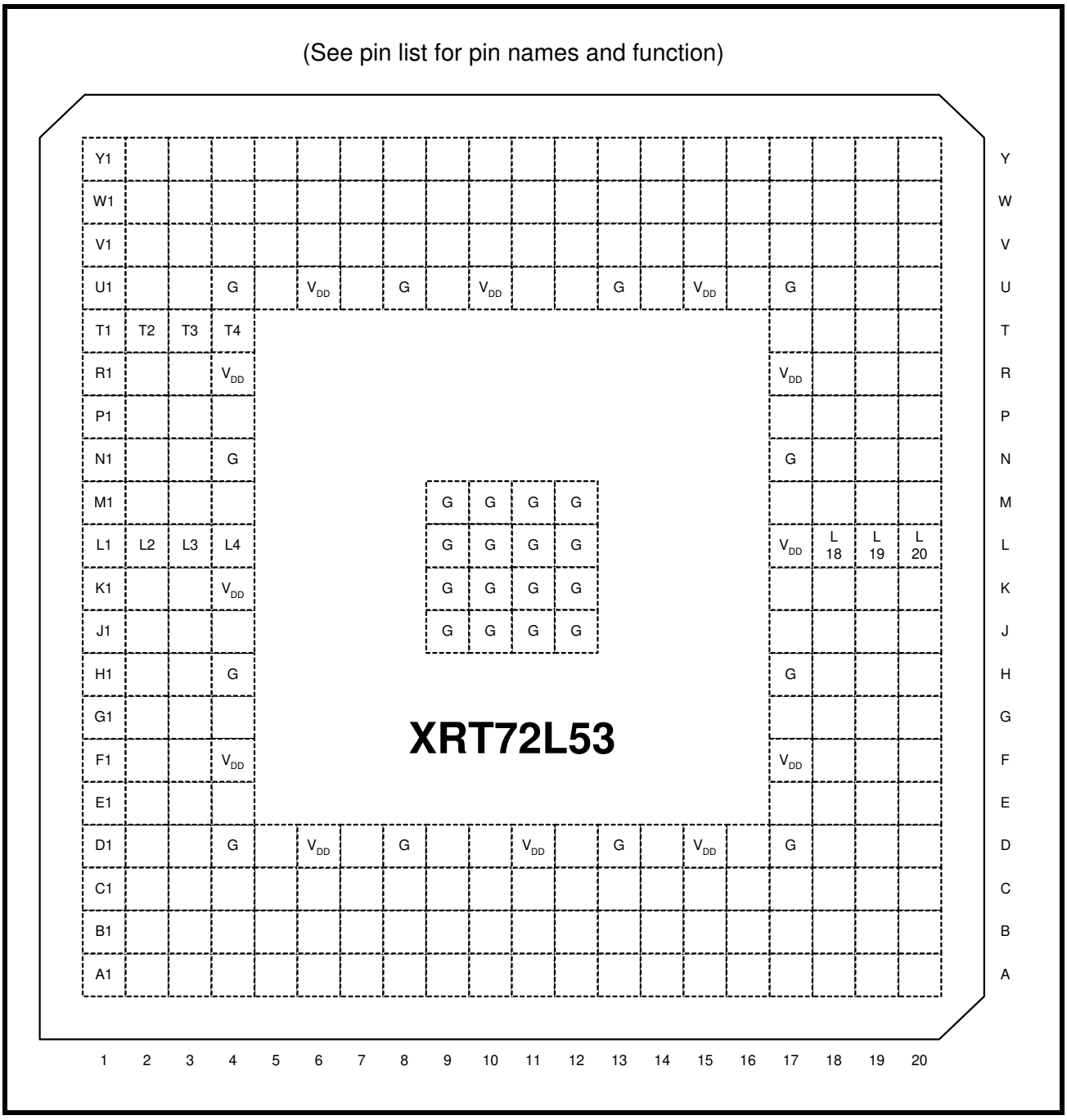


FIGURE 2. PIN OUT OF THE XRT72L53



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT72L53	27x27 mm 272 Ball PBGA	-40°C to +85°C

PIN DESCRIPTIONS

PIN DESCRIPTION NO CONNECTION PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
J18	NC	*****	**No Connection** **The pins listed here are not connected in the XRT72L53.**
K1	NC		
K2	NC		
L2	NC		
L4	NC		
L19	NC		
M2	NC		
M4	NC		
N2	NC		
P1	NC		
P4	NC		
R1	NC		
R2	NC		
T2	NC		
T4	NC		
U1	NC		
U2	NC		
U7	NC		
U16	NC		
U18	NC		
V2	NC		
V3	NC		
V4	NC		
V5	NC		
V8	NC		
V9	NC		
V10	NC		
V11	NC		
V12	NC		
V13	NC		
V14	NC		
V15	NC		
V18	NC		
V19	NC		
W7	NC		
W14	NC		
W17	NC		
W18	NC		
Y1	NC		
Y2	NC		
Y3	NC		
Y5	NC		
Y6	NC		
Y8	NC		
Y9	NC		
Y11	NC		
Y12	NC		
Y13	NC		
Y16	NC		
Y17	NC		
Y20	NC		

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
A1	TxLev[1]	O	**Transmit Line Build-Out Enable/Disable Select output pin - Channel 1:** See Description for Pin C3
A2	EncoDis[1]	O	**HDB3/B3ZS Encoder Enable/Disable output pin - Channel 1:** See Description for Pin B2
A3	RxOOF[0]	O	**Receive Out of Frame Indicator - Channel 0:** The Receive Section of Channel 0, within the XRT72L53 Framer IC will assert this output signal whenever it has declared an Out of Frame (OOF) condition with the incoming DS3 or E3 frames. This signal is negated when the framer correctly locates the framing alignment bits or bytes and correctly aligns itself with the incoming DS3 or E3 frames.
A4	RxRed[1]	O	**Receive Red Alarm Indicator - Channel 1:** See Description for Pin B5
A5	$\overline{\text{REQ}}$[0]	O	**Receive Equalization Enable/Disable Select output pin - Channel 0- (to be connected to the DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to either the $\overline{\text{REQ}}$, REQDIS or REQEN input pin of the DS3/E3 LIU. The user can control the state of this output pin by writing a '0' or '1' to Bit 5 ($\overline{\text{REQ}}$) within the Line Interface Driver Register (Address = 0x80). This output pin permits the user to have control over the state of the Receive Equalizer block(s) within the corresponding DS3/E3 LIU IC. Writing a "1" to Bit 5 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTE:*** *This output pin can also be used as a "General Purpose Output" pin.*
A6	LLOOP[1]	O	**Local Loop-back Output pin - Channel 1 (to be connected to the LLOOP input pin of the DS3/E3 LIU IC):** See Description for Pin C7
A7	RLOOP[1]	O	**Remote Loop-back Output pin - Channel 1 (to be connected to the RLOOP input pin of the DS3/E3 LIU IC):** See Description for Pin B7
A8	ExtLOS[1]	I	**Receive LOS (Loss of Signal) Input - Channel 1:** See Description for Pin D9
A9	RxOHClk[1]/ RxHDLCClk[1]	O	**Receive Overhead Data Output Clock signal/Receive HDLC Controller Output Clock signal - Channel 1:** See Description for Pin D12
A10	TxOHClk[1]	O	**Transmit Overhead Clock Output - Channel 1:** See Description for Pin A14
A11	TxOHFrame[1]/ TxHDLCClk[1]	O	**Transmit Overhead Framing Pulse/Transmit HDLC Controller Output clock signal - Channel 1:** See Description for Pin C13
A12	TxOH[1]/ TxHDLCDat5[1]	I	**Transmit Overhead Input pin/Transmit HDLC Controller Data Input - Bit 5 (Channel 1):** See Description for Pin A15

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
A13	RxOHFrame[0]/ RxHDLCDat4[0]	O	**Receive Overhead Frame Boundary Indicator/Receive HDLC Controller Data Output - Bit 4** The exact functionality of this output pin depends upon whether Channel 0 has been configured to operate in the "High Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Receive Overhead Frame Boundary Indicator:** This output pin pulses "High" whenever the Receive Overhead Data Output Interface" block outputs the first overhead bit (or nibble) of a new DS3 or E3 frame. **High Speed HDLC Controller Mode - Receive HDLC Data Output - Bit 4:** This pin functions as bit 4, within the byte-wide Receive HDLC Controller output interface (RxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High Speed HDLC Controller" Mode.
A14	TxOHClk[0]	O	**Transmit Overhead Clock output - Channel 0:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface block will provide a rising clock edge on this signal, one bit-period prior to the start to the instant that the "Transmit Overhead Data Input Interface" block (associated with Channel 1) is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the "TxOH[0]" input pin, on the falling edge of this clock signal (provided that the "TxOHIns[0]" input pin is "HIGH"). ***NOTE:*** *The Transmit Overhead Data Input Interface block will supply a clock edge for all overhead bits within the DS3 or E3 frame (via the "TxOHClk[0]" output signal). This includes those overhead bits that the "Transmit Overhead Data Input Interface" will not accept from the Terminal Equipment.*
A15	TxOH[0]/ TxHDLCDat5[0]	I	**Transmit Overhead Input Pin/Transmit HDLC Controller Data Input - Bit 5 (Channel 0):** The exact functionality of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Transmit Overhead Input pin - Channel 0:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the overhead bit position within the very next outbound DS3 or E3 frame. If the TxOHIns pin is pulled "High", then the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH[0]), on the falling edge of the TxOHClk[0] output pin. Conversely, if the TxOHIns[0] pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH[0]). Consequently, this data will be ignored. **High Speed HDLC Controller Mode - Transmit HDLC Data Input - Bit 5:** This pin functions as bit 5, within the byte-wide Transmit HDLC Controller input interface (TxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High Speed HDLC Controller" Mode.

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
A16	TxNib2[1]/ TxHDLCDat2[1]	I	**Transmit Nibble-Parallel Data Input - Bit 2/Transmit HDLC Data Input - Bit 2; Channel 1:** See Description for Pin C20
A17	RxSer[1]/ RxIdle[1]	O	**Receive Serial Output/Receive Flag Sequence Indicator - Channel 1:** See Description for Pin F19
A18	TxOHInd[1]/ TxHDLCDat6[1]	O I	**Transmit Overhead Data Indicator output/Transmit HDLC Data Input - Bit 6; Channel 1:** See Description for Pin E19
A19	RxOHInd[1]	O	**Receive Overhead Bit Indicator output - Channel 1:** See Description for Pin G18
A20	RxClk[1]	O	**Receive Clock Output signal for Serial and Nibble-Parallel Data Interface - Channel 1:** See Description for Pin D20
B1	TDI	I	**Test Data In:** Boundary Scan Test data input.
B2	EncoDis[0]	O	**Encoder (HDB3/B3ZS) Disable Output pin - Channel 0 (intended to be connected to either the ENCODIS or the ENDECDIS input to the DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to either the Encodis or ENDECDIS input pin of the DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (Encodis) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "High" then it will disable the B3ZS/HDB3 encoder circuitry within the DS3/E3 LIU IC. Conversely, if the user commands this output signal to toggle "Low", then the B3ZS/HDB3 Encoder circuitry, within the DS3/E3 LIU IC will be enabled. Writing a "1" to Bit 3 of the Line Interface Driver Register (Address = 0x80) will cause this output pin to toggle "High". Writing a "0" to this bitfield will cause this output pin to toggle "Low". The user is advised to disable the B3ZS/HDB3 encoder (within the DS3/E3 LIU IC) if Channel 0, within the XRT72L53 Framer IC has been configured to operate in the B3ZS/HDB3 line code. ***NOTE:*** *.This output pin can be used as a "General Purpose" Output pin.*
B3	RxLOS[1]	O	**Receive LOS (Loss of Signal) Indicator Output - Channel 1:** See Description for Pin C4
B4	RxAIS[1]	O	**Receive AIS (Alarm Indication Signal) Indicator Output - Channel 1:** See Description for Pin C5
B5	RxRed[0]	O	**Receive Red Alarm Indicator Output - Channel 0:** The Framer toggles this output pin "high" to denote that one of the following events has been detected by the Receive Framer block, within Channel 0: LOS - Loss of Signal Condition OOF - Out of Frame Condition AIS - Alarm Indication Signal Detection

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
B6	$\overline{\text{Req}}$[1]	O	**Receive Equalization Enable/Disable Select output pin - Channel 1:** See Description for Pin A5
B7	RLOOP[0]	O	**Remote Loopback Output Pin - Channel 0 (to be connected to DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the RLOOP input pin of the DS3/E3 Line Interface Unit IC. The user can command this signal to toggle "High" and, in turn, force the DS3/E3 Line Interface Unit IC into either the Remote or Digital Local- Loopback modes (depending upon the state of the LLOOP[0] pin. Conversely, the user can command this signal to toggle "Low" and allow the XRT7300 device to operate in the normal mode. Writing a "1" to bit 1 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause the RLOOP output to toggle "Low". ***NOTE:*** *This output pin can be used as a General Purpose Output pin.*
B8	RLOL[0]	I	**Receive Loss of Lock Indicator input pin - Channel 0 (from the DS3/E3 Line Interface Unit IC):** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the DS3/E3 Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 0x81). If this input pin is "Low", then it means that the clock recovery phase-locked-loop circuitry, within the LIU device is properly locked onto the incoming DS3 E3 data-stream; and is properly recovering clock and data from this DS3/E3 data-stream. However, if this input pin is "High", then it means that the phase-locked-loop circuitry, within the LIU device has lost lock with the incoming DS3 or E3 data-stream, and is not properly recovering clock and data. If the customer is not using an “Exar XRT73L0X Family of DS3/E3 LIU ICs, then this input pin can be used for other purposes.
B9	DMO[1]	I	**Drive Monitor Output input pin - Channel 1 (from the DS3/E3 LIU IC):** See Description for Pin C9
B10	RxOH[1]/ RxHDLCDat6[1]	O	**Receive Overhead Data Output port/Receive HDLC Data Output - Bit 6; Channel 1:** See Description for Pin C12
B11	TxOHIns[1]/ TxHDLCDat4[1]	I	**Transmit Overhead Data Insert Input/Transmit HDLC Data Input - Bit 4 - Channel 1:** See Description for Pin C14
B12	TxAISEn[1]	I	**Transmit AIS Command Input - Channel 1:** See Description for Pin B15

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
B13	RxOHEnable[0]/ RxHDLCDat5[0]	O	**Receive Overhead Enable Indicator/Receive HDLC Controller Data Output - Bit 5; Channel 0:** The exact functionality of this output pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Receive Overhead Enable Indicator - Channel 0:** The XRT72L53 will assert this output signal for one "RxOutClk" period when it is safe for the Terminal Equipment to sample the data on the "RxOH" output pin. **High-Speed HDLC Controller Mode - Receive HDLC Controller Data Ouptut - Bit 5, Channel 0:** This pin functions as bit 5, within the byte-wide Receive HDLC Controller output interface (RxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
B14	TxOHEnable[0]/ TxHDLCDat7[0]	O I	**Transmit Overhead Input Enable/Transmit HDLC Controller Data Output - Bit 7; Channel 0:** The exact functionality of this bit-field depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Transmit Overhead Input Enable Output - Channel 0:** Channel 0, within the XRT72L53 device, will assert this signal, for one "TxInClk[0]" period, just prior to the instant that the "Transmit Overhead Data Input Interface" will be sampling and processing an overhead bit. If the Terminal Equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 frame, it is expected to sample the state of this signal, upon the falling edge of "TxInClk". Upon sampling the "TxOHEnable" high, the Terminal Equipment should (1) place the desired value of the overhead bit, onto the "TxOH" input pin and (2) assert the "TxOHIns" input pin. The Transmit Overhead Data Input Interface" block will sample and latch the data on the "TxOH" signal, upon the rising edge of the very next "TxInClk" input signal. **High-Speed HDLC Controller Mode - Transmit HDLC Data Input - Bit 7; Channel 0:** This pin functions as bit 5, within the byte-wide Transmit HDLC Controller input interface (TxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
B15	TxAISEn[0]	I	**Transmit AIS Command Input - Channel 0:** Setting this input pin "High" configures the Transmit Section of Channel 0 to generate and transmit an AIS Pattern. Setting this input pin "Low" configures the Transmit Section to generate E3 or DS3 traffic in a normal manner.
B16	TxNib3[1]/ TxHDLCDat3[1]	I	**Transmit Nibble-Parallel Payload Data Input - Bit 3/Transmit HDLC Data Input - Bit 3; Channel 1:** See Description for Pin D19

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
B17	TxNibFrame[1]/ ValFCS[1]	O	**Transmit Frame Boundary Indicator - Nibble-Parallel Interface/ Transmit HDLC - VALID FRAME CHECK SEQUENCE Indicator - Channel 1:** See Description for Pin G17
B18	RxFrame[1]	O	**Receive Boundary of DS3 or E3 Frame Output Indicator - Channel 1:** See Description for Pin F20
B19	RxNib0[1]/ RxHDLCDat0[1]	O	**Receive Nibble Output - Bit 0/Receive HDLC Data Output - Bit 0; Channel 1:** See Description for Pin G19
B20	RxNib2[1]/ RxHDLCDat2[1]	O	**Receive Nibble Output - Bit 2/Receive HDLC Data Output - Bit 2; Channel 1:** See Description for Pin H18
C1	TxPOS[0]	O	**Transmit Positive Polarity Pulse output - Channel 0:** The exact role of this output pin depends upon whether Channel 0 is operating in the Single-Rail or Dual-Rail Mode. **Single-Rail Mode:** This output pin functions as the Single-Rail output signal for the outbound DS3 or E3 data stream. The signal, at this output pin, will be updated on the user-selected edge of the TxLineClk signal. **Dual-Rail Mode:** This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG[0] is the other output pin. This input is typically connected to the TPDATA input of the external DS3 or E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line
C2	TCK	I	**Test Clock:** Boundary Scan clock input.

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
C3	TxLev[0]	O	**Transmit Line Build-Out Enable/Disable Select Output - Channel 0 (to be connected to the DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the TxLev input pin of the DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 0x80). Writing a "1" to Bit 2 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". **For DS3 Application:** If the user commands this signal to toggle "High" then the Transmit Line Build-Out circuit (within the DS3/E3 LIU device) will be disabled. In this mode, the LIU device will output unshaped (e.g., square) pulses onto the line (via the TTIP and TRING output pins). Conversely, if the user commands this signal to toggle "Low" then the Transmit Line Build-Out circuit (within the DS3/E3 LIU device) will be disabled. In this mode, the LIU device will output shaped (e.g., more rounded) pulses onto the line (via the TTIP and TRING output pins). In order to comply with the DSX-3 Isolated Pulse Template Requirement (per Bellcore GR-499-CORE), the user is advised to command this output pin to be "High" if the cable length (between the transmit output of the XRT7300 device and the DSX-3 Cross-Connect System) is greater than 225 feet. Conversely, the user is advised to command this output pin to be "Low" if the cable length (between the transmit output of the XRT7300 device and the DSX-3Cross Connect System) is less than 225 feet. **For E3 Applications:** This pin can be used as a General Purpose Output pin. The Transmit Line Build-Out circuitry (within the XRT7300 device) is not active for E3 applications.
C4	RxLOS[0]	O	**Receive Loss of Signal Output Indicator - Channel 0:** This pin is asserted when the Receive Section of Channel 0 encounters a string of 180 consecutive 0's (for DS3 operation) or 32 consecutive 0's (for E3 operation) via the RxPOS[0] and RxNEG[0] pins. This pin will be negated once the Receive Section has detected at least 60 pulses within 180 bit-periods (for DS3 operation); or the Receive Section has detected a string of 32 consecutive bits, that does not contain a string of 4 consecutive "0s" (for E3 operation).
C5	RxAIS[0]	O	**Receive Alarm Indication Signal Output pin - Channel 0:** Channel 0 will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 or E3 data stream. **For DS3 Applications:** Channel 0 will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 data stream. An AIS is detected if the payload consists of the recurring pattern of 1010... and this pattern persists for 63 M-frames. An additional requirement for AIS indication is that the C-bits are set to 0, and the X-bits are set to 1. This pin will be negated when a sufficient number of frames, not exhibiting the "1010..." pattern in the payload has been detected. **For E3 Applications:** Channel 0 will declare an AIS condition, if it detects two consecutive E3 frames, each containing 7 or less "0s".

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
C6	TAOS[0]	O	**Transmit All Ones Signal (TAOS) Command Input - Channel 0 (for the DS3/E3 LIU IC):** This output pin is intended to be connected to the TAOS input pin of the DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 4 (TAOS) of the Line Interface Drive Register (Address = 0x80). If the user commands this signal to toggle "High" then it will force the Line Interface Unit IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "Low" then the DS3/E3 Line Interface Unit IC will proceed to transmit data based upon the pattern that it receives via the TxPOS[0] and TxNEG[0] output pins. Writing a "1" to Bit 4 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". If the customer is not using an Exar "XRT73L0X Family of DS3/E3 LIU ICs then this output pin can be used for a variety of other purposes.
C7	LLOOP[0]	O	**Local Loopback Output Pin - Channel 0 (to be connected to the DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the LLOOP input pin of the DS3/E3 LIU IC. The user can command this signal to toggle "High" and, in turn, force the LIU into the Local Loopback mode. Writing a "1" to bit 1 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause the RLOOP output to toggle "Low". ***NOTE:*** *This output pin can be used as a General Purpose Output.*
C8	RLOL[1]	I	**Receive Loss of Lock Indicator input - Channel 1 (from the DS3/E3 LIU IC):** See Description for Pin B8
C9	DMO[0]	I	**Drive Monitor Output Input pin - Channel 0 (from the DS3/E3 Line Interface Unit IC):** This input pin is intended to be tied to the DMO output pin of the DS3/E3 Line Interface Unit IC. The user can determine the state of this input pin by reading Bit 2 (DMO) within the Line Interface Scan Register (Address = 0x81). If this input signal is "High", then it means that the drive monitor circuitry (within the DS3/E3 Line Interface Unit IC) has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 (32 bit-periods. If this input signal is "Low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the DS3/E3 LIU device. ***NOTE:*** *This input pin can be used as a General Purpose Input pin.*
C10	RxOHFrame[1]/ RxHDLCDat4[1]	O	**Receive Overhead Frame Boundary Indicator/Receive HDLC Controller Data Output - Bit 4; Channel 1:** See Description for Pin A13
C11	TxOHEnable[1]/ TxHDLCDat7[1]	O I	**Transmit Overhead Data Input Enable/Transmit HDLC Controller Data Output - Bit 7; Channel 1:** See Description for Pin B14

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
C12	RxOH[0]/ RxHDLCDat6[0]	O	**Receive Overhead Data Output/Receive HDLC Data Output - Bit 6; Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the High Speed HDLC Controller Mode, or not. **Non-High Speed HDLC Controller Mode - Receive Overhead Data Output - Channel 0:** All overhead bits, which are received via the Receive Section of the Framer IC; will be output via this output pin, upon the rising edge of RxOHClk. **High Speed HDLC Controller Mode - Receive HDLC Data Output - Bit 6:** This pin functions as bit 6, within the byte-wide Receive HDLC Controller input interface (RxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the “High-Speed HDLC Controller” Mode.
C13	TxOHFrame[0]/ TxHDLCClk[0]	O	**Transmit Overhead Data Framing Pulse/Transmit HDLC Output Clock - Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the High-Speed HDLC Controller Mode, or not. **Non-High Speed HDLC Controller Mode - Transmit Overhead Data Framing Pulse:** This output pin pulses "High" when the Transmit Overhead Data Input Interface block is expecting the first Overhead bit, within a DS3 or E3 frame to be applied to the TxOH input pin. This pin is "High" for one clock period of TxOHClk. **High-Speed HDLC Controller Mode -Transmit HDLC Output Clock:** This pin functions as a demand and latching clock for the Transmit HDLC Controller input interface, when Channel 0 has been configured to operate in the “High-Speed HDLC Controller” Mode.

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
C14	TxOHIns[0]/ TxHDLCDat4[0]	I	**Transmit Overhead Data Insert Input/Transmit HDLC Data Input - Bit 4; Channel 0:** The exact functionality of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode or not. **Non-High Speed HDLC Controller Mode:** Asserting this input signal (e.g., setting it "High") enables the Transmit Overhead Data Input Interface (of Channel 0) to accept overhead data from the Terminal Equipment. In other words, while this input pin is "High", the Transmit Overhead Data Input Interface will sample the data at the TxOH[0] input pin, on the falling edge of the TxOHClk[0] output signal. Conversely, setting this pin "Low" configures the Transmit Overhead Data Input Interface to NOT sample (e.g., ignore) the data at the TxOH[0] input pin, on the falling edge of the TxOHClk[0] output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the Transmit Overhead Data Input Interface (e.g., if the Terminal Equipment asserts the TxOHIns signal, at a time when one of these non-insertable overhead bits are being processed); that particular insertion effort will be ignored.* **High-Speed HDLC Controller Mode - Transmit HDLC Data Input - Bit 4; Channel 0:** This pin functions as bit 4, within the byte-wide Transmit HDLC Controller input interface (TxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller Mode.
C15	TxNib1[1]/ TxHDLCDat1[1]	I	**Transmit Nibble-Parallel Payload Data Input - Bit 1/Transmit HDLC Data Input - Bit 1; Channel 1:** See Description for Pin E17
C16	TxSer[1]/ SndMsg[1]	I	**Transmit Serial Payload Data Input/Transmit HDLC Controller - SEND MESSAGE input - Channel 1:** See Description for Pin E18
C17	TxFrame[1]	O	**Transmit End of DS3 or E3 Frame Indicator - Channel 1:** See Description for Pin E20
C18	RxNib1[1]/ RxHDLCDat[1]	O	**Receive Nibble Output - Bit 1/Receive HDLC Data Output - Bit 1; Channel 1:** See Description for Pin G20
C19	RxNib3[1]/ RxHDLCDat3[1]	O	**Receive Nibble Output - Bit 3/Receive HDLC Data Output - Bit 3; Channel 1:** See Description for Pin H19

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
C20	TxNib2[0]/ TxHDLCDat2[0]	I	**Transmit Nibble-Parallel Payload Data Input - Bit 2/Transmit HDLC Data Input - Bit 2; Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Transmit Nibble-Parallel Payload Data Input -Bit 2; Channel 0:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. The XRT72L53 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **High Speed HDLC Controller Mode - Transmit HDLC Data Input - Bit 2:** This pin functions as bit 2, within the byte-wide Transmit HDLC Controller input interface (TxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
D1	TxNEG[0]	O	**Transmit Negative Polarity Pulse output - Channel 0:** The exact role of this output pin depends upon whether Channel 0 is operating in the Single-Rail or Dual-Rail Mode. **Single-Rail Mode:** This output signal pulses "High" for one bit period, at the end of each outbound DS3 or E3 frame. This output signal is kept at a logic "Low" for all of the remaining bit-periods of the outbound DS3 or E3 frames **Dual-Rail Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS[0] is the other output pin. This input is typically connected to the TNDATA input of the external DS3/E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.
D2	TRST	I	**JTAG Reset Pin:** Resets Boundary Scan Logic. ***NOTE:*** *For normal operation this input pin should be tied "low".*
D3	TMS	I	**Test Mode Select**: Boundary Scan Mode Select input. ***NOTE:*** *For normal operation, this input pin should be tied "low"*
D4	GND	****	**Ground**
D5	RxOOF[1]	O	**Receive Out of Frame Indicator - Channel 1:** See Description for Pin A3
D6	VDD	****	**Power Supply +3.3v ± 5%**
D7	TAOS[1]	O	**Transmit All Ones Signal (TAOS) Command Input - Channel 1 (fto be connected to the "TAOS" input of the DS3/E3 LIU IC):** See Description for Pin C6
D8	GND	****	**Ground**

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
D9	ExtLOS[0]	I	**Receive LOS (Loss of Signal) Indicator Input - Channel 0 (from the DS3/E3 LIU IC):** This input pin is intended to be connected to the RLOS (Receive Loss of Signal) output pin of the DS3/E3 Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 0 (RLOS0) within the Line Interface Scan Register (Address = 0x81). If this input pin is "Low", then it means that the LIU device is currently NOT declaring an LOS (Loss of Signal) condition. However, if this input pin is "High", then it means that the LIU device is currently declaring an LOS (Loss of Signal) condition. Asserting the RLOS input pin will cause the Receive Section of Channel 0 to declare an LOS (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.
D10	RxOHEnable[1]/ RxHDLCDat5[1]	O	**Receive Overhead Enable Indicator/Receive HDLC Controller Data Output - Bit 5; Channel 1:** See Description for Pin B13
D11	VDD	****	**Power Supply +3.3v ± 5%**
D12	RxOHClk[0]/ RxHDLCClk[0]	O	**Receive Overhead Output Clock Signal/Receive HDLC Controller Output Clock - Channel 0:** The exact function of this output pin depends upon whether Channel 0, within the XRT72L53 device has been configured to operate in the "High Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Receive Overhead Output Clock Signal - Channel 0:** Channel 0, within the XRT72L53 device will output the Overhead bits (within the incoming DS3 or E3 frames), via the RxOH[0] output pin, upon the falling edge of this clock signal. As a consequence, the user's data link equipment should use the rising edge of this clock signal to sample the data on both the RxOH[0] and RxOHFrame[0] output pins. ***NOTE:*** *This clock signal is always active.* **High Speed HDLC Controller Mode - Receive HDLC Output Clock - Channel 0:** When the HDLC controller is on, RxHDLCDat is updated by the 72L53 on this clock signal.
D13	GND	****	**Ground**
D14	TxNib0[1]/ TxHDLCDat0[1]	I	**Transmit Nibble-Parallel Payload Data Input - Bit 0/Transmit HDLC Data Input - Bit 0; Channel 1:** See Description for Pin D18
D15	VDD	****	**Power Supply +3.3v ± 5%**
D16	TxNIBClk[1]/ SndFCS[1]	O I	**Transmit Nibble Clock output signal/Transmit HDLC - SEND Frame Check Sequence - Channel 1:** See Description for Pin F18
D17	GND	****	**Ground**

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
D18	TxNib0[0]/ TxHDLCDat0[0]	I	**Transmit Nibble-Parallel Payload Data Input - Bit 0/Transmit HDLC Data Input - Bit 0; Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High-Speed HDLC Controller Mode - Transmit Nibble-Parallel Payload Data Input -Bit 0:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. Channel 0 will take data, applied to this pin (along with that applied to TxNib1[0], TxNib2[0], and TxNib3[0]), and insert it into an outbound E3 or DS3 frame. Channel 0 will sample the data that is at these input pins, upon the rising edge of the TxNibClk[0] signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **High-Speed HDLC Controller Mode - Transmit HDLC Data Input - Bit 0:** This pin functions as bit 0, within the byte-wide Transmit HDLC Controller input interface (TxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
D19	TxNib3[0]/ TxHDLCDat3[0]	I	**Transmit Nibble-Parallel Payload Data Input - Bit 3/Transmit HDLC Data Input - Bit 3; Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Transmit Nibble Parallel Payload Data Input - Bit 3; Channel 0:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound E3 or DS3 frame. The XRT72L53 will sample the data that is at these input pins, upon the rising edge of the TxNibClk signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **High Speed HDLC Controller Mode - Transmit HDLC Data Input - Bit 3:** This pin accepts bit 3 TxHDLC data when the HDLC controller is turned on.

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
D20	RxClk[0]	O	**Receive Clock Output Signal for Serial and Nibble/Parallel Data Interface - Channel 0:** The exact behavior of this signal depends upon whether the XRT72L53 is operating in the Serial or in the Nibble-Parallel-Mode. **Serial Mode Operation:** In the serial mode, this signal is a 44.736MHz clock output signal (for DS3 applications) or 34.368MHz clock output signal (for E3 applications). The Receive Payload Data Output Interface will update the data via the RxSer[0] output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxSer[0] pin, upon the falling edge of this clock signal. **Nibble-Parallel Mode Operation:** In this Nibble-Parallel Mode, Channel 0 will derive this clock signal, from the RxLineClk[0] signal. Channel 0 will pulse this clock signal 1176 times for each inbound DS3 frame (or 1074 times for each inbound "E3/ITU-T G.832" frame, or 384 times for each inbound "E3/ITU-T G.751 frame). The Receive Payload Data Output Interface will update the data, on the RxNib[3:0][0] output pins upon the falling edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the RxNib[3:0][0] output pins, upon the rising edge of this clock signal
E1	TxFrameRef[0]	I	**Transmit Framer Reference Input - Channel 0:** This input pin functions as the Transmit Frame Generation reference signal, if Channel 0 has been configured to operate in the Local-Time/Frame Slave Mode. If Channel 0 has been configured to operate in the Local-Time/Frame-Slave Mode, then the user's terminal equipment is expected to apply a pulse (to this input pin) once every 106.4 microseconds (for DS3 applications); once every 125 microseconds (for E3, ITU-T G.832 applications) or once every 44.7 microseconds (for E3, ITU-T G.751 applications). In the Local-Time/Frame-Slave Mode, the Transmit Section of Channel 0 will initiate its generation of a new outbound DS3 or E3 frame, upon the rising edge of this signal. ***NOTE:*** *The user can configure the XRT72L53 Framer IC to operate in the Local Time/Frame Slave Mode by writing "xxxx xx01" into the Framer Operating Mode Register (Address = 0x00).*
E2	TxLineClk[0]	O	**Transmit Line Interface Clock output - Channel 0:** This clock signal is output to the Line Interface Framer, along with the TxPOS[0] and TxNEG[0] signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Remote Terminal Equipment. The user can configure the source of this clock to be either the RxLineClk[0] (from the Receiver portion of Channel 0) or the TxInClk[0] input. The nominal frequency of this clock signal is 34.368 MHz (for E3 applications), or 44.736MHz for DS3 applications.

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
E3	RxOutClk[0]/ RxHDLCDat7[0]	O	**Receive Out Clock - Transmit Payload Data Input Interface Clock for Loop-Timing/Receive HDLC Data - Bit 7; Channel 0:** The exact function of this output pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode or not. **Non-High-Speed HDLC Controller Mode - Receive Out Clock - Transmit Payload Data Input Interface Clock for Loop-Timing applications - Channel 0:** This clock signal functions as the Terminal Interface clock source, if Channel 0 is operating in the loop-timing mode. In this mode, the Transmitting Terminal Equipment is expected to input data to the Transmit Section of Channel 0, via the "TxSer[0]" input pin, upon the rising edge of this clock signal. Channel 0 will use the rising edge of this clock signal to sample the data at the TxSer[0] input. ***NOTE:*** *This clock signal is a buffered version of the RxLineClk[0] signal.* **Receive HDLC Data Output - Bit 7:** This pin functions as bit 7 within the byte-wide Receive HDLC Controller output interface (RxHDLCDat[7:0]); whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
E4	TDO	O	**Test Data Out:** Boundary Scan test data output.
E17	TxNib1[0]/ TxHDLCDat1[0]	I	**Transmit Nibble-Parallel Payload Data Input - Bit 1/Transmit HDLC Data Input - Bit 2; Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Transmit Nibble-Parallel Payload Data Input -Bit 1:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium, to this input pin. The Framer IC will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. The Transmit Section of Channel 0 will sample the data that is at these input pins, upon the rising edge of the TxNibClk[0] signal. ***NOTE:*** *This input pin is active only if the Nibble-Parallel Mode has been selected.* **Transmit HDLC Data Input - Bit 1:** This pin functions as bit 1 within the byte-wide Transmit HDLC Controller input interface (TxHDLCDat[7:0]); whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
E18	TxSer[0]/	I	**Transmit Serial Payload Data Input pin/Transmit HDLC Controller - SEND MESSAGE Input pin - Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode or not. **Non-High-Speed HDLC Controller Mode - Transmit Serial Payload Data Input Pin - Channel 0:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium, to this input pin. The Transmit Section of Channel 0 will take data, applied to this pin, and insert it into an outbound E3 or DS3 frame. If Channel 0 has been configured to operate in the Local Time Mode, then it will sample the data (on this pin) upon the rising edge of TxInClk[0]. If Channel 0 has been configured to operate in the Loop-Time Mode, then it will sample the data (on this pin) upon the rising edge of RxOutClk[0]. ***NOTE:*** *This input pin is active only if the Serial Mode has been selected.* **High-Speed HDLC Controller Mode - Transmit HDLC SEND MESSAGE Input - Channel 0:** The Terminal Equipment is expected to pull this input pin high during the entire duration of the HDLC packet (including FCS bytes) to be transmitted, when the HDLC controller is turned on.
	SndMsg[0]		
E19	TxOHInd[0]/	O	**Transmit Overhead Data Indicator Output/Transmit HDLC Data Input - 6:** The exact function of this pin depends upon whether Channel0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High-Speed HDLC Controller Mode -Transmit Overhead Data Indicator Output - Channel 0:** This output pin will pulse "High" one-bit period prior to the time that the Transmit Section of Channel 0 will be processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that, during the very next bit-period, Channel 0 is going to be processing an Overhead bit and will be ignoring any data that is applied to the TxSer[0] input pin. ***NOTE:*** *For DS3 applications, this output pin is only active if Channel 0 is operating in the Serial Mode. This output pin will be pulled "Low" if Channel 0 is operating in the Nibble-Parallel Mode.* **Transmit HDLC Data Input - Bit 6:** This input pin functions as bit 6, within the byte-wide Transmit HDLC Controller Input interface (TxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
		I	
	TxHDLCDat6[0]		
E20	TxFrame[0]	O	**Transmit End of DS3 or E3 Frame Indicator - Channel 0:** The Transmit Section of Channel 0 will pulse this output pin "High" (for one bit-period), when the Transmit Payload Data Input Interface is processing the last bit of a given DS3 or E3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to Channel 0 (e.g., to permit Channel 0, within the XRT72L53 device to maintain Transmit DS3/E3 framing alignment control over the Terminal Equipment).

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
F1	RxLineClk[0]	I	**Receiver LIU (Recovered) Clock Input - Channel 0:** This input signal serves three purposes: 1. The Receive Section of Channel 0 uses it to sample and latch the signals at the RxPOS[0] and RxNEG[0] input pins (into the Receive Framer circuitry). 2. This input signal functions as the timing reference for the Receive Framer block, within Channel 0. 3. The Transmit Framer block (within Channel 0) can be configured to use this input signal as its timing reference. This signal is the recovered clock from the external DS3/E3 LIU (Line Interface Unit) IC, which is derived from the incoming DS3/E3 data.
F2	RxPOS[0]	I	**Receive Positive Data Input - Channel 0:** The exact role of this input pin depends upon whether Channel 0 is operating in the Single-Rail or Dual-Rail Mode. **Single-Rail Mode:** This input pin functions as the Single-Rail input for the incoming E3 data stream. The signal at this input pin will be sampled and latched (into the Receive DS3/E3 Framer block within Channel 0) on the user-selected edge of the RxLineClk[0] signal. **Dual-Rail Mode:** This input functions as one of the dual rail inputs for the incoming AMI/HDB3/B3ZS encoded DS3 or E3 data that has been received from an external Line Interface Unit (LIU) IC. RxNEG[0] functions as the other dual rail input for the channel. When this input pin is asserted, it means that the LIU has received a positive polarity pulse from the line.
F3	RxNEG[0]	I	**Receive Negative Data Input - Channel 0:** The exact role of this input pin depends upon whether Channel 0 is operating in the Single-Rail or Dual-Rail Mode. **Single-Rail Mode:** This input pin is inactive, and should be pulled “low” when Channel 0 is operating in the Single-Rail Mode. **Dual-Rail Mode:** This input pin functions as one of the dual rail inputs for the incoming AMI/HDB3/B3ZS encoded DS3 or E3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS[0] functions as the other dual rail input for the Channel. When this input pin is asserted, it means that the LIU has received a negative polarity pulse from the line.
F4	VDD	****	**Power Supply +3.3v ± 5%**
F17	VDD	****	**Power Supply +3.3v ± 5%**

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
F18	TxNIBClk[0]/	O	**Transmit Nibble Clock Output Signal/Transmit HDLC - SEND FRAME CHECK SEQUENCE Input - Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Transmit Nibble Clock output signal - Channel 0:** If the user opts to operate Channel 0 in the "Nibble-Parallel" mode, then the XRT72L53 Framer IC will derive this clock signal from either the "TxInClk[0]" or the "RxLineClk[0]" signal (depending upon which signal is selected as the timing reference). The user is advised to configure the Terminal Equipment to output the "outbound" payload data (to the XRT72L53 Framer IC) onto the "TxNib[3:0][0]" input pins, upon the rising edge of this clock signal. ***NOTES:*** 1. *For DS3 applications, the XRT72L53 Framer IC will output 1176 clock edges (to the Terminal Equipment) for each "outbound" DS3 frame.* 2. *For E3, ITU-T G.832 applications, the XRT72L53 Framer IC will output 1074 clock edges (to the Terminal Equipment) for each "outbound" E3 frame.* 3. *For E3, ITU-T G.751 applications, the XRT72L53 Framer IC will output 384 clock edges (fo the Terminal Equipment) for each "outbound" E3 frame.*
	SndFCS[0]	I	**High-Speed HDLC Controller Mode - SEND FRAME CHECK SEQUENCE Input - Channel 0:** The Terminal Equipment is expected to pull this input pin "High" whenever the "FCS bytes" are being transmitted, after transmitting a valid HDLC message.
F19	RxSer[0]/	O	**Receive Serial Output/Receive Flag Sequence Output - Channel 0** The exact function of this output pin depends upon whether Channel 0 is operating in the "High-Speed HDLC Controller" Mode, or not. **Non High Speed HDLC Controller Mode - Channel 0:** If the user opts to operate Channel 0 in the serial mode, then the chip will output the payload data, of the incoming DS3 or E3 frames, via this pin. Channel 0 will output this data upon the rising edge of RxClk[0]. The user is advised to design the Terminal Equipment such that it will sample this data on the falling edge of RxClk[0]. ***NOTE:*** *This signal is only active if the NibInt input pin is pulled "Low".*
	RxIdle[0]		**High Speed HDLC Controller Mode - Receive Flag Sequence Indicator - Channel 0:** This pin will go high indicating the idle period of sent HDLC data packets. Also, in combination with ValFCS[0] it can indicate error conditions.

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
F20	RxFrame[0]	O	**Receive Boundary of DS3 or E3 Frame Output Indicator - Channel 0:** The exact functionality of this output pin depends upon whether Channel 0 is operating in the “Serial” or “Nibble-Parallel” Mode. **Serial Mode Operation:** The Receive Section of Channel 0 will pulse this output pin “high” (for one bit-period) when the “Receive Payload Data Output Interface” block is driving the very first bit of a given DS3 or E3 frame, onto the “RxSer[0]” output pin. **Nibble-Parallel Operation:** The Receive Section of Channel 0 will pulse this output pin “high” (for one nibble-period), when the “Receive Payload Data Output Interface” block is driving the very first nibble of a given DS3 or E3 frame, onto the “RxNib[3:0][0] output pins.
G1	TxInClk[1]	I	**Transmit Framer Reference Clock Input - Channel 1:** See Description for Pin G4
G2	RxNEG[1]	I	**Receive Negative Data Input - Channel 1:** See Description for Pin F3
G3	TxFrameRef[1]	I	**Transmit Framer Reference Input - Channel 1:** See Description for Pin E1
G4	TxInClk[0]	I	**Transmit Framer Reference Clock Input - Channel 0:** This input pin functions as the Timing Reference for the Transmit Section of Channel 0, within the XRT72L53 Framer IC; if the device has been configured to operate in the Local-Time Mode. Further, if Channel 0 has been configured to operate in the Local-Time Mode, the Transmit Payload Data Input Interface will sample the data at the TxSer[0] input pin, upon the rising edge of TxInClk[0]. For E3 applications, the user should apply a 34.368MHz clock signal to this input. Likewise, for DS3 applications, the user should apply a 44.736MHz clock signal to this input pin. Channel 0, within the XRT72L53 Framer IC can be configured to operate in the Local-Time mode by writing "xxxx xx01" or "xxxx xx1x" into the Framer Operating Mode register (Address = 0x00)

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
G17	TxNibFrame[0]/ ValFCS[0]	O	**Transmit Frame Boundary Indicator - Nibble-Parallel Interface/ Transmit HDLC Controller - VALID FRAME CHECK SEQUENCE output - Channel 0:** The exact function of this input pin depends upon whether Channel 0 has been configured to operate in the “High-Speed HDLC Controller” Mode or not. **Non-High-Speed HDLC Controller Mode - Transmit Frame Boundary Indicator - Nibble/Parallel Interface:** This output pin pulses "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNib[3:0][0] input pins. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame to the XRT72L53 device. **Transmit HDLC - VALID FRAME CHECK SEQUENCE output - Channel 0:** When the HDLC is on, this pin will pulse high, as it completes its reception of an HDLC frames, in order denote reception of an HDLC frame with a “VALID” FCS value.
G18	RxOHInd[0]	O	**Receive Overhead Bit Indicator - Channel 0:** The exact functionality of this output pin depends upon whether the XRT72L53 Framer IC is operating in the “Serial” or “Nibble-Parallel” Mode. **Serial Mode Operation:** This output pin pulses "High" (for one bit-period) whenever an overhead bit is being output via the RxSer output pin, by the Receive Payload Data Output Interface block. **Nibble-Parallel Mode Operation:** This output pin pulses “high” (for one nibble-period) whenever an “overhead” nibble is being output via the “RxNib[3:0] output pins, by the “Receive Payload Data Output Interface” block. ***NOTE:*** *The purpose of this output pin is to alert the Receive Terminal Equipment that an overhead bit is being output via the RxSer output pin, and that this data should be ignored.*

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
G19	RxNib0[0]/ RxHDLCDat0[0]	O	**Receive Nibble Output - Bit 0/Receive HDLC Data - Bit 0, Channel 0:** The exact function of this input pin depends upon whether Channel 0 is operating in the "High-Speed HDLC Controller" Mode, or not. **Non-High Speed HDLC Controller Mode - Receive Nibble Output - Bit 0:** The Receive Section of Channel 0 will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib1[0], RxNib2[0] and RxNib3[0]. The data at this pin is updated on the rising edge of the RxClk[0] output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **Receive HDLC Data Output - Bit 0:** This output pin functions as Bit 0 (the LSB) within the byte-wide Receive HDLC Controller output interface (RxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
G20	RxNib1[0]/ RxHDLCDat1[0]	O	**Receive Nibble Output - Bit 1/Receive HDLC Data - Bit 1; Channel 0:** The exact function of this input pin depends upon whether Channel 0 is operating in the "High-Speed HDLC Controller" Mode, or not. **Non-High-Speed HDLC Controller Mode - Receive Nibble Output - Bit 1:** The Receive Section of Channel 0 will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0[0], RxNib2[0] and RxNib3[0]. The data at this pin is updated on the rising edge of the RxClk[0] output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **Receive HDLC Data Output - Bit 1:** This output pin functions as Bit 1 within the byte-wide Receive HDLC Controller output interface (RxHDLCDat[7:0]), whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
H1	TxLineClk[1]	O	**Transmit Line Interface Clock output - Channel 1:** See Description for Pin E2
H2	RxLineClk[1]	I	**Receiver LIU (Recovered) Clock input - Channel 1:** See Description for Pin F1
H3	RxPOS[1]	I	**Receive Positive Data Input - Channel 1:** See Description for Pin F2
H4	GND	****	**Ground**
H17	GND	****	**Ground**

PIN DESCRIPTION CONNECTED PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
H18	RxNib2[0]/ RxHDLCDat2[0]	O	**Receive Nibble Output - Bit 2/Receive HDLC Data Output - Bit 2; Channel 0:** The exact function of this bit-field depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High-Speed HDLC Controller Mode - Receive Nibble Output - Bit 2:** The Receive Section of Channel 0 will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0[0], RxNib1[0] and RxNib2[0]. The data at this pin is updated on the rising edge of the RxClk[0] output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **High-Speed HDLC Controller Mode - Receive HDLC Data Output - Bit 2:** This pin functions as bit 2, within the byte-wide Receive HDLC Controller output interface (RxHDLCDat[7:0]) whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
H19	RxNib3[0]/ RxHDLCDat3[0]	O	**Receive Nibble Output - Bit 2/Receive HDLC Data Output - Bit 3; Channel 0:** The exact function of this bit-field depends upon whether Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode, or not. **Non-High-Speed HDLC Controller Mode - Receive Nibble Output - Bit 3:** The Receive Section of Channel 0 will output Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0[0], RxNib1[0] and RxNib2[0]. The data at this pin is updated on the rising edge of the RxClk[0] output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **High-Speed HDLC Controller Mode - Receive HDLC Data Output - Bit 3:** This pin functions as bit 3, within the byte-wide Receive HDLC Controller output interface (RxHDLCDat[7:0]) whenever Channel 0 has been configured to operate in the "High-Speed HDLC Controller" Mode.
H20	Int	O	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Framer device is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the Interrupt Request input of the local microprocessor.
J1	TxFrameRef[2]	I	**Transmit Framer Reference Input - Channel 1:** See Description for Pin E1