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FOUR CHANNEL DS3/E3 FRAMER IC WITH HDLC CONTROLLER

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GENERAL DESCRIPTION

The XRT72L54, 4 Channel DS3/E3 Framer IC is designed to accept “User Data” from the Terminal Equipment and insert this data into the “payload” bitfields within an “outbound” DS3/E3 Data Stream. Further, the Framer IC is also designed to receive an “inbound” DS3/E3 Data Stream (from the Remote Terminal Equipment) and extract out the “User Data”.

The XRT72L54 DS3/E3 Framer device is designed to support full-duplex data flow between Terminal Equipment and an LIU (Line Interface Unit) IC. The Framer Device will transmit, receive and process data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.

The XRT72L54 DS3/E3 Framer IC consists of Four Transmit sections, Four Receiver sections, Four Performance Monitor Sections and a Microprocessor interface.

The Transmit Sections, include a Transmit Payload Data Input Interface, a Transmit Overhead data Input Interface Section, a Transmit HDLC Controller, a Transmit DS3/E3 Framer block and a Transmit LIU Interface Block which permits the Terminal Equipment to transmit data to a remote terminal.

The Receive Sections, consist of a Receive LIU Interface, a Receive DS3/E3 Framer, a Receive HDLC Controller, a Receive Payload Data Output Interface, and a Receive Overhead Data Interface which allows the local terminal equipment to receive data from remote terminal equipment.

The Microprocessor Interface is used to configure the Framer IC in different operating modes and monitor the performance of the Framer.

The Performance Monitor Sections consist of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/health of the Four channels of the Framer IC/system.

FEATURES

- Transmits, Receives and Processes data in the DS3-C-bit Parity, DS3-M13, E3-ITU-T G.751 and E3-ITU-T G.832 Framing Formats.
- 6 Channel HDLC Controller - Tx and Rx
- Interfaces to all Popular Microprocessors
- Integrated Framer Performance Monitor
- Available in a 272 Ball PBGA package
- 3.3V Power Supply, 5V Tolerant I/O
- Operating Temperature -40°C to +85°C

APPLICATIONS

- Network Interface Units
- CSU/DSU Equipment.
- PCM Test Equipment
- Fiber Optic Terminals
- DS3/E3 Frame Relay Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT72L54

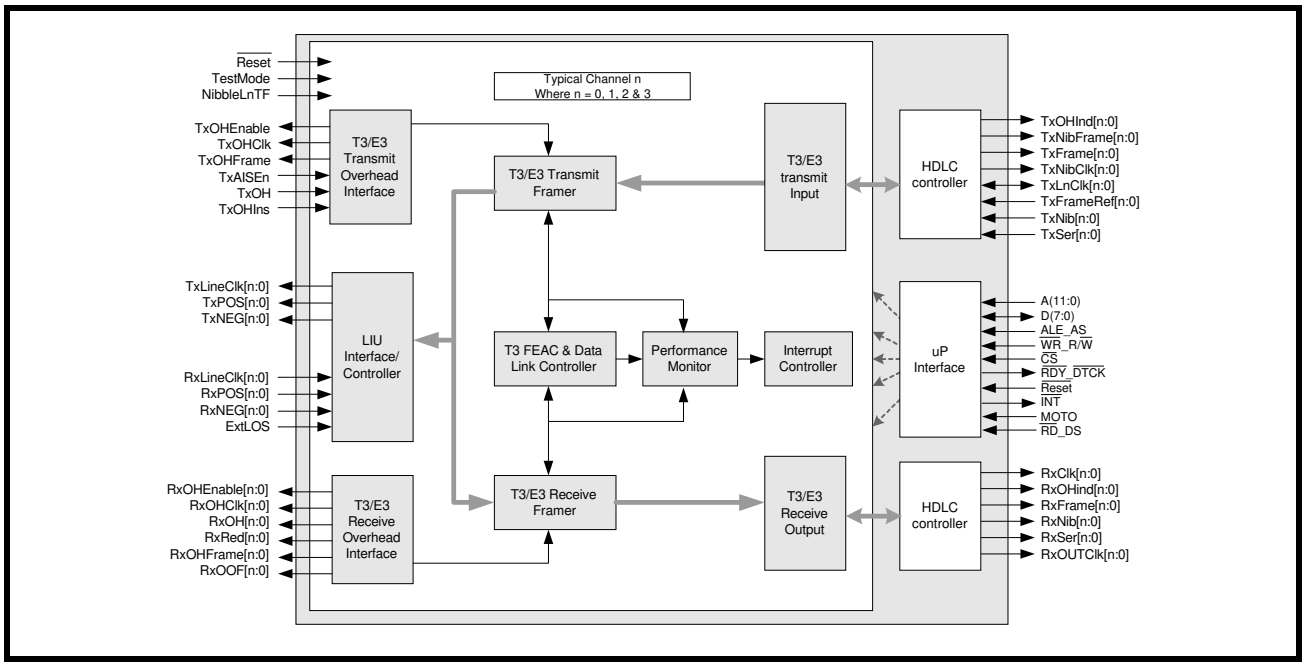
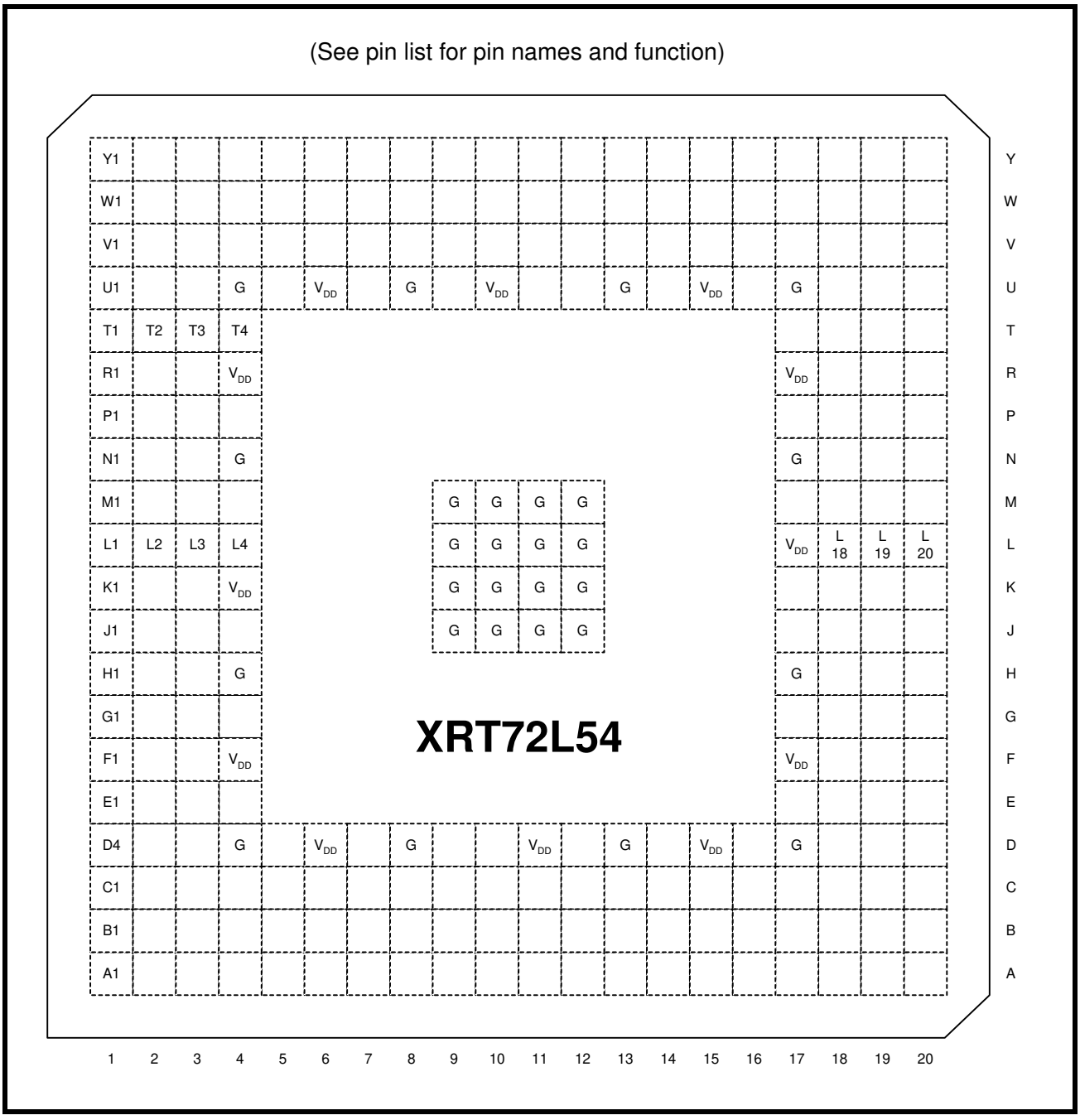


FIGURE 2. PIN OUT OFTHE XRT72L54



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT72L54	27x27 mm 272 Ball PBGA	-40°C to +85°C

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PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
A1	TxLev[1]	O	See Description for Pin C3
A2	EncoDis[1]	O	See Description for Pin B2
A3	RxOOF[0]	O	**Receiver "Out of Frame" Indicator:** The Receive Section of the XRT72L54 Framer IC will assert this output signal whenever it has declared an "Out of Frame" (OOF) condition with the incoming DS3 or E3 frames. This signal is negated when the framer correctly locates the framing alignment bits or bytes and correctly aligns itself with the incoming DS3 or E3 frames.
A4	RxRed[1]	O	See Description for Pin B5
A5	$\overline{\text{Req}}$[0]	O	**Receive Equalization Enable/Disable Select output pin - (to be connected to the XRT7300 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the $\overline{\text{REQ}}$ input pin of the XRT7300 DS3/E3 ($\overline{\text{REQDIS}}$ or $\overline{\text{REQEN}}$ of the XRT73L03 or XRT 73L04) Line Interface Unit IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 5 ($\overline{\text{REQ}}$) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "high" then the internal Receive Equalizer (within the XRT7300 Device) will be disabled. Conversely, if the user commands this output signal to toggle "low", then the internal Receive Equalizer (within the XRT7300 Device) will be enabled. For information on the criteria that should be used when deciding whether to bypass the equalization circuitry or not, please consult the "XRT7300 DS3/E3 Line Interface Unit" data sheet. Writing a "1" to Bit 5 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". If the Exar XRT7300 DS3/E3 family of Line Interface Unit IC's are not used, then this output pin can be used for other purposes.
A6	LLOOP[1]	O	See Description for Pin C7
A7	RLOOP[1]	O	See Description for Pin B7
A8	ExtLOS[1]	I	See Description for Pin D9
A9	RxOHClk[1]/ RxHDLCClk[1]	O	See Description for Pin D12
A10	TxOHClk[1]	O	See Description for Pin A14
A11	TxOHFrame[1]/ TxHDLCClk[1]	O	See Description for Pin C13
A12	TxOH[1]/ TxHDLCDat5[1]	I	See Description for Pin A15
A13	RxOHFrame[0]/ RxHDLCDat4[0]	O	**Receive Overhead Frame Boundary Indicator:** This output pin pulses "high" whenever the Receive Overhead Data Output Interface" block outputs the first overhead bit (or nibble) of a new DS3 or E3 frame. **Receive HDLC Data Output - 4:** This pin contains bit 4 RxHDLC data when the HDLC controller is on.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
A14	TxOHClk[0]	O	**Transmit Overhead Clock:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface block will provide a rising clock edge on this signal, one bit-period prior to the start to the instant that the “Transmit Overhead Data Input Interface” block is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the “TxOH” input pin, on the falling edge of this clock signal (provided that the “TxOHIns” input pin is “HIGH”). ***NOTE:*** *The Transmit Overhead Data Input Interface block will supply a clock edge for all overhead bits within the DS3 or E3 frame (via the “TxOHClk” output signal). This includes those overhead bits that the “Transmit Overhead Data Input Interface” will not accept from the Terminal Equipment.*
A15	TxOH[0]/ TxHDLCDat5[0]	I	**Transmit Overhead Input Pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the "overhead" bit position within the very next "outbound" DS3 or E3 frame. If the "TxOHIns" pin is pulled "high", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the "TxOHClk" output pin. Conversely, if the "TxOHIns" pin is pulled "low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored. **Transmit HDLC Data Input - 5:** This pin accepts bit 5 TxHDLC data when the HDLC controller is turned on.
A16	TxNib2[1]/ TxHDLCDat2[1]	I	See Description for Pin C20
A17	RxSer[1]/ RxIdle[1]	O	See Description for Pin F19
A18	TxOHInd[1]/ TxHDLCDat6[1]	O I	See Description for Pin E19
A19	RxOHInd[1]	O	See Description for Pin G18
A20	RxClk[1]	O	See Description for Pin D20
B1	TDI	I	**Test Data In:** Boundary Scan Test data input.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
B2	EncoDis[0]	O	**Encoder (HDB3) Disable Output pin (intended to be connected to the XRT7300 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the Encodis input pin of the XRT7300 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (Encodis) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "high" then it will disable the B3ZS/HDB3 encoder circuitry within the XRT7300 IC. Conversely, if the user commands this output signal to toggle "low", then the B3ZS/HDB3 Encoder circuitry, within the XRT7300 IC will be enabled. Writing a "1" to Bit 3 of the Line Interface Driver Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". The user is advised to disable the B3ZS/HDB3 encoder (within the XRT7300 IC) if the XRT72L54 Framer IC has been configured to operate in the B3ZS/HDB3 line code. ***NOTE:*** *If the customer is not using the XRT7300 DS3/E3 Line Interface Unit IC, then he/she can use this output pin for a variety of other purposes.*
B3	RxLOS[1]	O	See Description for Pin C4
B4	RxAIS[1]	O	See Description for Pin C5
B5	RxRed[0]	O	**Receiver Red Alarm Indicator - Receive Framer:** The Framer asserts this output pin to denote that one of the following events has been detected by the Receive Framer: LOS - Loss of Signal Condition OOF - Out of Frame Condition AIS - Alarm Indication Signal Detection
B6	$\overline{\text{Req}}$[1]	O	See Description for Pin A5
B7	RLOOP[0]	O	**Remote Loopback Output Pin (to the XRT7300 DS3/E3 Line Interface Unit IC):** This output pin is intended to be connected to the RLOOP input pin of the XRT7300 DS3/E3 Line Interface Unit IC. The user can command this signal to toggle "high" and, in turn, force the XRT7300 DS3/E3 Line Interface Unit IC into the "Remote Loopback" mode. Conversely, the user can command this signal to toggle "low" and allow the XRT7300 device to operate in the normal mode. (For a detailed description of the XR-T7300 DS3/E3 Line Interface Unit IC's operation during Remote Loopback, please see the XR-T7300 DS3/STS-1/ E3 Line Interface Unit IC's Data Sheet). Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause the RLOOP output to toggle "low". ***NOTE:*** *If the customer is not using the XRT7300 DS3/E3 Line Interface Unit IC, then he/she can use this output pin for a variety of other purposes.*

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
B8	RLOL[0]	I	**Receive Loss of Lock Indicator - from the XRT7300 DS3/E3 Line Interface Unit IC:** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the XRT7300 Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 0x81). If this input pin is "low", then it means that the "clock recovery phase-locked-loop" circuitry, within the XRT7300 device is properly locked onto the incoming DS3 E3 data-stream; and is properly recovering clock and data from this DS3/E3 data-stream. However, if this input pin is "high", then it means that the phase-locked-loop circuitry, within the XRT7300 device has lost lock with the incoming DS3 or E3 data-stream, and is not properly recovering clock and data. For more information on the operation of the XRT7300 DS3/E3 Line Interface Unit IC, please consult the "XRT7300 DS3/E3 Line Interface Unit" data sheet. If the customer is not using the XRT7300 DS3/E3 Line Interface Unit IC, he/she can use this input pin for other purposes.
B9	DMO[1]	I	See Description for Pin C9
B10	RxOH[1]/ RxHDLCDat6[1]	O	See Description for Pin C12
B11	TxOHIns[1]/ TxHDLCDat4[1]	I	See Description for Pin C14
B12	TxAISEn[1]	I	See Description for Pin B15
B13	RxOHEnable[0]/ RxHDLCDat5[0]	O	**Receive Overhead Enable Indicator:** The XRT72L54 device will assert this output signal for one “RxOutClk” period when it is safe for the Terminal Equipment to sample the data on the “RxOH” output pin. **Receive HDLC Data Output - 5:** This pin contains bit 5 RxHDLC data when the HDLC controller is on.
B14	TxOHEnable[0]/ TxHDLCDat7[0]	O I	**Transmit Overhead Input Enable:** The XRT72L54 device will assert this signal, for one “TxInClk” period, just prior to the instant that the “Transmit Overhead Data Input Interface” will be sampling and processing an overhead bit. If the Terminal Equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 frame, it is expected to sample the state of this signal, upon the falling edge of “TxInClk”. Upon sampling the “TxOHEnable” high, the Terminal Equipment should (1) place the desired value of the overhead bit, onto the “TxOH” input pin and (2) assert the “TxOHIns” input pin. The Transmit Overhead Data Input Interface” block will sample and latch the data on the “TxOH” signal, upon the rising edge of the very next “TxInClk” input signal. **Transmit HDLC Data Input - 7:** This pin accepts bit 7 TxHDLC data when the HDLC controller is turned on.