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GENERAL DESCRIPTION

The XRT72L71 DS3 ATM User Network Interface (UNI)/Clear-Channel Framer is designed to function as either a DS3 ATM UNI or Clear channel framer. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for both the public and private networks at DS3 rates. For Clear-Channel framer applications, this device supports the transmission and reception of "user data" via the DS3 payload bits.

The XRT72L71incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive sections.

APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Concentrators
- DSLAM Equipment
- DS3 Frame Relay Equipment

FEATURES

- Compliant with UTOPIA Level 1 and 2 with 8 or 16 Bit Interface Specification and supports UTOPIA Bus speeds of up to 50 MHz
- Contains on-chip 16 cell FIFO in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit OAM Cell buffer and a 108 byte Receive OAM cell buffer, for transmission, reception and processing of OAM cells.
- Supports PLCP or ATM Direct Mapping modes
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3 Clear Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Local, Remote-Line, Cell, and PLCP Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs
- Low power 3.3V, 5V input tolerant, CMOS
- 160 pin PQFP Package
- 3 and 4 Channel Version also Available

FIGURE 1. XRT72L71 SIMPLIFIED BLOCK DIAGRAM WITH SYSTEM INTERFACES

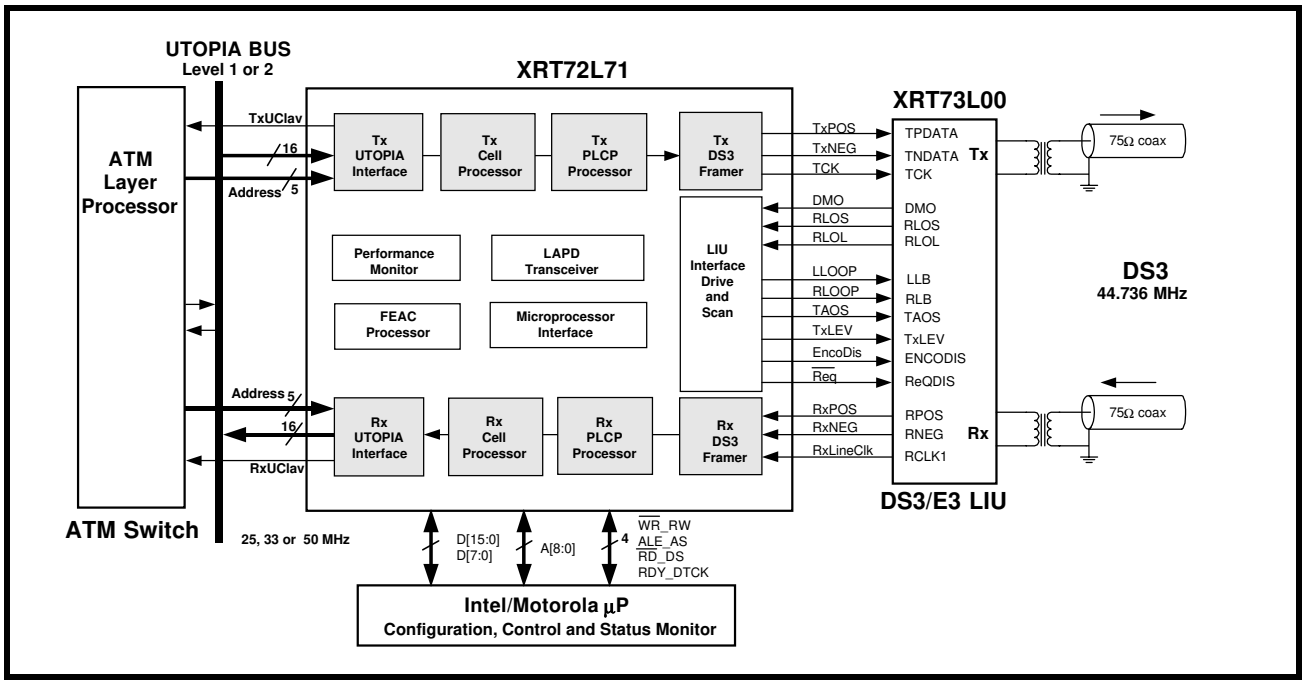


FIGURE 2. BLOCK DIAGRAM OF THE XRT72L71 DS3 UNI

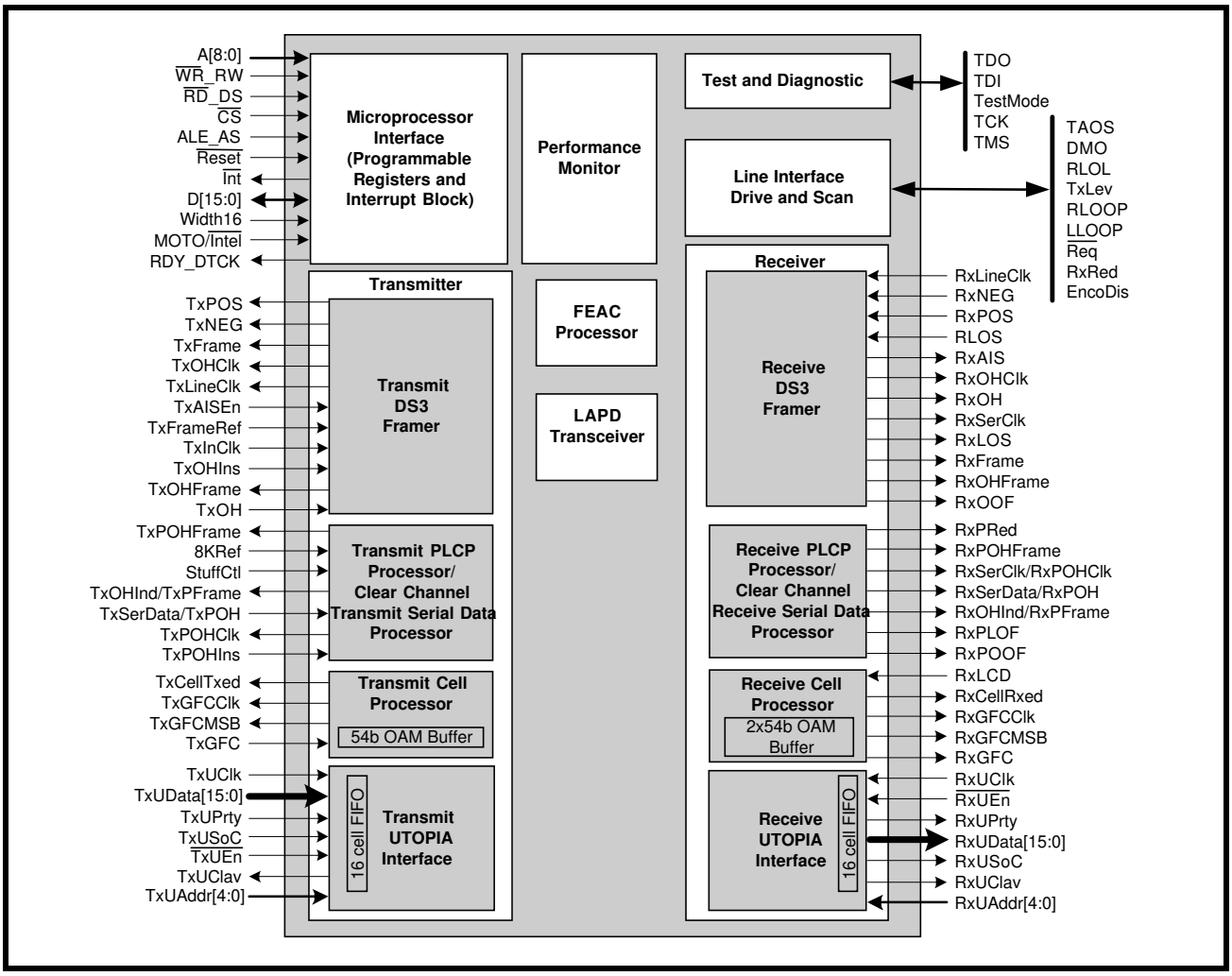
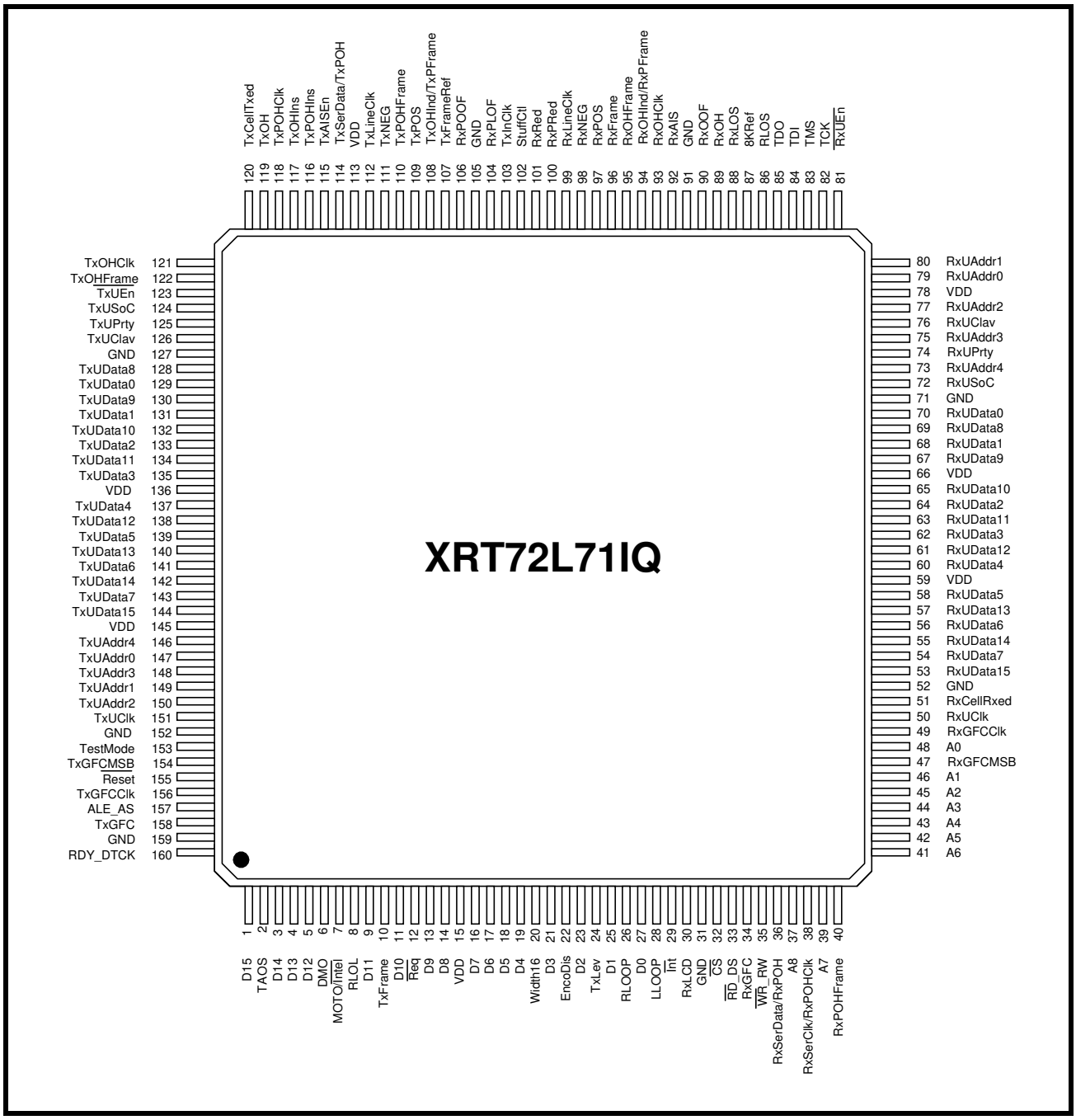


FIGURE 3. PIN OUT OF THE XRT72L71 DS3 ATM UNI



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L71IQ	160 PQFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS (SEE FIGURE 3)

PIN DESCRIPTION

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1	D15	I/O	**MSB of Bi-Directional Data Bus (Microprocessor Interface Section):** This pin, along with pins D0 - D14, function as the Microprocessor Interface bi-directional data bus, and is intended to be interfaced to the "local" microprocessor. This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus.
2	TAOS	O	**"Transmit All Ones Signal" (TAOS) Command (for the XRT7300 LIU IC).** This output pin is intended to be connected to the TAOS input pin of the XRT7300 LIU IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 4 (TAOS) within the Line Interface Drive Register (Address = 0x72). If the user commands this signal to toggle "High" then it will force the XRT7300 DS3 Line Transmitter IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "Low" then the XRT7300 DS3 Line Transmitter IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins. Writing a "1" to Bit 4 of the Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTE:*** *If the designer is not using the XRT7300 DS3/E3/STS-1 LIU IC, then this output pin can be used for other purposes.*
3 4 5	D14 D13 D12	I/O	**Bi-directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. Please see description for D15, pin 1.
6	DMO	I	**"Drive Monitor Output" Input (from the XRT7300 LIU IC):** This input pin is intended to be tied to the DMO output pin of the XRT7300 E3/DS3/STS-1 LIU IC. The user can determine the state of this input pin by reading Bit 2 (DMO) within the Line Interface Scan Register (Address = 0x73). If this input signal is "High", then it means that the drive monitor circuitry (within the XRT7300 LIU IC) has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 ± 32 bit-periods. If this input signal is "Low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT7300. ***NOTE:*** *If the designer is not using the XRT7300 E3/DS3/STS-1 LIU IC, then this input pin can be used for other purposes.*
7	MOTO/$\overline{\text{Intel}}$	I	**Motorola/Intel Processor Interface Select Mode:** This input pin allows the user to configure the Microprocessor Interface to interface with either a "Motorola-type" or "Intel-type" microprocessor/microcontroller. Tying this input pin to VDD, configures the microprocessor interface to operate in the Motorola mode (e.g., the UNI/Framer can be readily interfaced to a "Motorola type" local microprocessor). Tying this input pin to GND configures the microprocessor interface to operate in the Intel Mode (e.g., the UNI/Framer can be readily interfaced to an "Intel type" local microprocessor).

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
8	RLOL	I	**Receive Loss of Lock Indicator—from the XRT7300 E3/DS3/STS-1 LIU IC:** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the XRT7300 LIU IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 0x73). If this input pin is "Low", then it means that the phase-locked-loop circuitry, within the XRT7300 is properly locked onto the incoming DS3 data-stream; and is properly recovering clock and data from this DS3 data-stream. However, if this input pin is "High", then it means that the phase-locked-loop circuitry, within the XRT7300 has lost lock with the incoming DS3 data-stream, and is not properly recovering clock and data. For more information on the operation of the XRT7300 E3/DS3/STS-1 LIU IC, please consult the "XRT7300 E3/DS3/STS-1 LIU IC" data sheet. ***NOTE:*** *If the designer is not using the XRT7300 DS3/E3/STS-1 LIU IC, this input pin can be used for other purposes.*
9	D11	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8-bit wide data bus. Please see description for D15, pin 1.
10	TxFrame	O	**Transmit End of DS3 Frame Indicator:** The function of this pin is same in both Clear Channel and ATM UNI modes of the XRT72L71. This pin marks the end of each DS3 frame. **ATM UNI Mode** This pin is pulsed for one DS3 clock period when the transmit input interface is processing the last bit of the given DS3 frame. This just serves as an indication to terminal equpiment in the ATM UNI mode. **Clear Channel Mode** When the XRT72L71is configured to operate in the "Clear-Channel Framer" mode, then the Transmit DS3 Framer block will pulse this output pin "High" (for one bit period) when the "Transmit Payload Data Input Interface" block is processing the last bit of a given DS3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 frame to the XRT72L71 (e.g., to permit the XRT72L71 to maintain Transmit DS3 framing alignment control over the Terminal Equipment).
11	D10	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. (Please see description for D15, pin 1)
12	$\overline{\text{Req}}$	O	**Receive Equalization Bypass Control Output Pin—(to be connected to the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the $\overline{\text{Req}}$ input pin of the XRT7300 E3/DS3/STS-1 LIU IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 5 ($\overline{\text{Req}}$) of the Line Interface Driver Register (Address = 0x72). If the user commands this signal to toggle "High" then it will cause the incoming DS3 line signal to "bypass" equalization circuitry, within the XRT7300. Conversely, if the user commands this output signal to toggle "Low", then the incoming DS3 line signal with be routed through the equalization circuitry. For information on the criteria that should be used when deciding whether to bypass the equalization circuitry or not, please consult the "XRT7300 E3/DS3/STS-1 LIU IC" data sheet. Writing a "1" to Bit 5 of the Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTE:*** *If the designer is not using the XRT7300 E3/DS3/STS-1 LIU IC, then this output pin can be used for other purposes.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
13	D9	I/O	**Bi-Directional Data bus (Microprocessor Interface Section): T**his pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. Please see description for D15, pin1.
14	D8	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. Please see description for D15, pin1.
15	VDD	***	**Power Supply Pin**
16 17 18 19	D7 D6 D5 D4	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** Please see description for D15, pin 1.
20	Width16	I	**Microprocessor Interface Block Data Bus Width Selector:** This input pin permits the user to configure the microprocessor interface of the UNI/Framer, to operate over either an 8 or 16 bit wide bi-directional data bus. Tying this pin to VDD configures the Microprocessor Interface Data Bus width to be 16 bits. Tying this pin to GND configures the Microprocessor Interface Data Bus width to be 8 bits.
21	D3	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** Please see description for D15, pin 1.
22	EncoDis	O	**Encoder (B3ZS) Disable Output pin (intended to be connected to the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the EncoDis input pin of the XRT7300 LIU IC. The user can control the state of this output pin by writing a “0” or “1” to Bit 3 (EncoDis) of the Line Interface Driver Register (Address = 0x72). If the user commands this signal to toggle “High” then it will disable the B3ZS encoder circuitry within the XRT7300 IC. Conversely, if the user commands this output signal to toggle “Low”, then the B3ZS Encoder circuitry, within the XRT7300 IC will be enabled. Writing a “1” to Bit 3 of the Line Interface Driver Register (Address = 0x72) will cause this output pin to toggle “High”. Writing a “0” to this bit-field will cause this output pin to toggle “Low”. ***NOTES:*** *1. The user is advised to disable the B3ZS encoder (within the XRT7300 IC) if the Transmit and Receive DS3 Framers (within the UNI) are configured to operate in the B3ZS line code.* *2. If the designer is not using the XRT7300 DS3/E3/STS-1 Line Transmitter IC, then output pin can be used for other purposes.*
23	D2	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** Please see description for D15, pin1.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
24	TxLev	O	**Transmit Line Build Enable/Disable Select (to be connected to the TxLev input pin of the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the TxLev input pin of the XRT7300 E3/DS3/STS-1 LIU IC. The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 0x72). If the user commands this signal to toggle "High" then it will disable the "Transmit Line Build-Out" circuitry within the XRT7300. In this case, the XRT7300 will output unshaped (square-wave) pulses onto the "Transmit Line Signal". In order to insure that the XRT7300 generates a line signal that is compliant with the Bellcore GR-499-CORE Pulse Template requirements (at the DSX-3 Cross-Connect), the user is advised to set this output pin "High", if the cable length (between the Transmit Output of the XRT7300 and the DSX-3 Cross-Connect) is greater than 225 feet. Conversely, if the user commands this signal to toggle "High", then it will enable the "Transmit Line Build-Out" circuitry within the XRT7300. In this case, the XRT7300 will output shaped pulses onto the "Transmit Line Signal". In order to ensure that the XRT7300 generates a line signal that is compliant with the Bellcore GR-499-CORE Pulse Template requirements (at the DSX-3 Cross-Connect), the user is advised to set this output pin "Low", if the cable length (between the Transmit Output of the XRT7300 and the DSX-3 Cross Connect) is less than 225 ft. of cable. Writing a "1" to Bit 2 of the Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTE:*** *If the customer is not using the XRT7300 DS3/E3/STS-1 LIU IC, then this output pin can be used for other purposes.*
25	D1	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** Please see description for D15, pin1.
26	RLOOP	O	**Remote Loop-back Output Pin (to the XRT7300 DS3/E3/STS-1 LIU IC):** This output pin is intended to be connected to the RLOOP input pin of the XRT7300 LIU IC. This output pin, along with the LLOOP input pin (pin 28) permits the user to configure the XRT7300 to operate in either of the following three (3) loop-back modes. • Analog Local Loop-back Mode • Digital Local Loop-back Mode • Remote Loop-back Mode. Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause the RLOOP output to toggle "Low". ***NOTE:*** *If the customer is not using the XRT7300 DS3/E3/STS-1 IC, then this output pin can be used for other purposes.*
27	D0	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** Please see description for D15, pin1.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
28	LLOOP	O	**Local Loop-back Output Pin (to the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the LLOOP input pin of the XRT7300 LIU IC. This input pin, along with "RLOOP" (pin 26) permits the user to configure the XRT7300 LIU IC to operate in either of the following three (3) loop-back modes. • Analog Local Loop-Back Mode • Digital Local Loop-Back Mode • Remote Loop-Back Mode. Writing a "1" to bit 1 of the "Line Interface Drive Register" (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause the RLOOP output to toggle "Low". ***NOTE:*** *If the user is not using the XRT7300 DS3/E3/STS-1 LIU IC, then this output pin can be used for other purposes.*
29	$\overline{\text{Int}}$	O	**Interrupt Request Output:** This open-drain, active-"Low" output signal will be asserted when the UNI/Framer is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the local microprocessor.
30	RxLCD	O	**Loss of Cell Delineation Indicator:** This active-"High" output pin will be asserted whenever the Receive Cell Processor has experienced a "Loss of Cell Delineation". This pin will return "Low" once the Receive Cell Processor has regained Cell Delineation. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
31	GND	***	**Ground Pin Signal**
32	$\overline{\text{CS}}$	I	**Chip Select Input:** This active-"Low" input signal selects the Microprocessor Interface Section of the UNI/Framer and enables Read/Write operations between the "local" microprocessor and the UNI/Framer on-chip registers and RAM locations.
33	$\overline{\text{RD}}$_DS	I	**Read Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this input will function as the $\overline{\text{RD}}$ (READ STROBE) input signal from the local µP. Once this active-"Low" signal is asserted, then the UNI/Framer will place the contents of the addressed registers (within the UNI/Framer IC) on the Microprocessor Data Bus (D[15:0]). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe (Motorola Mode):** If the microprocessor interface is operating in the Motorola mode, then this pin will function as the active-"Low" Data Strobe signal.
34	RxGFC	O	**Receive GFC Nibble Field Serial Output pin:** This pin, along with the RxGFCClk and the RxGFCMSB pins form the "Receive GFC Nibble-Field" serial output port. This pin will serially output the contents of the GFC Nibble field of each cell that is processed through the Receive Cell Processor. This data is serially clocked out of this pin on the rising edge of the RxGFCClk signal. The Most Significant Bit (MSB) of each GFC value is designated by a pulse at the RxGFCMSB output pin. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
35	$\overline{WR}$_RW	I	**Write Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this active-"Low" input pin functions as the WR (Write Strobe) input signal from the µP. Once this active-"Low" signal is asserted, then the UNI will latch the contents of the µP Data Bus, into the addressed register (or RAM location) within the UNI/Framer IC. **R/W Input Pin (Motorola Mode):** When the Microprocessor Interface Section is operating in the "Motorola Mode", then this pin is functionally equivalent to the "R/W*" pin. In the Motorola Mode, a "READ" operation occurs if this pin is at a logic "1". Similarly, a WRITE operation occurs if this pin is at a logic "0".
36	RxSerData/ RxPOH	O	**Receive Serial Output/Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Output Pin:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM UNI Mode. **Clear Channel Mode:** In clear channel mode, all DS3 data which is received by XRT72L71 will be output as a serial data stream via this pin. The XRT72L71 will output data (via this pin) upon the falling edge of "RxSerClk". As a consequence, this data should be sampled with the rising edge of RxSerClk. **ATM UNI Mode:** This output pin, along with RxPOHClk, RxPOHFrame, and RxPOHIns pins comprise the "Receive PLCP Frame POH Byte" serial output port. For each PLCP frame that is received by the Receive PLCP Processor, this serial output port will output the contents of all 12 POH (Path Overhead) bytes. The data that is output via this pin, is updated on the rising edge of the RxPOHClk output clock signal. The RxPOHFrame pin will pulse "High" when the first bit of the Z6 byte is being output on this output pin.
37	A8	I	**Address Bus Input (Microprocessor Interface)—MSB (Most Significant Bit):** This input pin, along with inputs A0 - A7 are used to select the on-chip UNI register and RAM space for READ/WRITE operations with the "local" microprocessor.
38	RxSerClk/ RxPOHClk	O	**Clear Channel Mode Receive Clock Output Signal for Serial Data Interface/ Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Output Clock Signal:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM UNI Mode. **Clear Channel Mode - RxSerClk:** In clear channel mode, this pin can be used by the external interface to sample the clear channel serial data stream on RxSer pin. The Receive Section of the XRT72L71 will output all "inbound" DS3 data, via the "RxSerData" output pin, upon the rising edge of this output pin. Hence, the user should be sampling the data (on the "RxSerData" output pin) upon the rising edge of this clock. **ATM UNI MODE - RxPOHClk:** In the ATM UNI mode of operation, this pin serves as RxPOHClk. This output clock pin, along with RxPOH, RxPOHframe pins comprise the 'Receive PLCP OH serial output' interface.
39	A7	I	**Address Bus Input (Microprocessor Interface):** Please see description for A8, pin 37.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
40	RxPOHFrame	O	**Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Beginning of Frame Signal Pin:** This output pin, along with RxPOH, RxPOHClk, and RxPOHIns pins comprise the "Receive PLCP Frame POH Byte" serial output port. This output pin provides framing information to external circuitry receiving and processing this POH (Path Overhead) data, by pulsing "High" when the first bit of the Z6 byte is output via the RxPOH output pin. This pin is "Low" at all other times during this PLCP POH framing cycle. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configued to operate in the "ATM UNI" Mode.*
41 42 43 44 45 46	A6 A5 A4 A3 A2 A1	I	**Address Bus Input (Microprocessor Interface):** Please see description for A8, pin 37.
47	RxGFCMSB	O	**Received GFC Nibble Field—MSB Indicator**: This output pin functions as a part of the "Receive GFC-Nibble Field" Serial Output port; which also consists of the RxGFC and RxGFCClk pins. This pin pulses "High" the instant that the MSB (Most Significant Bit) of a GFC Nibble is being output on the RxGFC pin. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
48	A0	I	**Address Bus Input (Microprocessor Interface)—LSB (Least Significant Bit):** Please see description for A8, pin 37.
49	RxGFCClk	O	**Received GFC Nibble Serial Output Port Clock Signal:** This output pin functions as a part of the "Receive GFC Nibble-Field" Serial Output Port; also consisting of the RxGFC and RxGFCMSB pins. This pin provides a clock pulse which allows external circuitry to latch in the GFC Nibble-Data via the RxGFC output pin. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
50	RxUClk	I	**Receive UTOPIA Interface Clock Input:** The byte (or word) data, on the Receive UTOPIA Data bus is updated on the rising edge of this signal. The Receive UTOPIA Interface can be clocked at rates up to 50 MHz. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer'" Mode.*
51	RxCellRxed	O	**Receive Cell Processor—Cell Received Indicator:** This output pin pulses "High" each time the Receive Cell Processor receives a new cell from the Receive PLCP Processor or the Receive DS3 Framer. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
52	GND	***	**Ground Pin Signal**
53	RxUData15	O	**Receive UTOPIA Data Bus Output (MSB):** This output pin, along with RxUData14 through RxUData0 functions as the Receive UTOPIA Data Bus. ATM cell data that has been received from the "Remote Terminal Equipment" is output on the Receive UTOPIA Data Bus, where it can be read and processed by the ATM Layer Processor. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
54 55 56 57 58	RxUData7 RxUData14 RxUData6 RxUData13 RxUData5	O	**Receive UTOPIA Data Bus Output:** Please see description of RxUData15, pin 53. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
59	VDD	***	**Power Supply Pin**
60 61 62 63 64 65	RxUData4 RxUData12 RxUData3 RxUData11 RxUData2 RxUData10	O	**Receive UTOPIA Data Bus Output:** Please see description of RxUData15, pin 53. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
66	VDD	***	**Power Supply Pin**
67 68 69	RxUData9 RxUData1 RxUData8	O	**Receive UTOPIA Data Bus Output:** Please see description of RxUData15, pin 53. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
70	RxUData0	O	**Receive UTOPIA Data Bus Output - LSB:** Please see description of RxUData15, pin 53. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
71	GND	***	**Ground Signal Pin**
72	RxUSoC	O	**Receive UTOPIA Interface—Start of Cell Indicator:** This output pin allows the ATM Layer Processor to determine the boundaries or the ATM cells that are output via the Receive UTOPIA Data bus. The Receive UTOPIA Interface block will assert this signal when the first byte (or word) of a new cell is present on the Receive UTOPIA Data Bus; RxUData[15:0]. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
73	RxUAddr4	I	**Receive UTOPIA Address Bus input (MSB):** This input pin, along with RxUAddr3 through RxUAddr0 functions as the Receive UTOPIA Address bus inputs. These input pins are only active when the UNI is operating in the Multi-PHY Mode. The Receive UTOPIA Address Bus input is sampled on the rising edge of the RxUClk signal. The contents of this address bus are compared with the value stored in the "Rx UT Address Register (Address = 6Ch). If these two values match, then the UNI will inform the ATM Layer Processor on whether or not it has any new ATM cells to be read from the RxFIFO; by driving the RxUClav output to the appropriate level. If these two address values do not match, then the UNI will not respond to the ATM Layer Processor; and will keep its RxUClav output signal tri-stated. ***NOTE:*** *The user should tie this pin to "GND", whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
74	RxUPrty	O	**Receive UTOPIA Interface—Parity Output pin:** The Receive UTOPIA interface block will compute the odd-parity of each byte (or word) that will place in the Receive UTOPIA Data Bus. This odd-parity value will be output on this pin, while the corresponding byte (or word) is present on the Receive UTOPIA Data Bus. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
75	RxUAddr3	I	**Receive UTOPIA Address Bus input:** Please see description for RxUAddr4, pin 73. ***NOTE:*** *The user should tie this pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
76	RxUClav	O	**Receive UTOPIA—Cell Available:** The Receive UTOPIA Interface block will assert this output pin in order to indicate that the Rx FIFO has some ATM cell data that needs to be read by the ATM Layer Processor. The exact functionality of this pin depends upon whether the UNI is operating in the "Octet Level" or "Cell Level" handshake mode. **Octet Level Handshaking Mode** When the Receive UTOPIA Interface block is operating in the "octet-level handshaking" mode; this signal is asserted (toggles "High") when at least one byte of cell data exists within the RxFIFO (within the Receive UTOPIA Interface block). This output pin will toggle "Low" if the RxFIFO is depleted of ATM cell data. **Cell Level Handshaking Mode** When the Receive UTOPIA Interface block is operating in the "cell-level handshaking" mode; this signal is asserted if the RxFIFO contains at least one full cell of data. This signal will toggle "Low" if the RxFIFO is depleted of data, or if it contains less than one full cell of data. **Multi-PHY Operation:** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the RxUClk cycle following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents on the Receive UTOPIA Address bus pins match that with the Receive UTOPIA Address Register). Afterwards, this output pin will behave in accordance with the cell-level handshake mode. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
77	RxUAddr2	I	**Receive UTOPIA Address Bus input:** Please see description for RxUAddr4, pin 73. ***NOTE:*** *The user should tie this pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
78	VDD	****	**Power Supply Pin**
79	RxUAddr0	I	**Receive UTOPIA Address Bus input - LSB:** Please see description for RxUAddr4, pin 73. ***NOTE:*** *The user should tie this pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel Framer" Mode.*
80	RxUAddr1	I	**Receive UTOPIA Address Bus input:** Please see description for RxUAddr4, pin 73. ***NOTE:*** *The user should tie this pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel Framer" Mode.*
81	$\overline{\text{RxUEn}}$	I	**Receive UTOPIA Interface—Output Enable:** This active-"Low" input signal is used to control the drivers of the Receive UTOPIA Data Bus. When this signal is "High" (negated) then the Receive UTOPIA Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the "front of the RxFIFO" will be "popped" and placed on the Receive UTOPIA Data bus on the very next rising edge of RxUClk. ***NOTE:*** *The user should tie this pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
82	TCK	I	**Test Clock:** Boundry Scan clock input. ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
83	TMS	I	**Test Mode Select:** Boundry Scan Mode Select input. ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
84	TDI	I	**Test Data In:** Boundry Scan Test data input. ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
85	TDO	O	**Test Data Out:** Boundry Scan test data output.
86	RLOS	I	**Receive LOS (Loss of Signal) Indicator Input (from XRT7300 E3/DS3/ STS-1 Line Interface Unit).** This input pin is intended to be connected to the RLOS (Receive Loss of Signal) output pin of the XRT7300 E3/DS3 /STS-1 Line Interface IC. The user can monitor the state of this pin by reading the state of Bit 0 (RLOS) within the Line Interface Scan Register (Address = 73h). If this input pin is "Low", then it means that the XRT7300 is detecting a sufficient amount of signal energy on the line, due to the incoming DS3 data-stream. However, if this input pin is "High", then it means that the XRT7300 is not detecting a sufficient amount of signal energy on the line, due to the incoming DS3 data-stream, and may be experiencing a "Loss of Signal" condition. For more information on the operation of the XRT7300 E3/DS3/STS-1 Line Interface Unit IC, please consult the "XRT7300 " data sheet. ***NOTE:*** *Asserting the RLOS input pin will cause the XRT72L71 DS3 UNI to declare an "LOS" (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.*
87	8KRef	I	**8 kHz Reference Clock Input for the PLCP Processors:** The Transmit PLCP processor can be configured to synchronize its PLCP frame processing to this clock signal. The Transmit PLCP Processor will also use this signal to compute the trailer nibble stuff opportunities. ***NOTES:*** 1. *This input signal is active only if the user has configured the PLCP Processors to use this signal as their "master clock" signal. The user can configure the UNI to use this signal by setting TimRefSel[1,0] (within the UNI Operating Mode Register) to 01.* 2. *The user should tie this pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
88	RxLOS	O	**Receive DS3 Framer—Loss of Signal Output Indicator:** This pin is asserted when the Receive DS3 Framer encounters 180 consecutive 0's via the RxPOS and RxNEG pins. This pin will be negated once the Receive DS3 Framer has detected at least 60 "1s" out of 180 consecutive bits.
89	RxOH	O	**Receive Overhead Output Port** All overhead bits, which are received via the "Receive Section" of the Framer IC; will be output via this output pin, upon the rising edge of RxOHClk.
90	RxOOF	O	**Receiver DS3 Framer—"Out of Frame" Indicator:** The Receive DS3 Framer-block will assert this output signal (e.g., pull it "High") whenever it has declared an "Out of Frame" (OOF) condition with the incoming DS3 frames. This signal is negated when the framer correctly locates the F- and M-bits and regains synchronization with the DS3 frame.
91	GND	***	**Ground Signal Pin**

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
92	RxAIS	O	**Receive "Alarm Indication Signal" Output pin:** The UNI/Framer IC will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 data stream. An "AIS" is detected if the payload consists of the recurring pattern of 1010... and this pattern persists for 63 M-frames. An additional requirement for AIS indication is that the C-bits are set to 0, and the X-bits are set to 1. This pin will be negated when a sufficient number of frames, not exhibiting the "1010..." pattern in the payload has been detected.
93	RxOHClk	O	**Receive Overhead Output Clock Signal:** This pin serves as the clock signal for external device to sample the Overhead data on the RxOH pin. The external interface should use the rising edge of this clock to sample the OH data on RxOH pin.
94	RxOHInd/ RxPFrame	O	**Receive Overhead Bit Indicator/PLCP Frame Boundary Indicator Output—Receive PLCP Processor.** The exact functionality of this output pin depends upon whether the XRT72L71 UNI/Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode - RxOHInd:** In clear channel mode, this pin is pulsed "High" for one bit period whenever an over-head bit is being output via the RxSerData output pin. In other words, the "RxSerData" output pin will contain an over-head if this pin is sampled "High". **ATM UNI Mode:** This output pin pulses "High" when the Receive PLCP Processor is receiving the last bit of a given PLCP frame.
95	RxOHFrame	O	**Receive Overhead Frame Boundary Indicator:** This pin is pulsed "High" for one RxOHClk period whenever the first 'X' bit is output on RxOH pin. If external device samples this pin "High" on the rising edge of RxOHClk, the data on RxOH is 'X' bit (first OH bit in the received DS3 frame).
96	RxFrame	O	**Receive Boundary of DS3 Frame Output Indicator:** The exact functionality of this output pin depends upon whether the XRT72L71 UNI/Framer IC is operating in the Clear Channel or ATM UNI Mode. **Clear Channel Mode:** In clear channel mode this pin is pulsed "High" for one DS3 clock period whenever the 'X' bit (first OH bit in the DS3 frame) of the frame is being output on the RxSer pin. RxSer will contain 'X' bit (first OH bit of DS3 frame) if this pin is sampled "High". **ATM UNI Mode:** In the ATM UNI mode, this signal indicates the start of the received DS3 frame and is "High" for one DS3 clock period.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
97	RxPOS	I	**Receive Positive Data Input:** The exact role of this input pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin functions as the "Single-Rail" input for the "incoming" DS3 data stream. The signal at this input pin will be sampled and latched (into the Receive DS3 Framer) on the "user-selected" edge of the RxLineClk signal. **Bipolar Mode:** This input functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxNEG functions as the other dual rail input for the UNI. When this input pin is asserted, it means that the LIU has received a "positive polarity" pulse from the line.
98	RxNEG	I	**Receive Negative Data Input:** The exact role of this input pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin is inactive, and should be pulled ("Low" or "High") when the UNI is operating in the Unipolar Mode. **Bipolar Mode:** This input pin functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS functions as the other dual rail input for the UNI. When this input pin is asserted, it means that the LIU has received a "negative polarity" pulse from the line.
99	RxLineClk	I	**Receive LIU (Recovered) Clock Input:** This input signal serves three purposes: 1. The Receive DS3 Framer uses it to sample and "latch" the signals at the RxPOS and RxNEG input pins (into the Receive DS3 Framer circuitry). 2. This input signal functions as the timing reference for the Receive Framer block. 3. The Transmit DS3 Framer block can be configured to use this input signal as its timing reference. ***NOTE:*** *Note: This signal is the recovered clock from the external DS3 LIU (Line Interface Unit) IC, which is derived from the incoming DS3 data.*
100	RxPRed	O	**Receiver Red Alarm Indicator—Receive PLCP Processor:** The UNI asserts this output pin to denote that one of the following events has been detected by the Receive PLCP Processor: • OOF—Out of Frame Condition • LOF—Loss of Frame Condition ***NOTE:*** *This output pin is only active whenever the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
101	RxRed	O	**Receiver Red Alarm Indicator—Receive DS3 Framer:** The UNI asserts this output pin to denote that one of the following conditions is currently being declared by the Receive DS3 Framer block: • LOS—Loss of Signal Condition • OOF—Out of Frame Condition • AIS—Alarm Indication Signal Detection ***NOTE:*** *This output pin is effectively, the "Wired-OR" of the "RxLOS", the "RxOOF" and the "RxAIS" output pins.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
102	StuffCtl	I	**External PLCP Frame Stuff Control:** This input allows the user to externally exercise or forego trailer nibble stuffing opportunities by the Transmit PLCP Processor. PLCP trailer nibble stuff opportunities occur in periods of three PLCP frames (375µs). The first PLCP frame (first within a "stuff opportunity" period) will have 13 trailer nibbles appended to it. The second PLCP frame (second within a "stuff opportunity" period) will have 14 trailer nibbles appended to it. The third PLCP frame (the location of the stuff opportunity) will contain 13 trailer nibbles if the StuffCtl input is "Low" and 14 trailer nibbles is the StuffCtl input is "High". ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
103	TxInClk	I	**Transmit DS3 Framer Block—Clock Signal:** The Transmit DS3 Framer can be configured to use this input signal as the timing reference. If this input pin is chosen to be the timing reference, then the user must supply a "High" quality 44.736 MHz signal to this input pin. In this configuration, frame generation, by the Transmit DS3 Framer, will be asynchronous (with any other timing signals within the UNI). However, frame timing will be based upon this clock signal. ***NOTE:*** *This input pin should be tied to "GND" if it is not used as the Transmit DS3 Framer timing reference.*
104	RxPLOF	O	**Receive PLCP—"Loss of Frame" Output Indicator:** The Receive PLCP Processor will assert this pin, when it declares a "Loss of Frame" condition. This output will be negated when the Receive PLCP Processor reaches the "In Frame" Condition. ***NOTE:*** *This output pin is only active if the user has configured the XRT72L71 to operate in the "ATM UNI" Mode.*
105	GND	***	**Ground Signal Pin**
106	RxPOOF	O	**Receive PLCP "Out of Frame" Indicator:** The Receive PLCP Processor will assert this pin, when it declares an "Out of Frame" condition. This output will be negated when the Receive PLCP Processor reaches the "In Frame" Condition. ***NOTE:*** *This output pin is only active if the user has configured the XRT72L71 to operate in the "ATM UNI" Mode.*
107	TxFrameRef	I	**Transmit DS3 Framer—Frame Reference Input Pin:** The Transmit DS3 Framer can be configured to use this input signal as the "framing" reference for the Transmit DS3 Framer block. If this input pin is chosen to be the timing reference, then any rising edge at this input will cause the Transmit DS3 Framer to begin its creation a new DS3 M-frame. Consequently, the user must supply a clock signal that is equivalent to the DS3 Frame rate (or 9398.3 Hz). Further, the signal which is driving this input pin, must be synchronized witht he 44.736MHz clock signal, which is applied to the "TxInClk" input pin. ***NOTE:*** *This input pin should be tied to "GND" if it is not used as the Transmit DS3 Framer frame reference signal.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
108	TxOHInd/ TxPFrame	O	**Transmit Overhead Data Indicator/Transmit PLCP Frame Boundary Indicator—Output:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In the Clear Channel Mode, this pin serves as the transmit OH Indication for the external interface. This pin is pulsed for one bit period of DS3 clock to indicate to the external device that the transmit input interface is going to process OH data at the rising edge of next clock. When the external interface samples TxOHInd as "High" With the rising edge of DS3 Clk; it is expected NOT to provide useful payload data bit on TxSer pin. Instead it can provide corresponding OH data bit on TxSer input. However, in that case the user has to program a register bit to configure XRT72L71 to accept the OH data from the TxSer input. Otherwise, the OH data will be geaerated internally or be taken from the TxOH pin if TxOHIns is "High". This pin is pulsed "High" for one bit period prior to all DS3 OH bit positions. **ATM UNI Mode:** In ATM UNI mode of operation, this pin functions as Transmit PLCP Frame signal which pulses "High" once for each outbound PLCP frame, when the last nibble is being routed.
109	TxPOS	O	**Transmit Positive Polarity Pulse:** The exact role of this output pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output pin functions as the "Single-Rail" output signal for the "outbound" DS3 data stream. The signal, at this output pin, will be updated on the "user-selected" edge of the TxLineClk signal. **Bipolar Mode:** This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPDATA input of the external DS3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line.
110	TxPOHFrame	O	**Transmit PLCP Frame Path Overhead Byte Serial Input Port—Beginning of Frame indicator.** This output pin, along with the TxPOH, TxPOHClk, and TxPOHIns pins comprise the "Transmit PLCP Frame POH Byte Insertion" serial input port. This particular pin will pulse "High" when the "Transmit PLCP POH Byte Insertion" serial input port is expecting the first bit of the Z6 byte at the TxPOH input pin. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
111	TxNEG	O	**Transmit Negative Polarity Pulse:** The exact role of this output pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output signal pulses "High" for one bit period, at the end of each "outbound" DS3 frame. This output signal is at a logic "Low" for all of the remaining bit-periods of the "outbound" DS3 frames. **Bipolar Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNDATA input of the external DS3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
112	TxLineClk	O	**Transmit Line Interface Clock:** This clock signal is output to the Line Interface Unit, along with the TxPOS and TxNEG signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The user can configure the source of this clock to be either the RxLineClk (from the Receiver portion of the UNI) or the TxlineClk input. The nominal frequency of this clock signal is 44.736 MHz.
113	VDD	***	**Power Supply Pin**
114	TxSerData/ TxPOH	I	**Transmit Serial Payload Data Input/Transmit PLCP Frame POH Byte Insertion Serial Input:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In clear channel mode, this pin can be used by the external interface to provide the serial input data (payload and OH) that has to be mapped in outgoing DS3 frame. If user want to insert OH data on TxSer pin then the user should configure the XRT72L71 accordingly. **ATM UNI Mode:** This input pin becomes active when the user asserts the TxPOHIns input pin. When this happens the user will be permitted to serially input their own value for PLCP POH bytes into the "outbound" PLCP frame. This data will be clocked into the UNI Framer via the TxPOHClk output signal. This UNI will also assert the TxPOHMSB output pin when it expects the MSB (Most significant bit) of the Z6 Byte (within the PLCP frame).
115	TxAISEn	I	**Transmit AIS Pattern input:** When this input pin is pulled "High" then the Transmit DS3 Framer block will insert the AIS pattern into the DS3 output data stream.
116	TxPOHIns	I	**Transmit PLCP Frame POH Data Insert Enable:** This input can be asserted to allow the user to input his/her own value for the PLCP POH bytes via the TxPOH input pin, in each PLCP frame, prior to transmission. If this input pin is not asserted, then the UNI will generate its own PLCP POH bytes. ***NOTE:*** *The user should tie this input pin to "GND" if the XRT72L71 is going to be configured to operate in either the "Clear-Channel-Framer" Mode or in the "Direct-Mapped ATM" Mode.*
117	TxOHIns	I	**Transmit Overhead Data Insert Input:** The function of this pin is the same in both Clear Channel and ATM UNI Modes of the XRT72L71. This pin is used to indicate if the OH bit should be taken from the external interface. The OH data on TxOH will be considered by the only if this pin is "High" during OH positions.
118	TxPOHClk	O	**Transmit PLCP Frame POH Byte Insertion Clock:** This pin, along with the TxPOH and the TxPOHMSB input pins, function as the "Transmit PLCP Frame POH Byte" serial input port. This output pin functions as a clock output signal that is used to sample the user's POH data at the TxPOH input pin. This output pin is always active, independent of the state of the "TxPOHIns" pin. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
119	TxOH	I	**Transmit Overhead Input Pin** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the "overhead" bit position within the very next "outbound" DS3 frame. If the "TxOHIns" pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the "TxOHClk" output pin. Conversely, if the "TxOHIns" pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
120	TxCellTxed	O	**Transmit Cell Processor—Cell Transmitted Indicator:** This output pin pulses “High” each time the Transmit Cell Processor transmits a cell to the Transmit PLCP Processor (or Transmit DS3 Framer). ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the “ATM UNI” Mode.*
121	TxOHClk	O	**Transmit Overhead Clock:** The function of this pin is the same in both Clear Channel and ATM UNI Modes of the XRT72L71. This pin serves as the clock signal for the external interface to insert the OH data on the TxOH pin. The user can insert OH data on the TxOH pin at the rising edge of this clock signal.
122	TxOHFrame	O	**Transmit Overhead Framing Pulse:** The function of this pin is same in both Clear Channel and ATM UNI modes of XRT72L71. When the external interface samples this pin "High" at the rising edge of TxOHClk, it should provide 'X' bit (first OH bit within DS3 frame) on the TxOH pin. This signal is "High" for one TxOHClk duration and repeats once for each DS3 frame.
123	$\overline{\text{TxUEn}}$	I	**Transmit UTOPIA Interface Block—Write Enable:** This active-”Low” signal, from the ATM Layer processor enables the data on the Transmit UTOPIA Data Bus to be written into the TxFIFO on the rising edge of TxUClk. When this signal is asserted, then the contents of the byte or word that is present, on the Transmit UTOPIA Data Bus, will be latched into the Transmit UTOPIA Interface block, on the rising edge of TxUClk. When this signal is negated, then the Transmit UTOPIA Data bus inputs will be tri-stated. ***NOTE:*** *The user should tie this input pin to “GND” whenever the XRT72L71 has been configured to operate in the “Clear-Channel-Framer” Mode.*
124	TxUSoC	I	**Transmitter—Start of Cell (SoC) Indicator Input:** This input pin is driven by the ATM Layer processor and is used to indicate the start of an ATM cell that is being transmitted from the ATM layer processor. This input pin must be pulsed “High” when the first byte (or word) of a new cell is present on the Transmit UTOPIA Data Bus. This input pin must remain “Low” at all other times. ***NOTE:*** *The user should tie this input pin to “GND” whenever the XRT72L71 has been configured to operate in the “Clear-Channel-Framer” Mode.*
125	TxUPrty	I	**Transmit UTOPIA Data Bus—Parity Input:** The ATM Layer processor will apply the parity value of the byte or word which is being applied to the Transmit UTOPIA Data Bus (e.g., TxUData[7:0] or TxUData[15:0]) inputs of the UNI, respectively. Note: this parity value should be computed based upon the odd-parity of the data applied at the Transmit UTOPIA Data Bus. The Transmit UTOPIA Interface block (within the UNI) will independently compute an odd-parity value of each byte (or word) that it receives from the ATM Layer processor and will compare it with the logic level of this input pin. ***NOTE:*** *The user should tie this input pin to “GND” whenever the XRT72L71 has been configured to operate in the “Clear-Channel-Framer” Mode.*

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
126	TxUClav	O	**Transmit UTOPIA Interface—Cell Available Output Pin:** This output pin supports data flow control between the ATM Layer processor and the Transmit UTOPIA Interface block. The exact functionality of this pin depends upon whether the UNI is operating in the "Octet Level" or "Cell Level" handshaking mode. **Octet Level Handshaking:** When the Transmit UTOPIA Interface block is operating in the octet-level handshaking mode, this signal is negated (toggles "Low") when the TxFIFO is not capable of handling four more write operations; by the ATM Layer processor to the Transmit UTOPIA Interface block. This signal will be asserted when the TxFIFO is capable of receiving four or more write operations of ATM cell data. **Cell Level Handshaking:** When the Transmit UTOPIA Interface block is operating the cell-level handshaking mode, this signal is asserted (toggles "High") when the TxFIFO is capable of receiving at least one more full cell of data from the ATM Layer processor. This signal is negated, if the TxFIFO is not capable of receiving one more full cell of data from the ATM Layer processor. **Multi-PHY Operation:** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the TxUClk cycle following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., when the contents on the Transmit UTOPIA Address bus pins match that within the Transmit UTOPIA Address Register). Afterwards, this output pin will behave in accordance with the cell-level handshake mode. ***NOTE:*** *This output pin is only active if the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
127	GND	***	Ground Signal Pin.
128 129 130 131 132 133 134 135	TxUData8 TxUData0 TxUData9 TxUData1 TxUData10 TxUData2 TxUData11 TxUData3	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15, pin 144. ***NOTES:****The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.* *TxUData0 - Transmit UTOPIA Data Bus Input - LSB.*
136	VDD	***	**Power Supply Pin**
137 138 139 140 141 142 143	TxUData4 TxUData12 TxUData5 TxUData13 TxUData6 TxUData14 TxUData7	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
144	TxUData15	I	**Transmit UTOPIA Data Bus Input—MSB:** This input pin, along with TxUData14 through TxUData0 comprise the Transmit UTOPIA Data Bus input pins. When the ATM Layer Processor wishes to transmit ATM cell data through the XRT72L71 DS3 UNI, it must place this data on these pins. The data, on the Transmit UTOPIA Data Bus is latched into the Transmit UTOPIA Interface block on the rising edge of TxUClk. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
145	VDD	***	**Power Supply Pin**

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
146	TxUAddr4	I	**Transmit UTOPIA Address Bus—MSB Input:** This input pin, along with TxUAddr3 through TxUAddr0 comprise the Transmit UTOPIA Address Bus input pins. The Transmit UTOPIA Address Bus is only in use when the UNI is operating in the M-PHY mode. When the ATM Layer processor wishes to write data to a particular UNI device, it will provide the address of the "intended UNI" on the Transmit UTOPIA Address Bus. The contents of the Transmit UTOPIA Address Bus input pins are sampled on the rising edge of TxUClk. The DS3 UNI will compare the data on the Transmit UTOPIA Address Bus with the pre-programmed contents of the TxUT Address Register (Address = 70h). If these two values are identical and the $\overline{\text{TxUEN}}$ pin is asserted, then the TxUClav pin will be driven to the appropriate state (based upon the TxFIFO fill level) for the Cell Level handshake mode of operation. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in either the "Clear-Channel-Framer" Mode or in the "Single-PHY" Mode.*
147	TxUAddr0	I	**Transmit UTOPIA Address Bus Input—LSB:** (See Description for TxUAddr4 pin 146). ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in either the "Clear-Channel-Framer" Mode or in the "Single-PHY" Mode.*
148 149 150	TxUAddr3 TxUAddr1 TxUAddr2	I	**Transmit UTOPIA Address Bus Input:** Please see description for TxUAddr4, pin 146. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in either the "Clear-Channel-Framer" Mode or in the "Single-PHY" Mode.*
151	TxUClk	I	**Transmit UTOPIA Interface Clock:** The Transmit UTOPIA Interface clock is used to latch the data on the Transmit UTOPIA Data bus, into the Transmit UTOPIA Interface block. This clock signal is also used as the timing source for circuitry used to process the ATM cell data into and through the TxFIFO. During Multi-PHY operation, the data on the Transmit UTOPIA Address bus pins is sampled on the rising edge of TxUClk. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L71 has been configured to operate in the "Clear-Channel-Framer" Mode.*
152	GND	***	**Ground Signal Pin**
153	TestMode	***	**Factory Test Mode Pin** ***NOTE:*** *The user should tie this pin to ground.*
154	TxGFCMSB	O	**Transmit GFC Nibble-Field Serial Input Port—MSB Indicator:** This signal, along with TxGFC and TxGFCClk combine to function as the "Transmit GFC Nibble Field" serial input port. This output signal will pulse "High" when the MSB (most significant bit) of the GFC Nibble (for a given cell) is expected at the TxGFC input pin. ***NOTE:*** *This output pin is only active whenever the XRT72L71 has been configured to operate in the "ATM UNI" Mode.*
155	$\overline{\text{Reset}}$	I	**Reset Input:** When this active-"Low" signal is asserted, the UNI Framer will be asynchronously reset. Additionally, all outputs will be "tri-stated", and all on-chip registers will be reset to their default values.