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XRT7300

E3/DS3/STS-1 LINE INTERFACE UNIT

MAY 2011 *REV. 1.1.2*

GENERAL DESCRIPTION

The XRT7300 DS3/E3/STS-1 Line Interface Unit is designed to be used in DS3, E3 or SONET STS-1 applications and consists of a line transmitter and receiver integrated on a single chip.

XRT7300 can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates.

In the transmit direction, the XRT7300 encodes input data to either B3ZS (for DS3/STS-1 applications) or HDB3 (for E3 applications) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction the XRT7300 performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of line code violations.

The XRT7300 also contains a 4-Wire Microprocessor Serial Interface for accessing the on-chip Command registers.

FEATURES

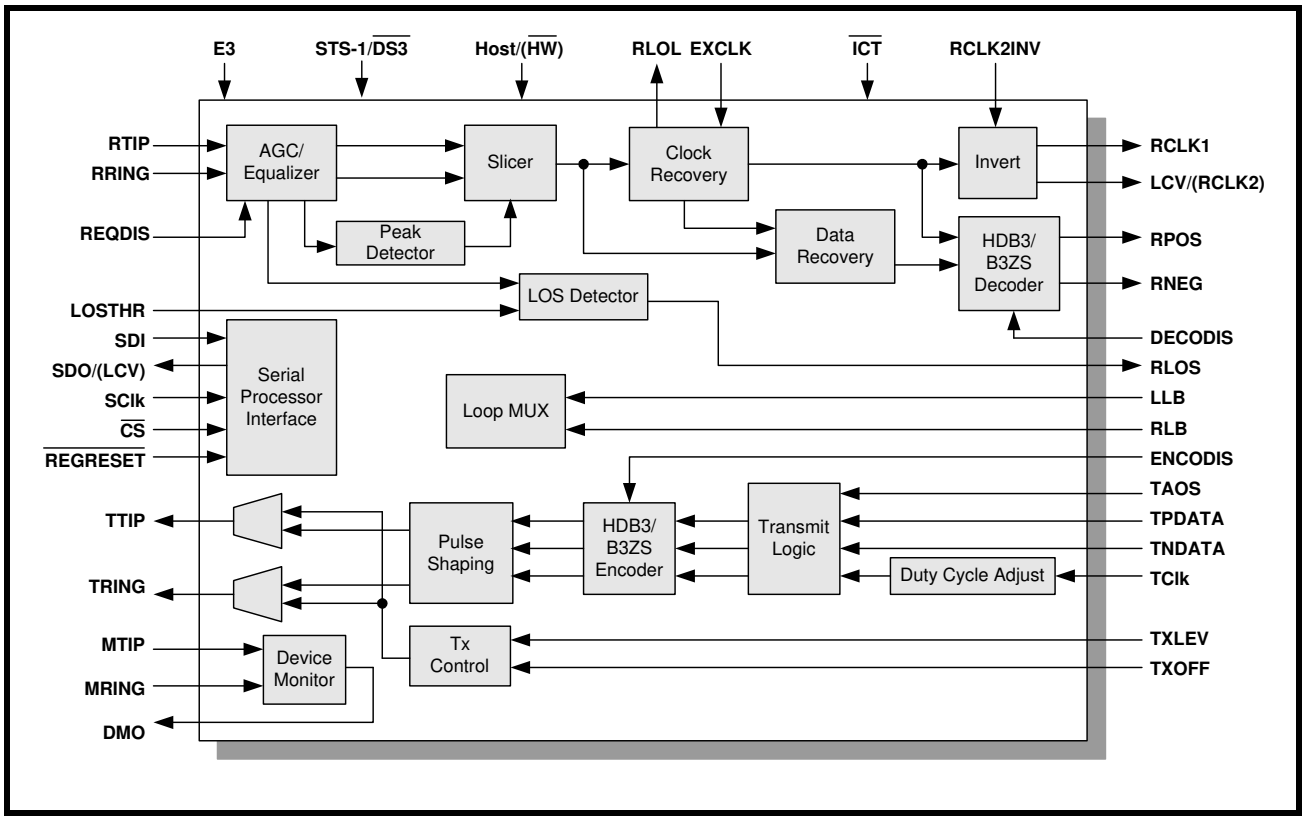
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Contains a 4-Wire Microprocessor Serial Interface
- Uses Minimum External components
- Requires Single +5V Power Supply
- -40°C to +85°C Operating Temperature Range
- Available in a 44 pin TQFP package

APPLICATIONS

- Interfaces to E3, DS3 or SONET STS-1 Networks
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

NOTE: *This Device is Protected by US Patent # 6,157,270*

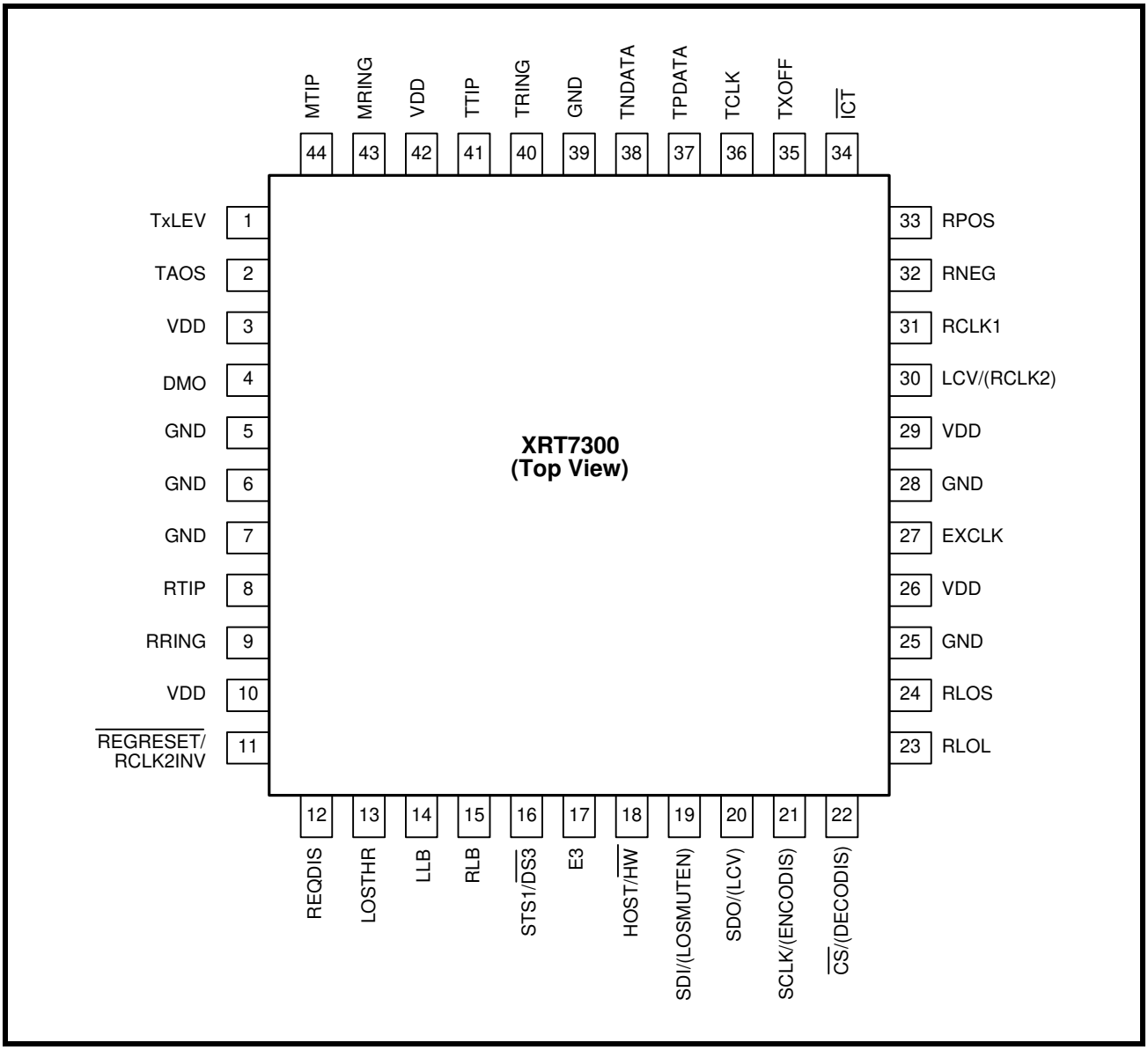
FIGURE 1. BLOCK DIAGRAM OF THE XRT7300



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT7300IV	44 Pin TQFP (10mm x 10mm)	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT7300 IN THE 44 PIN TQFP



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PIN DESCRIPTION

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
1	TXLEV	I	**Transmit Line Build-Out Enable/Disable Select:** This input pin is used to enable or disable the Transmit Line Build-Out circuit in the XRT7300. Setting this pin to “High” disables the Line Build-Out circuit. In this mode, the XRT7300 outputs partially shaped pulses onto the line via the TTIP and TRING output pins. Setting this pin to “Low” enables the Line Build-Out circuit. In this mode, the XRT7300 outputs partially-shaped pulses onto the line via the TTIP and TRING output pins. To comply with the isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-Core or Bellcore GR-253-Core: 1. Set this input pin to a "1" if the cable length between the Cross-Connect and the transmit output of the XRT7300 is greater than 225 feet. 2. Set this input pin to a "0" if the cable length between the Cross-Connect and the transmit output of the XRT7300 is less than 225 feet. This pin is active only if both of the following are true: (a) The XRT7300 is configured to operate in either the DS3 or SONET STS-1 modes and (b) The XRT7300 is configured to operate in the Hardware Mode. ***NOTE:*** *This pin should be tied to GND if the XRT7300 is to be operated in the HOST mode.*
2	TAOS	I	**Transmit All Ones Select:** A “High” on this pin causes a continuous AMI all “1’s” pattern to be transmitted onto the line. The frequency of this “1’s” pattern is determined by TCLK. ***NOTES:*** *1. This input pin is ignored if the XRT7300 is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT7300 is going to be operating in the HOST Mode.*
3	VDD	****	**Transmit Digital Power Supply**
4	DMO	O	**Drive Monitor Output:** If no transmitted AMI signal is present on MTIP and MRING input pins for 128±32 TCLK periods, then the DMO pin toggles and remains “High” until the next AMI signal is detected.
5	GND	****	**Transmit Digital GND**
6	GND	****	**Analog GND (Substrate)**
7	GND	****	**Receive Analog GND**
8	RTIP	I	**Receive TIP Input:** This input pin along with RRING is used to receive the line signal from the Remote DS3/E3/STS-1 Terminal.
9	RRING	I	**Receive RING Input:** This input pin along with RTIP is used to receive the line signal from the Remote DS3/E3/STS-1 Terminal.
10	VDD	****	**Receive Analog VDD**

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
11	$\overline{\text{REGRESET}}$/ (RCLK2INV)	I	**Register Reset Input pin (Invert RCLK2 Output - Select):** The function of this pin depends upon whether the XRT7300 is operating in the HOST Mode or in the Hardware Mode. **HOST Mode - Register Reset Input pin:** Setting this input pin "Low" causes the XRT7300 to reset the contents of the Command Registers to their default settings and operating configuration. This pin is internally pulled "High". **Hardware Mode - Invert RCLK2 Output Select:** Setting this input pin "Low" configures the Receive Section of the XRT7300 to output the recovered data via the RPOS and RNEG output pins on the rising edge of the RCLK2 output signal. Setting this input pin "High" configures the Receive Section to output the recovered data on the falling edge of the RCLK2 output signal.
12	REQDIS	I	**Receive Equalization Disable Input:** Setting this input pin "High" disables the Internal Receive Equalizer in the XRT7300. Setting this pin "Low" enables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTES:*** *1. This input pin is ignored if the XRT7300 is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT7300 is going to be operating in the HOST Mode.*
13	LOSTHR	I	**Loss of Signal Threshold Control:** The voltage forced on this pin controls the input loss of signal (LOS) threshold. Two settings are provided by forcing this signal to either GND or VDD. ***NOTE:*** *This pin is only applicable during DS3 or STS-1 operations.*
14	LLB	I	**Local Loop-Back Select:** This input pin along with RLB dictates which Loop-Back mode the XRT7300 is operating in. A "High" on this pin with RLB being set to "Low" configures the XRT7300 to operate in the Analog Local Loop-Back Mode. A "High" on this pin with RLB also being set to "High" configures the XRT7300 to operate in the Digital Local Loop-Back Mode. ***NOTES:*** *1. This input pin is ignored if the XRT7300 is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT7300 is going to be operating in the HOST Mode.*
15	RLB	I	**Remote Loop-Back Select:** This input pin along with LLB dictates which Loop-Back mode the XRT7300 is be operating in. A "High" on this pin with LLB being set to "Low" configures the XRT7300 to operate in the Remote Loop-Back Mode. A "High" on this pin with LLB also being set to "High" configures the XRT7300 to operate in the Digital Local Loop-Back Mode. ***NOTES:*** *1. This input pin is ignored if the XRT7300 is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT7300 is going to be operating in the HOST Mode.*

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
16	STS-1/$\overline{DS3}$	I	**STS-1/$\overline{DS3}$ Select Input:** A "High" on this pin configures the Clock Recovery Phase Locked Loop to set its VCO Center frequency to around 51.84 MHz (optimal for SONET STS-1 operations). A "Low" on this pin configures the Clock Recovery Phase Locked Loop to set its VCO Center frequency to around 44.736 MHz (optimal for DS3 operations). ***NOTES:*** *1. The XRT7300 ignores this pin if the E3 pin (pin 17) is set to "1".* *2. This input pin is ignored if the XRT7300 is operating in the HOST Mode.* *3. Tie this pin to GND if the XRT7300 is going to be operating in the HOST Mode.*
17	E3	I	**E3 Select Input:** A "High" on this pin configures the XRT7300 to operate in the E3 Mode. A "Low" on this pin configures the XRT7300 to check the state of the STS-1/$\overline{DS3}$ input pin. ***NOTES:*** *1. This input pin is ignored if the XRT7300 is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT7300 is going to be operating in the HOST Mode.*
18	HOST/$\overline{HW}$	I	**HOST/$\overline{HW}$ Mode Select:** This input pin is used to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SCLK, $\overline{CS}$ and $\overline{REGRESET}$ pins). Setting this input pin "High" enables the Microprocessor Serial Interface (e.g. configures the XRT7300 to operate in the HOST Mode). In this mode, the XRT7300 is configured by writing data into the on-chip Command Registers via the Microprocessor Serial Interface. When the XRT7300 is operating in the HOST Mode, it ignores the states of many of the discrete input pins. Setting this input pin "Low" disables the Microprocessor Serial Interface (e.g., configures the XRT7300 to operate in the Hardware Mode). In this mode, many of the external input control pins are functional.
19	SDI/ (LOSMUTEN)	I	**Serial Data Input for the Microprocessor Serial Interface (HOST Mode) or MUTE-upon-LOS Enable Input (Hardware Mode):** The function of this input pin depends upon whether the XRT7300 is operating in the HOST or the Hardware Mode. **Serial Data Input for the Microprocessor Serial Interface (HOST Mode):** This pin is used to read or write data into the Command Registers of the Microprocessor Serial Interface. The Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations are applied to this pin. This input is sampled on the rising edge of the SCLK pin (pin 21). **MUTE-upon-LOS Enable Input (Hardware Mode):** When in the Hardware Mode, this input pin is used to configure the XRT7300 to MUTE the recovered data via the RPOS and RNEG output pins whenever it declares an LOS condition. Setting this input pin "High" configures the XRT7300 to automatically pull the RPOS and RNEG output pins to GND whenever it is declaring an LOS condition, thereby MUTing the data being output to the Terminal Equipment. Setting this input pin "Low" configures the XRT7300 to NOT automatically MUTE the recovered data whenever an LOS condition is declared.

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
20	SDO/(LCV)	O	**Serial Data Output from the Controller Port/(Line Code Violation Output (LCV) Indicator.):** The function of this input pin depends upon whether the XRT7300 is operating in the HOST or the Hardware Mode. **HOST Mode - Microprocessor Serial Interface - Serial Data Output.** This pin serially outputs the contents of the specified Command Register during Read Operations. The data on this pin is updated on the falling edge of the SCLK input signal. This pin is tri-stated upon completion of data transfer. **Hardware Mode - Line Code Violation Output Indicator.** This pin pulses "High" for one bit period any time the Receive Section of the XRT7300 detects a Line Code Violation in the incoming E3, DS3 or STS-1 Data Stream.
21	SCLK/(ENCO-DIS)	I	**Microprocessor Serial Interface Clock Signal/Encoder Disable:** **HOST Mode - Microprocessor Serial Interface Clock Signal** This signal is used to sample the data on the SDI pin on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. **Hardware Mode - B3ZS/HDB3 Encoder Disable** Setting this input pin "High" disables the B3ZS/HDB3 Encoder and configures the XRT7300 to transmit the line signal in an AMI Format. Setting this input pin "Low" enables the B3ZS/HDB3 Encoder and configures the XRT7300 to transmit the line signal in the B3ZS format (for DS3/STS-1 operation) or in the HDB3 format (for E3 operation).
22	$\overline{CS}$/(DECODIS)	I	**Microprocessor Serial Interface - Chip Select/Decoder Disable** The function of this input pin depends upon whether the XRT7300 is operating in the HOST or the Hardware Mode. **HOST Mode - Chip Select Input:** The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT7300 via the Microprocessor Serial Interface. **Hardware Mode - (B3ZS/HDB3 Decoder Disable)** Setting this input pin "High" disables the B3ZS/HDB3 Decoder. Setting this input pin "Low" enables the B3ZS/HDB3 Decoder.
23	RLOL	O	**Receive Loss of Lock Output Indicator** This output pin toggles "High" if the XRT7300 has detected a Loss of Lock Condition. The XRT7300 declares an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXCLK input pin) by more than 0.5%.
24	RLOS	O	**Receive Loss of Signal Output Indicator** This output pin toggles "High" if the XRT7300 has detected a Loss of Signal Condition in the incoming line signal. The criteria the XRT7300 uses to declare an LOS Condition depends upon whether the device is operating in the E3 or DS3/STS-1 Mode.
25	GND	****	**Digital GND**
26	VDD	****	**Digital VDD**

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
27	EXCLK	I	**External Reference Clock Input:** Apply a 34.368MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications.
28	GND	****	Receiver Digital Ground
29	VDD	****	Receiver Digital VDD
30	LCV/(RCLK2)	O	**Line Code Violation Indicator/Receive Clock Output pin 2:** The function of this pin depends upon whether the XRT7300 is operating in the HOST Mode, the Hardware Mode or User selection. **HOST Mode - Line Code Violation Indicator Output:** If the XRT7300 is configured to operate in the HOST Mode, then this pin functions as the LCV output pin by default. However, by using the on-chip Command Registers, this pin can be configured to function as the second Receive Clock signal output pin (RCLK2). **Hardware Mode - Receive Clock Output pin 2:** This output pin is the Recovered Clock signal from the incoming line signal. The receive section of the XRT7300 outputs data via the RPOS and RNEG output pins on the rising edge of this clock signal. ***NOTE:*** *If the XRT7300 is operating in the HOST Mode and this pin is configured to function as the additional Receive Clock signal output pin, then the XRT7300 can be configured to update the data on the RPOS and RNEG output pins on the falling edge of this clock signal.*
31	RCLK1	O	**Receive Clock Output pin 1:** This output pin is the Recovered Clock signal from the incoming line signal. The receive section of the XRT7300 outputs data via the RPOS and RNEG output pins on the rising edge of this clock signal. ***NOTE:*** *If the XRT7300 device is operating in the "Host" Mode, then the user can configure the device to update the data on the RPOS and RNEG output pins on the falling edge of this clock signal.*
32	RNEG	O	**Receive Negative Pulse Output:** This output pin pulses "High" whenever the XRT7300 has received a Negative Polarity pulse in the incoming line signal at the RTIP/RRING inputs. ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
33	RPOS	O	**Receive Positive Pulse Output:** This output pin pulses "High" whenever the XRT7300 has received a Positive Polarity pulse in the incoming line signal at the RTIP/RRING inputs. ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
34	$\overline{\text{ICT}}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. This pin is internally pulled "High".

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
35	TXOFF	I	**Transmitter OFF Input:** Setting this input pin "High" configures the XRT7300 to turn off the Transmitter in the device. ***NOTES:*** 1. *This input pin is ignored if the XRT7300 is operating in the HOST Mode.* 2. *Tie this pin to GND if the XRT7300 is going to be operating in the HOST Mode.*
36	TCLK	I	**Transmit Clock Input for TPDATA and TNDATA:** This input pin must be driven at 34.368 MHz for E3 applications, 44.736MHz for DS3 applications, or 51.84MHz for SONET STS-1 applications. The XRT7300 uses this signal to sample the TPDATA and TNDATA input pins. By default, the XRT7300 is configured to sample these two pins on the falling edge of this signal. If the XRT7300 is operating in the HOST Mode, then the device can be configured to sample the TPDATA and TNDATA input pins on the rising edge of TCLK.
37	TPDATA	I	**Transmit Positive Data Input:** The XRT73L00 samples this pin on the falling edge of TCLK. If the device samples a "1" at this input pin, then it generates and transmits a positive polarity pulse to the line. ***NOTES:*** 1. *The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* 2. *If the XRT73L00 is operating in the HOST Mode, then the XRT73L00 can be configured to sample the TPDATA pin on either the rising or falling edge of TCLK.*
38	TNDATA	I	**Transmit Negative Data Input:** The XRT7300 samples this pin on the falling edge of TCLK. If the device samples a "1" at this input pin, then it generates and transmits a negative polarity pulse to the line. ***NOTES:*** 1. *This input pin is ignored and should be tied to GND if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* 2. *If the XRT7300 is operating in the HOST Mode, then the XRT7300 can be configured to sample the TNDATA pin on either the rising or falling edge of TCLK.*
39	GND	-	**Transmit Analog Ground**
40	TRING	O	**Transmit RING Output:** The XRT7300 uses this pin, along with TRING, to transmit a bipolar line signal via a 1:1 transformer.
41	TTIP	O	**Transmit TIP Output:** The XRT7300 uses this pin, along with TTIP, to transmit a bipolar line signal via a 1:1 transformer.
42	VDD	-	**Transmit Analog Power Supply**

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
43	MRING	I	**Monitor Ring Input:** The bipolar line output signal from TRING can be connected to this pin via a 270 Ω resistor in order to check for line driver failure. This pin is internally pulled "High".
44	MTIP	I	**Monitor Tip Input:** The bipolar line output signal from TTIP can be connected to this pin via a 270 Ω resistor in order to check for line driver failure. This pin is internally pulled "High".

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (TA = 25°C, VDD = 5.0V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DDD}	DC Supply Voltage	4.75	5	5.25	V
V_{DDA}	DC Supply Voltage	4.75	5	5.25	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all “1’s”)				
	DS-3 Mode		167	200	mA
	STS-1 Mode		180	220	mA
V^{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		VDD	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA	0		0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA	2.8		VDD	V
I_L	Input Leakage Current*			±10	mA

** Not applicable to pins with pull-up/pull-down resistors.*

AC ELECTRICAL CHARACTERISTICS (TA = 25°C, VDD = 5.0V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Terminal Side Timing Parameters (See Figure 3 & Figure 4)					
	TCLK Clock Duty Cycle (DS3/STS-1)	30	50	70	%
	TCLK Clock Duty Cycle (E3)	30	50	70	%
	TCLK Frequency (SONET STS-1)		51.84		MHz
	TCLK Frequency (DS3)		44.736		MHz
	TCLK Frequency (E3)		34.368		MHz
t_{RTX}	TCLK Clock Rise Time (10% to 90%)			4	ns
t_{FTX}	TCLK Clock Fall Time (90% to 10%)			4	ns
t_{TSU}	TPDATA/TNDATA to TCLK Falling Set up time	3			ns
t_{THO}	TPDATA/TNDATA to TCLK Falling Hold time	3			ns
t_{LCVO}	RCLK to rising edge of LCV output delay		2.5		ns
t_{TDY}	TTIP/TRING to TCLK Rising Propagation Delay time	0.6		14	ns
	RCLK Clock Duty Cycle	45	50	55	%
	RCLK Frequency (SONET STS-1)		51.84		MHz
	RCLK Frequency (DS3)		44.736		MHz
	RCLK Frequency (E3)		34.368		MHz

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = 5.0V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{CO}	RCLK to RPOS/RNEG Delay Time			4	ns
t_{RRX}	RCLK Clock Rise Time (10% to 90%)		2	4	ns
t_{FRX}	RCLK Clock Fall Time (10% to 90%)		1.5	3	ns
C_i	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

FIGURE 3. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE

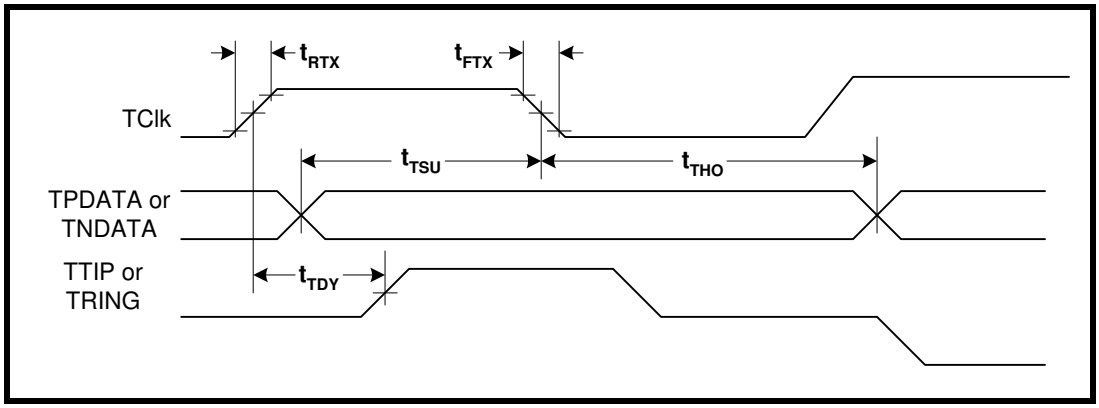
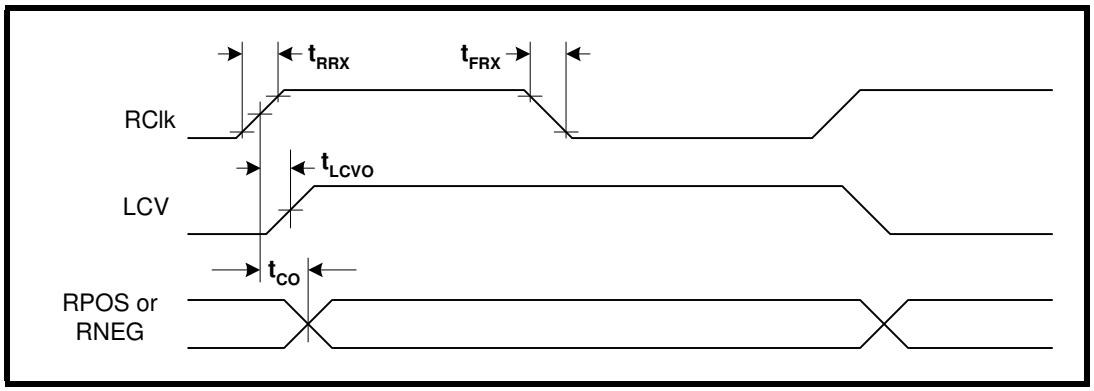


FIGURE 4. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE



AC ELECTRICAL CHARACTERISTICS (CONTINUED) (TA = 25°C, VDD = 5.0V ± 5%, UNLESS OTHERWISE SPECIFIED)

Line Side Parameters

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DS3 Application Parameters **Transmit Line Characteristics (See Figure 5)**					
	Transmit Output Pulse Amplitude (Measured at 0 feet, TXLEV = 0)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured at 0 feet, TXLEV = 1)	0.90	1.0	1.1	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input clock at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of Cable)	900	1000		feet
	Receive Intrinsic Jitter (All One's Pattern)		0.01		UI
	Receive Intrinsic Jitter (100 Pattern) (1)		0.02		UI
LOS Level With Equalizer Enabled (Table 4)					
	Signal Level to Declare Loss of Signal (LOSTHR = 0)			55	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0)	220			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1)			22	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1)	90			mV
LOS Level With Equalizer Disabled (Table 4)					
	Signal Level to Declare Loss of Signal (LOSTHR = 0)			35	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0)	155			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1)			17	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1)	70			mV
	Max Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 1KHz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 10KHz	5			UI
	Max Jitter Tolerance @ Jitter Frequency = 800KHz	0.4			UI

(1) Measured at Nominal DSX3 level, Equalizer enabled, VDD = 5V and TA = 25°C

AC ELECTRICAL CHARACTERISTICS (CONTINUED) (TA = 25°C, VDD = 5.0V ± 5%, UNLESS OTHERWISE SPECIFIED)

Line Side Parameters

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
E3 Application Parameters **Transmit Line Characteristics (See Figure 5)**					
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer)	0.9	1.00	1.1	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input clock at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	1100			feet
	Interference Margin	-20	-17		dB
	Signal Level to Declare Loss of Signal			-35	dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10	100	255	UI
	Termination of LOS to LOS Clearance Time	10	100	255	UI
	Intrinsic Jitter (all "1's" Pattern) (1)		0.01		UI
	Intrinsic Jitter (100 Pattern)		0.03		
	Max Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 1KHz	30			UI
	Max Jitter Tolerance @ Jitter Frequency = 10KHz	4			UI
	Max Jitter Tolerance @ Jitter Frequency = 800KHz	0.15			UI
SONET STS-1 Application Parameters **Transmit Line Characteristics (See Figure 5)**					
	Transmit Output Pulse Amplitude (Measured with TXLEV = 0)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured with TXLEV = 1)	0.93	0.98	1.08	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free clock input at TCLK		0.02	0.05	UIpp

AC ELECTRICAL CHARACTERISTICS (CONTINUED) (TA = 25°C, VDD = 5.0V ± 5%, UNLESS OTHERWISE SPECIFIED)

Line Side Parameters

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	900			feet
	Signal Level to Declare or Clear Loss of Signal (see Table 4)				mV
	Intrinsic Jitter (all "1's" Pattern) (2)		0.03		UI
	Intrinsic Jitter (100 Pattern)		0.03		UI
	Max Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 1KHz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 10KHz	5			UI
	Max Jitter Tolerance @ Jitter Frequency = 800KHz	0.4			UI

(1) Measured with Equalizer enabled, 12db cable attenuation, VDD = 5V and TA = 25°C

(2) Measured at nominal STSX-1 level with Equalizer enabled, VDD = 5V and TA = 25°C

ABSOLUTE MAXIMUM RATINGS

POWER SUPPLY	**-0.5 TO +6.5V**
STORAGE TEMPERATURE	**-65°C TO 150°C**
INPUT VOLTAGE AT ANY PIN	**-0.5V TO VDD +0.5V**
POWER DISSIPATION TQFP PACKAGE	**1.2W**
INPUT CURRENT AT ANY PIN	**+100MA**
ESD RATING (MIL-STD-883, M-3015)	**AT LEAST 1500V**

Figure 5 presents the test circuit that was used to test and measure the pulse amplitudes as listed in the ELECTRICAL CHARACTERISTICS tables.

Figure 6, Figure 7 and Figure 8 present the Pulse Template requirements for the E3, DS3 and STS-1 Rates.

FIGURE 5. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR DS3, E3 AND STS-1 RATES

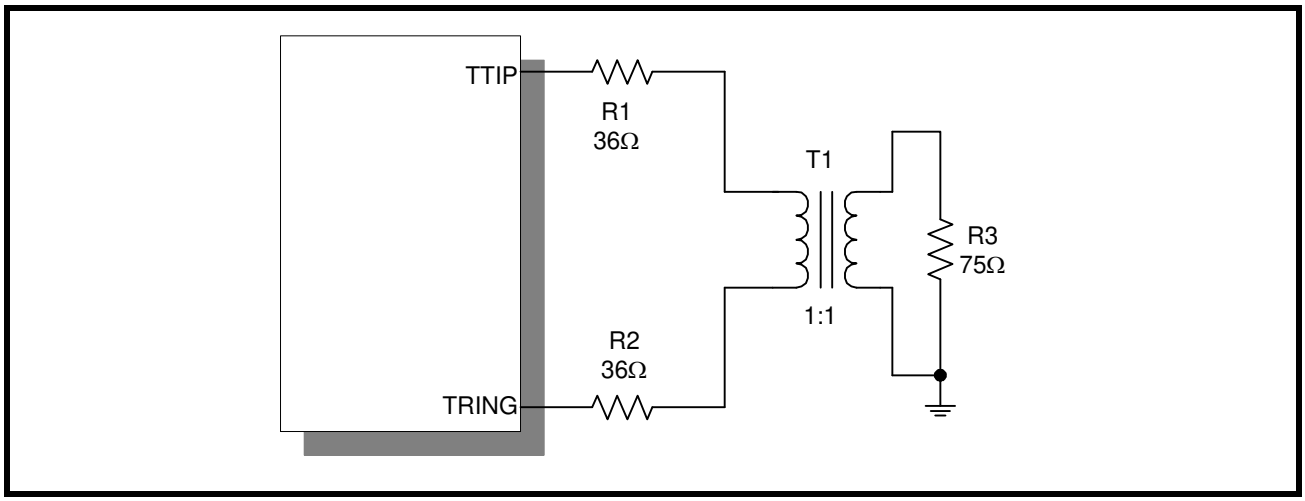


FIGURE 6. ITU-T G.703 TRANSMIT OUTPUT PULSE TEMPLATE FOR E3 APPLICATIONS

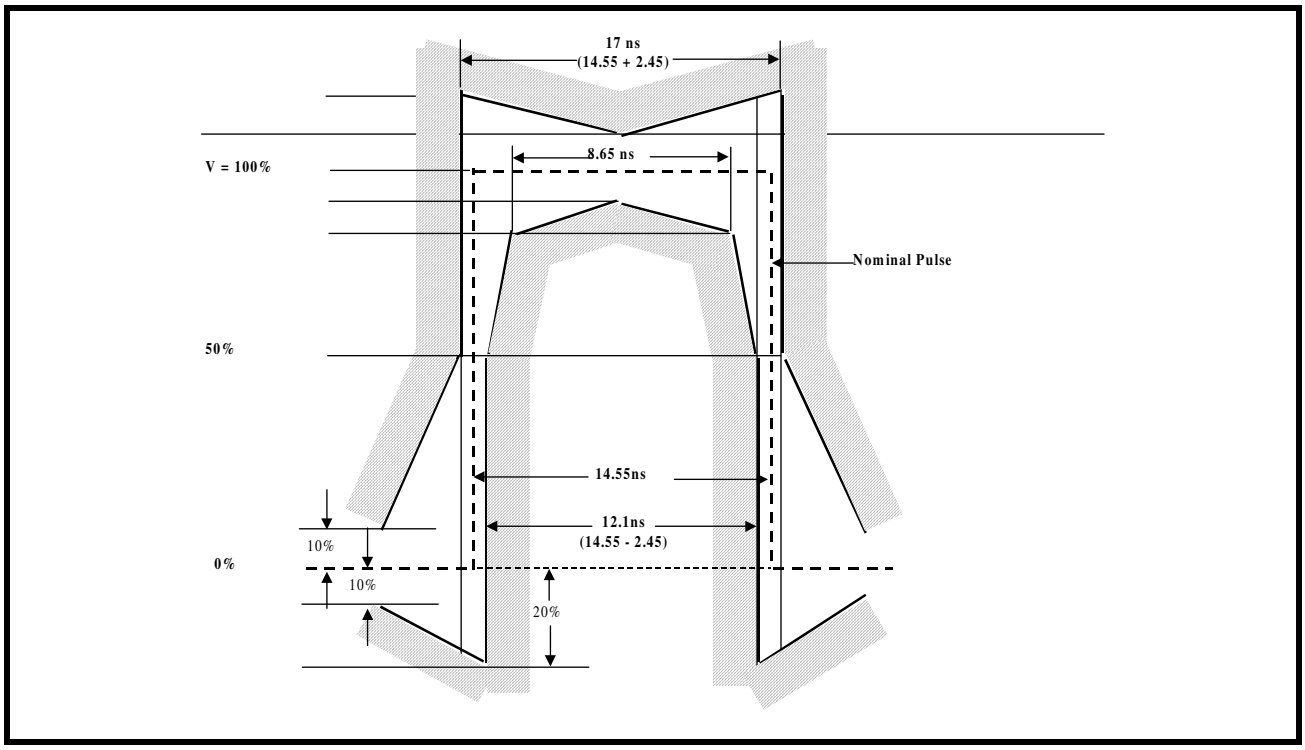


FIGURE 7. BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

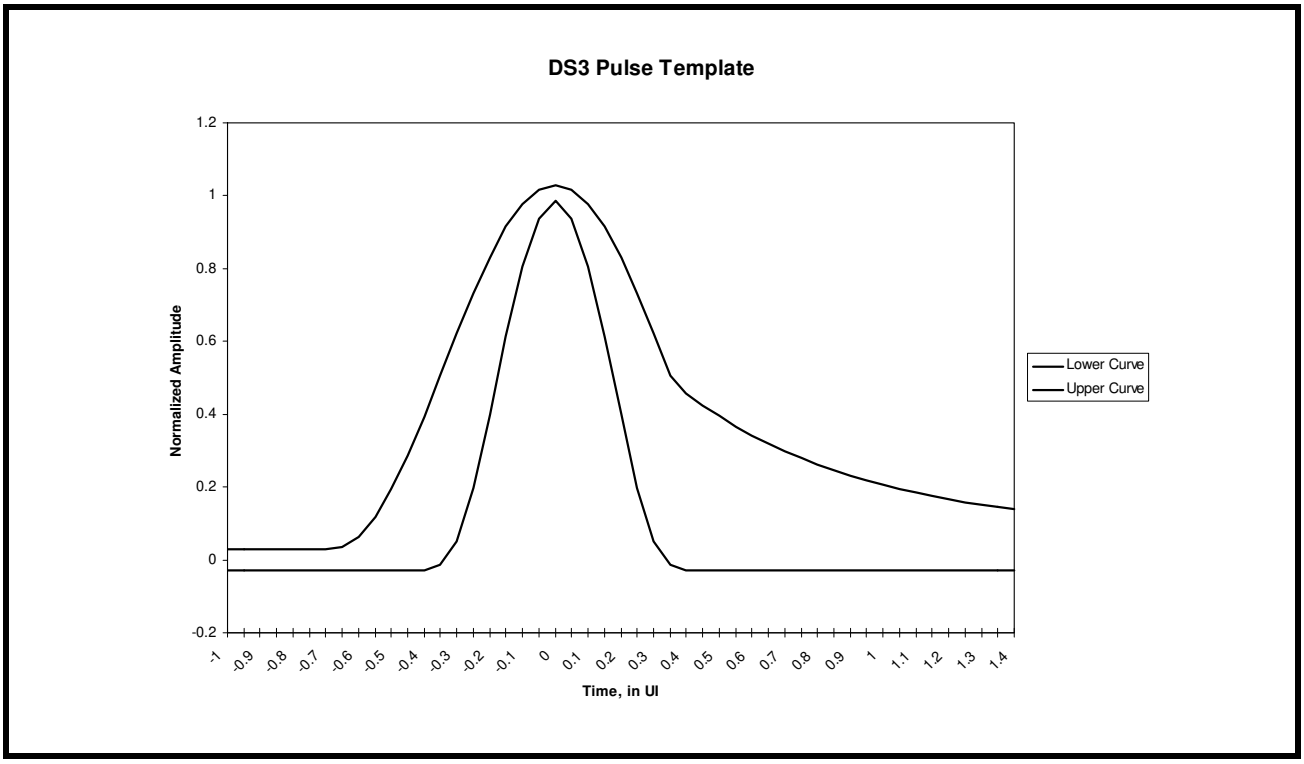
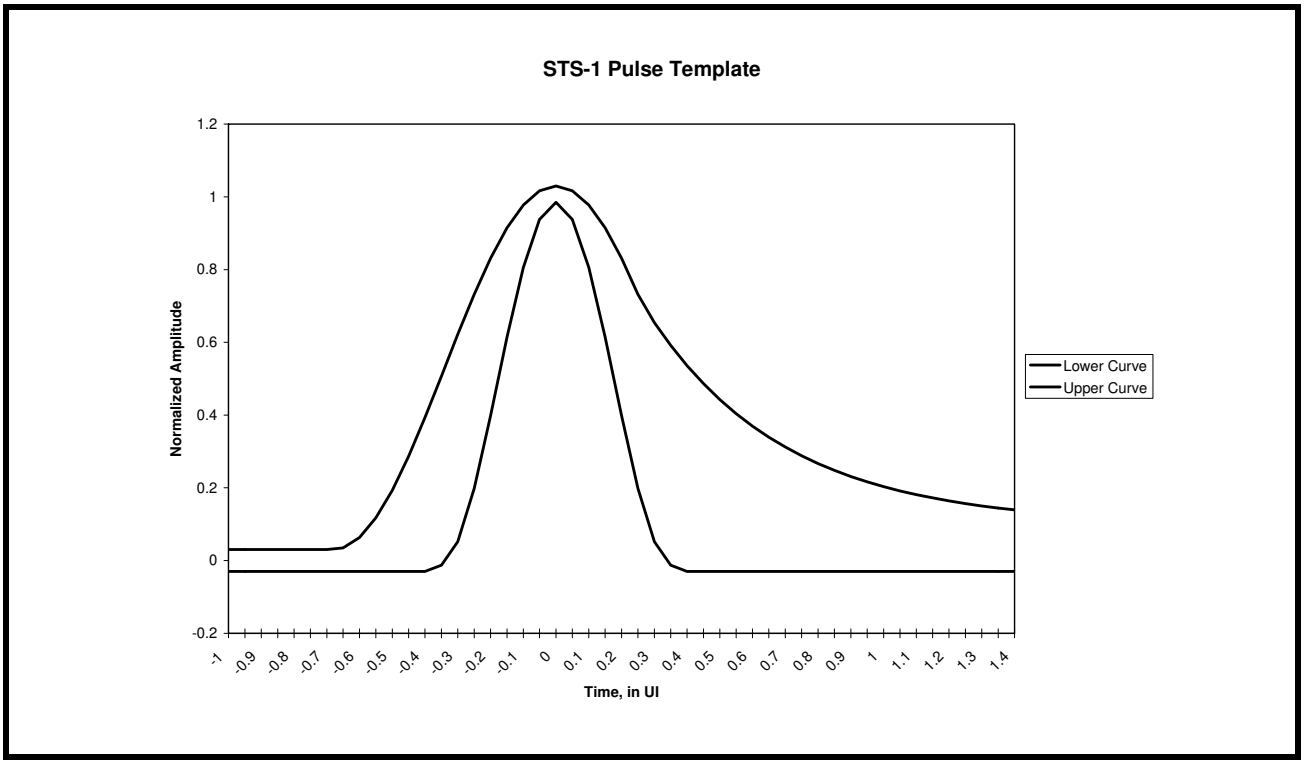


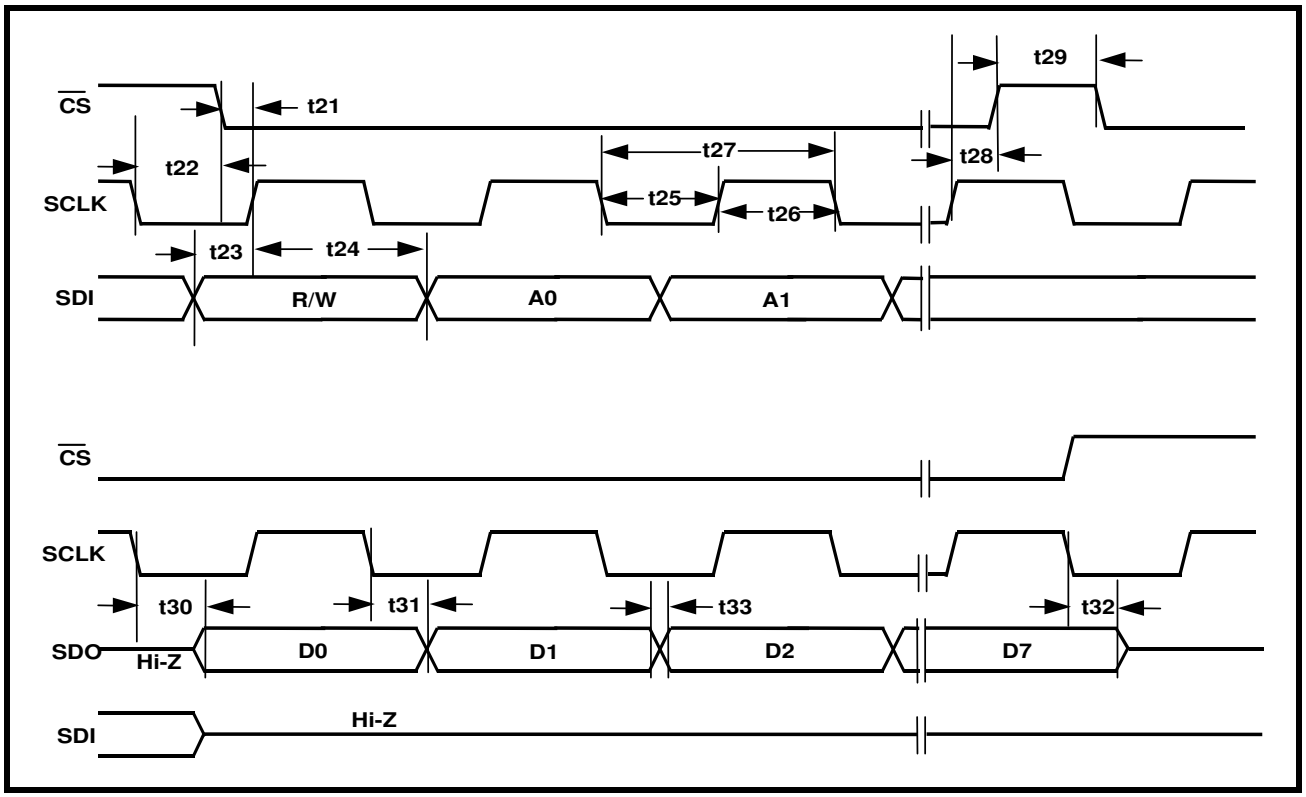
FIGURE 8. BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS



MICROPROCESSOR SERIAL INTERFACE TIMING (SEE FIGURE 9)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SCLK Setup Time	50			ns
t_{22}	$\overline{CS}$ High to Rising Edge of SCLK Hold Time	20			ns
t_{23}	SDI to Rising Edge of SCLK Setup Time	50			ns
t_{24}	SDI to Rising Edge of SCLK Hold Time	50			ns
t_{25}	SCLK “Low” Time	240			ns
t_{26}	SCLK “High” Time	240			ns
t_{27}	SCLK Period	500			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SCLK Hold Time	50			ns
t_{29}	$\overline{CS}$ Inactive Time	250			ns
t_{30}	Falling Edge of SCLK to SDO Valid Time			200	ns
t_{31}	Falling Edge of SCLK to SDO Invalid Time			100	ns
t_{32}	Falling Edge of SCLK or Rising Edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			40	ns

FIGURE 9. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



SYSTEM DESCRIPTION

A functional block diagram of the XRT7300 E3/DS3/STS-1 Transceiver IC (see Figure 1) shows that the device contains three distinct sections:

- The Transmit Section
- The Receive Section
- The Microprocessor Serial Interface

THE TRANSMIT SECTION

The Transmit Section accepts TTL/CMOS level signals from the Terminal Equipment in either a Single-Rail or Dual-Rail format. The Transmit Section then takes this data and does the following:

- Encodes the data into the B3ZS format if the DS3 or SONET STS-1 Modes have been selected or into the HDB3 format if the E3 Mode has been selected.
- Converts the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements.
- Drives these pulses onto the line via the TTIP and TRING output pins across a 1:1 Transformer.

NOTE: *The Transmit Section drives a "1" (or a Mark) on the line by driving either a positive or negative polarity pulse across the 1:1 Transformer within a given bit period. The Transmit Section drives a "0" (or a Space) onto the line by driving no pulse onto the line.*

THE RECEIVE SECTION

The Receive Section receives a bipolar signal from the line either via a 1:1 Transformer or a 0.01mF Capacitor. As the Receive Section receives this line signal it does the following:

- Adjusts the signal level through an AGC circuit.
- Optionally equalizes this signal for cable loss.
- Attempts to quantify a bit-interval within the line signal as either a “1”, “-1” or a “0” by slicing this data. This sliced data is used by the Clock Recovery PLL to recover the timing element within the line signal.
- The sliced data is routed to the HDB3/B3ZS Decoder, during which the original data content as transmitted by the Remote Terminal Equipment is restored to its original content.
- Outputs the recovered clock and data to the Local Terminal Equipment in the form of CMOS level signals via the RPOS, RNEG, RCLK1 and RCLK2 output pins.

THE MICROPROCESSOR SERIAL INTERFACE

The XRT7300 can be configured to operate in either the Hardware Mode or the HOST Mode.

The Hardware Mode

Connect the HOST/$\overline{HW}$ input pin (pin 18) to GND to configure the XRT7300 to operate in the Hardware Mode.

When the XRT7300 is operating in the Hardware Mode, the following is true:

1. The Microprocessor Serial Interface block is disabled.
2. The XRT7300 is configured via input pin settings.

Each of the pins associated with the Microprocessor Serial Interface takes on their alternative role as defined in Table 1.

3. All of the remaining input pins become active.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT7300 IS OPERATING IN THE HARDWARE MODE

PIN #	PIN NAME	FUNCTION WHILE IN THE HARDWARE MODE
11	$\overline{REGRESET}$/(RCLK2INV)	RCLK2INV
19	SDI/(LOSMUTEN)	LOSMUTEN
20	SDO/(LCV)	LCV
21	SCLK/(ENCODIS)	ENCODIS
22	CS/(DECODIS)	DECODIS
30	LCV/(RCLK2)	RCLK2

The HOST Mode

To configure the XRT7300 to operate in the HOST Mode, connect the HOST/$\overline{HW}$ input pin (pin 18) to VDD.

When the XRT7300 is operating in the HOST Mode, the following is true:

1. The Microprocessor Serial Interface block is enabled. Many configuration selections are made by writing the appropriate data into the on-chip Command Registers via the Microprocessor Serial Interface.
2. All of the following input pins are disabled:
   - Pin 1 - TXLEV
   - Pin 2 - TAOS
   - Pin 12 - REQDIS
   - Pin 14 - LLB
   - Pin 15 - RLB
   - Pin 16 - STS-1/$\overline{DS3}$
   - Pin 17 - E3
   - Pin 35 - TXOFF

Tie each of these pins to GND if the XRT7300 IC is to be operated in the HOST Mode.

Please see Section 5.0 for a detailed description on operating the Microprocessor Serial Interface or the on-chip Command Registers.

1.0 SELECTING THE DATA RATE

The XRT7300 can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Selection of the data rate is dependent on whether the XRT7300 is operating in the Hardware or HOST Mode.

TABLE 2: SELECTING THE DATA RATE FOR THE XRT7300 VIA THE E3 AND STS-1/$\overline{DS3}$ INPUT PINS (HARDWARE MODE)

DATA RATE	STATE OF E3 PIN (PIN 17)	STATE OF STS-1/$\overline{DS3}$ PIN (PIN 16)	MODE OF B3ZS/HDB3 ENCODER/ DECODER BLOCKS
E3 (34.368 Mbps)	VDD	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	VDD	B3ZS

A. When operating in the Hardware Mode.

To configure the XRT7300 for the desired data rate, the E3 and the STS-1/$\overline{DS3}$ pins must be set to the appropriate logic states shown in Table 2.

B. When operating in the HOST Mode.

To configure the XRT7300 for the desired data rate, appropriate values need to be written into the STS-1/$\overline{DS3}$ and E3 bit-fields in Command Register CR4.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$	E3	LLB	RLB
X	X	X	X	X

Table 3 relates the values of these two bit-fields with respect to the selected data rates.

TABLE 3: SELECTING THE DATA RATE FOR THE XRT7300 VIA THE STS-1/$\overline{DS3}$ AND THE E3 BIT-FIELDS WITHIN COMMAND REGISTER CR4 (HOST MODE)

SELECTED DATA RATE	STS-1/$\overline{DS3}$	E3
E3	Don't Care	1
DS3	0	0
STS-1	1	0

The results of making these selections are:

1. The VCO Center Frequency of the Clock Recovery Phase-Locked-Loop is configured to match the selected data rate.
2. The B3ZS/HDB3 Encoder and Decoder blocks are configured to support B3ZS Encoding/Decoding if the DS3 or STS-1 data rates were selected or,
3. The B3ZS/HDB3 Encoder and Decoder blocks are configured to support HDB3 Encoding/ Decoding if the E3 data rate was selected.
4. The on-chip Pulse-Shaping circuitry is configured to generate Transmit Output pulses of the correct

shape and width to meet the applicable pulse template requirement.

5. The LOS Declaration/Clearance Criteria is established.

2.0 THE TRANSMIT SECTION

Figure 1 indicates that the Transmit Section of the XRT7300 consists of the following blocks:

- Transmit Logic Block
- Duty Cycle Adjust Block
- HDB3/B3ZS Encoder
- Pulse Shaping Block

The purpose of the Transmit Section in the XRT7300 is to take TTL/CMOS level data from the terminal equipment and encode it into a format that can:

1. be efficiently transmitted over coaxial cable at E3, DS3 or STS-1 data rates.
2. be reliably received by the Remote Terminal at the other end of the E3, DS3 or STS-1 data link.
3. comply with the applicable pulse template requirements.

2.1 THE TRANSMIT LOGIC BLOCK

The purpose of the Transmit Logic Block is to accept either Dual-Rail or Single-Rail (a binary data stream) TTL/CMOS level data and timing information from the Terminal Equipment.

Accepting Dual-Rail Data from the Terminal Equipment

The XRT7300 accepts Dual-Rail data from the Terminal Equipment via the following input signals:

- TPDATA
- TNDATA
- TCLK

Figure 10 illustrates the typical interface for the transmission of data in a Dual-Rail Format between the Terminal Equipment and the Transmit Section of the XRT7300.

FIGURE 10. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT FROM THE TRANSMITTING TERMINAL EQUIPMENT TO THE TRANSMIT SECTION OF THE XRT7300

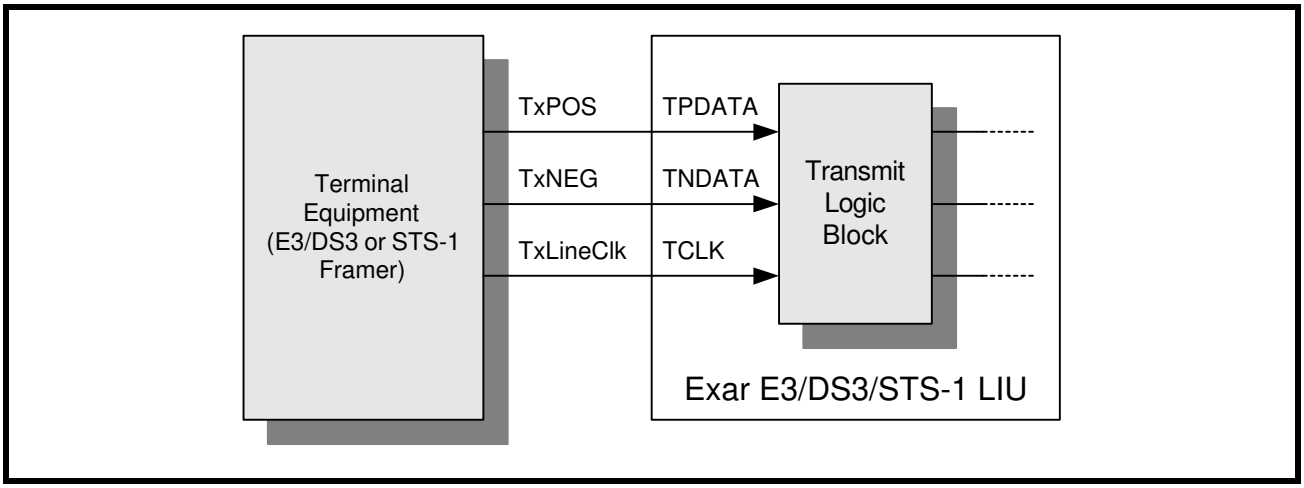
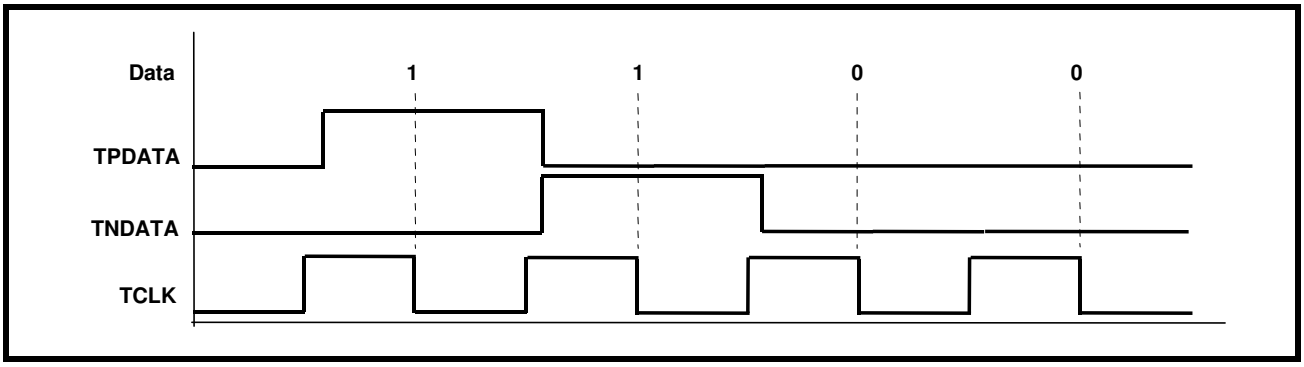


FIGURE 11. HOW THE XRT7300 SAMPLES THE DATA ON THE TPDATA AND TNDATA INPUT PINS



The manner that the LIU handles Dual-Rail data is described below and illustrated in Figure 11. The XRT7300 typically samples the data on the TPDATA and TNDATA input pins on the falling edge of TCLK.

TCLK is typically a clock signal that is of the selected data rate frequency. For the E3 data rate, TCLK is 34.368 MHz. For the DS3 data rate, TCLK is 44.736 MHz and for the SONET STS-1 rate, TCLK is 51.84 MHz. In general, if the XRT7300 samples a "1" on the TPDATA input pin, the Transmit Section of the device ultimately generates a positive polarity pulse via the TTIP and TRING output pins across a 1:1 transformer. If the XRT7300 samples a "1" on the TNDATA input pin, the Transmit Section of the device ultimately generates a negative polarity pulse via the TTIP and TRING output pins across a 1:1 transformer.

2.1.1 Accepting Single-Rail Data from the Terminal Equipment

Do the following if data is to be transmited from the Terminal Equipment to the XRT7300 in Single-Rail format (a binary data stream) without having to convert it into a Dual-Rail format.

A. Configure the XRT7300 to operate in the HOST Mode or,

B. access the Microprocessor Serial Interface and write a "1" into the TXBIN (TRANSMIT BINary) bit-field in Command Register 1.

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
X	X	X	X	1

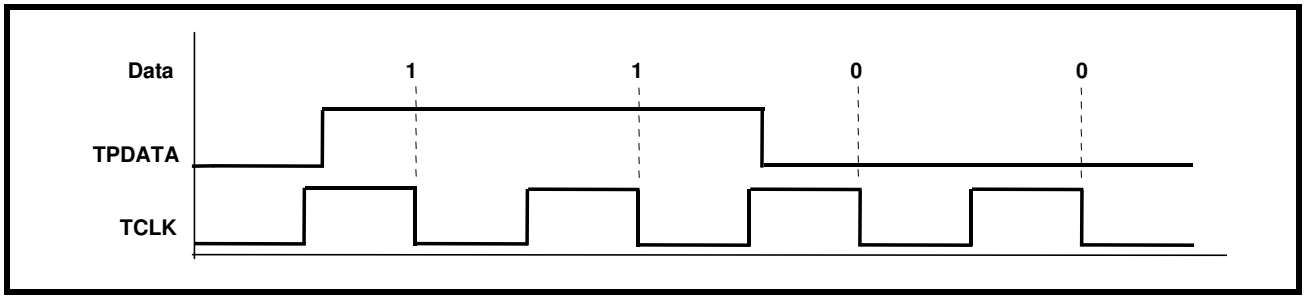
After taking these steps, the Transmit Logic Block accepts Single-Rail data via the TPDATA input pin. The XRT7300 samples this input pin on the falling edge of the TCLK clock signal and encodes it into the appropriate bipolar line signal across the TTIP and TRING output pins.

NOTES:

1. *In this mode the Transmit Logic Block ignores the TNDATA input pin.*
2. *If the Transmit Section of the XRT7300 is configured to accept Single-Rail data from the Terminal Equipment, the B3ZS/HDB3 Encoder must be enabled.*

Figure 12 illustrates the behavior of the TPDATA and TCLK signals when the Transmit Logic Block has been configured to accept Single-Rail data from the Terminal Equipment.

FIGURE 12. THE BEHAVIOR OF THE TPDATA AND TCLK INPUT SIGNALS WHILE THE TRANSMIT LOGIC BLOCK IS ACCEPTING SINGLE-RAIL DATA FROM THE TERMINAL EQUIPMENT



2.2 THE TRANSMIT CLOCK DUTY CYCLE ADJUST CIRCUITRY

The on-chip Pulse-Shaping circuitry (in the Transmit Section of the XRT7300) has the responsibility for generating pulses of the shape and width to comply with the applicable pulse template requirement. The widths of these output pulses are defined by the width of the half-period pulses in the TCLK signal.

Allowing the widths of the pulses in the TCLK clock signal to vary significantly could jeopardize the chip's ability to generate Transmit Output pulses of the appropriate width, thereby failing the applicable Pulse Template Requirement Specification. Consequently, the chips ability to generate compliant pulses could depend upon the duty cycle of the clock signal applied to the TCLK input pin.

In order to combat this phenomenon, the Transmit Clock Duty Cycle Adjust circuit was designed into the XRT7300. The Transmit Clock Duty Cycle Adjust Circuitry is a PLL that was designed to accept clock pulses via the TCLK input pin at duty cycles ranging from 30% to 70% and to regenerate these signals with a 50% duty cycle.