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GENERAL DESCRIPTION

The XRT73L06 is a six channel fully integrated Line Interface Unit (LIU) for E3/DS3/STS-1 applications. The LIU incorporates 6 independent Receivers and Transmitters in a single 217 Lead BGA package.

Each channel of the XRT73L06 can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT73L06's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12 dB of cable attenuation.

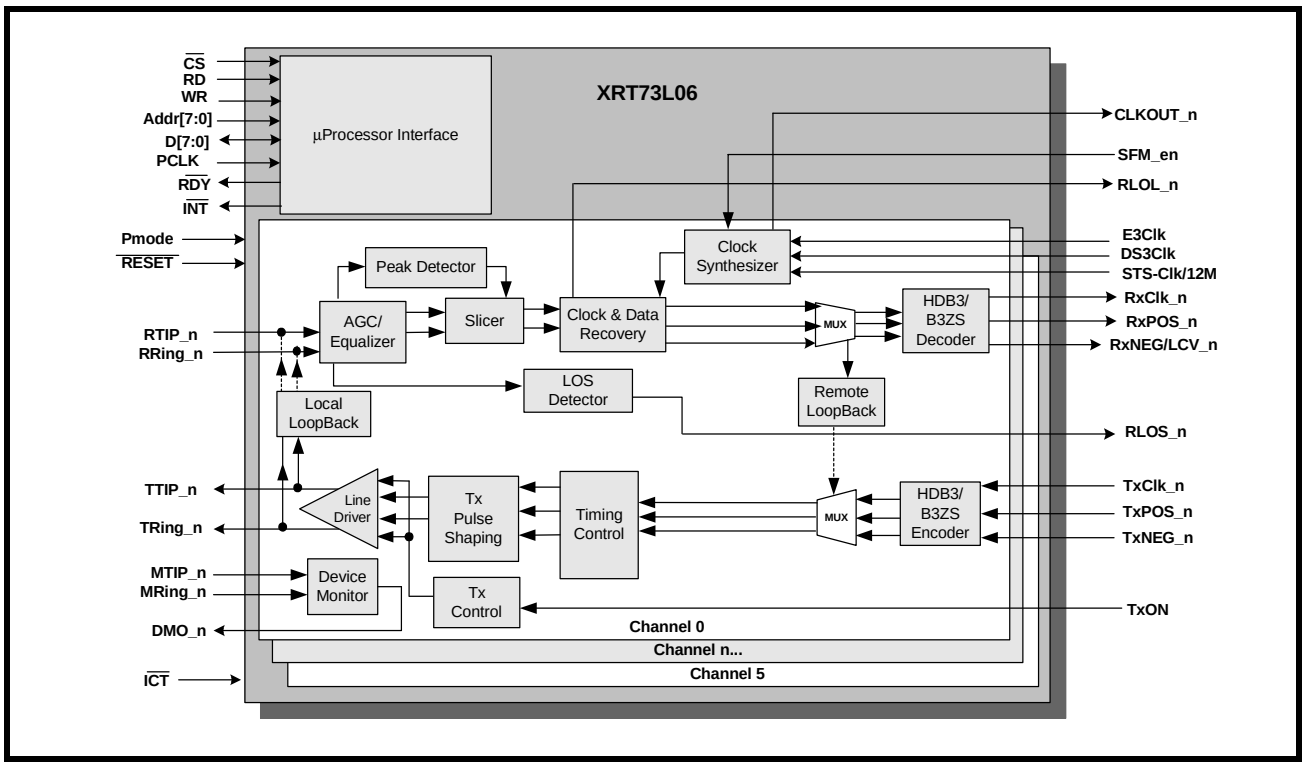
The XRT73L06 provides a Parallel Microprocessor Interface for programming and control.

The XRT73L06 supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

APPLICATIONS

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT 73L06



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73L06IB	217 Lead BGA	-40°C to +85°C

FEATURES

RECEIVER

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be turned on or off

CONTROL AND DIAGNOSTICS

- Parallel Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring
- Each channel supports Analog, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant digital inputs
- Available in 217 pin BGA Package
- - 40°C to 85°C Industrial Temperature Range

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Lock (LOL) Alarm
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

FIGURE 2. XRT73L06 IN BGA PACKAGE (BOTTOM VIEW)

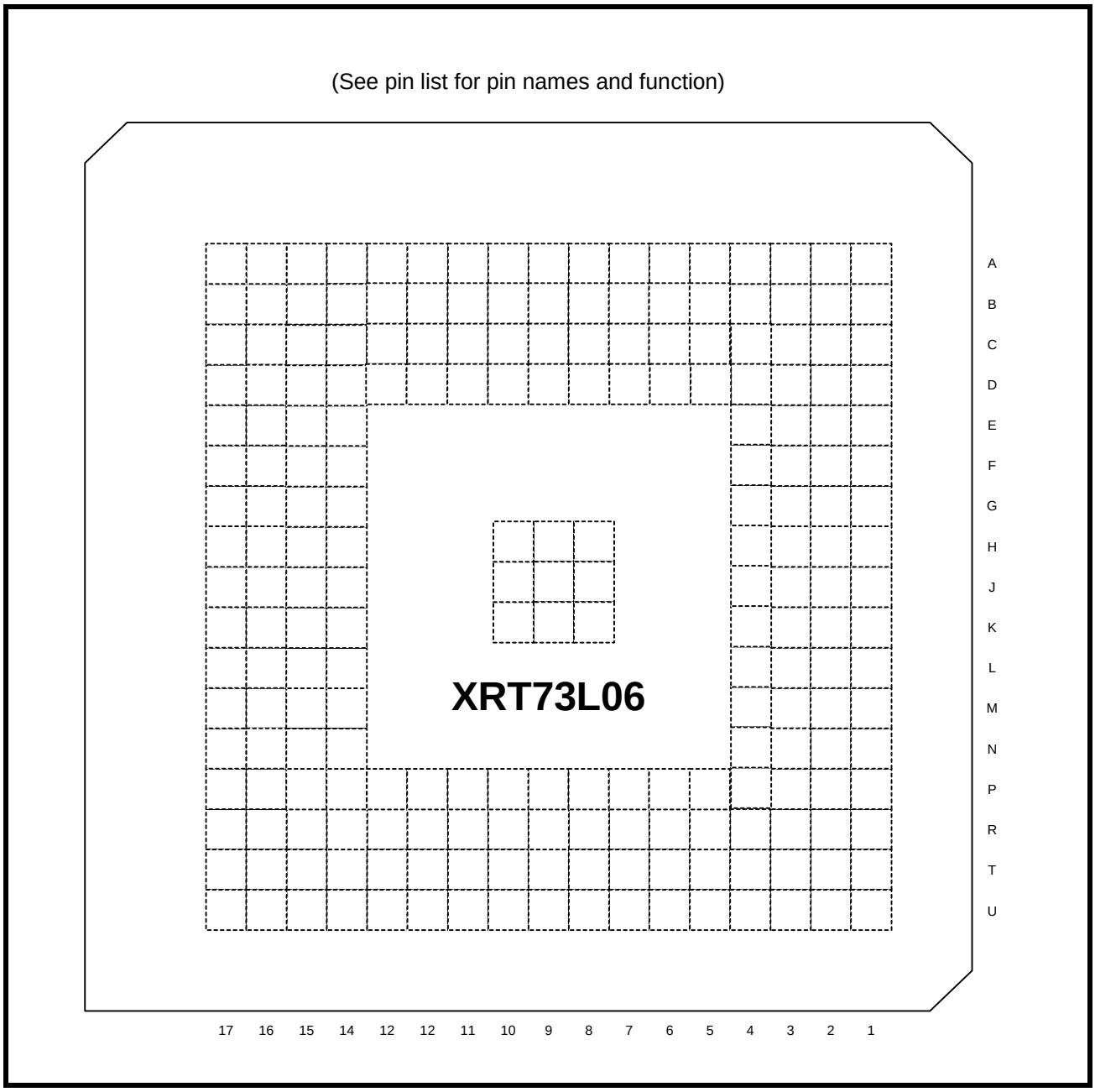


TABLE OF CONTENTS

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

<table>
<tr><th>LEAD #</th><th>SIGNAL NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>T15
R16
R15
N14
P14
P13</td><td>TxON_0
TxON_1
TxON_2
TxON_3
TxON_4
TxON_5</td><td>I</td><td>Transmitter ON Input - Channel 0:
Transmitter ON Input - Channel 1:
Transmitter ON Input - Channel 2:
Transmitter ON Input - Channel 3:
Transmitter ON Input - Channel 4:
Transmitter ON Input - Channel 5:
These pins are active only when the corresponding TxON bits are set.
Table below shows the status of the transmitter based on theTxON bit and TxON pin settings.
<table><tr><th>Bit</th><th>Pin</th><th>Transmitter Status</th></tr><tr><td>0</td><td>0</td><td>OFF</td></tr><tr><td>0</td><td>1</td><td>OFF</td></tr><tr><td>1</td><td>0</td><td>OFF</td></tr><tr><td>1</td><td>1</td><td>ON</td></tr></table>NOTES:
1. These pins will be active and can control the TTIP and TRING outputs only when the TxON_n bits in the channel register are set .
2. When Transmitters are turned off the TTIP and TRING outputs are Tri-stated.
3. These pins are internally pulled up.</td></tr>
<tr><td>E3
M3
F15
P16
G3
H15</td><td>TxCLK_0
TxCLK_1
TxCLK_2
TxCLK_3
TxCLK_4
TxCLK_5</td><td>I</td><td>Transmit Clock Input for TPOS and TNEG - Channel 0:
Transmit Clock Input for TPOS and TNEG - Channel 1:
Transmit Clock Input for TPOS and TNEG - Channel 2:
Transmit Clock Input for TPOS and TNEG - Channel 3:
Transmit Clock Input for TPOS and TNEG - Channel 4:
Transmit Clock Input for TPOS and TNEG - Channel 5:
The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%.
By default, input data is sampled on the falling edge of TxCLK.</td></tr>
</table>

TRANSMIT INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
F2 P2 G15 R17 H3 K15	TNEG_0 TNEG_1 TNEG_2 TNEG_3 TNEG_4 TNEG_5	I	**Transmit Negative Data Input - Channel 0:** **Transmit Negative Data Input - Channel 1:** **Transmit Negative Data Input - Channel 2:** **Transmit Negative Data Input - Channel 3:** **Transmit Negative Data Input - Channel 4:** **Transmit Negative Data Input - Channel 5:** In Dual-rail mode, these pins are sampled on the falling or rising edge of TxCLK_n . ***NOTES:*** *1. These input pins are ignored and must be grounded if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.*
F3 N3 F16 P15 G2 J15	TPOS_0 TPOS_1 TPOS_2 TPOS_3 TPOS_4 TPOS_5	I	**Transmit Positive Data Input - Channel 0:** **Transmit Positive Data Input - Channel 1:** **Transmit Positive Data Input - Channel 2:** **Transmit Positive Data Input - Channel 3:** **Transmit Positive Data Input - Channel 4:** **Transmit Positive Data Input - Channel 5:** By default sampled on the falling edge of TxCLK.
D1 N1 D17 N17 H1 H17	TTIP_0 TTIP_1 TTIP_2 TTIP_3 TTIP_4 TTIP_5	O	**Transmit TTIP Output - Channel 0:** **Transmit TTIP Output - Channel 1:** **Transmit TTIP Output - Channel 2:** **Transmit TTIP Output - Channel 3:** **Transmit TTIP Output - Channel 4:** **Transmit TTIP Output - Channel 5:** These pins along with TRING transmit bipolar signals to the line using a 1:1 transformer.
E1 M1 E17 M17 J1 J17	TRING_0 TRING_1 TRING_2 TRING_3 TRING_4 TRING_5	O	**Transmit Ring Output - Channel 0:** **Transmit Ring Output - Channel 1:** **Transmit Ring Output - Channel 2:** **Transmit Ring Output - Channel 3:** **Transmit Ring Output - Channel 4:** **Transmit Ring Output - Channel 5:** These pins along with TTIP transmit bipolar signals to the line using a 1:1 transformer.

RECEIVE INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
A2 U2 A17 U17 D8 P8	RxCLK_0 RXCLK_1 RxCLK_2 RxCLK_3 RxCLK_4 RxCLK_5	O	**Receive Clock Output - Channel 0:** **Receive Clock Output - Channel 1:** **Receive Clock Output - Channel 2:** **Receive Clock Output - Channel 3:** **Receive Clock Output - Channel 4:** **Receive Clock Output - Channel 5:** By default, RPOS and RNEG data sampled on the rising edge RxCLK.. Set the RxCLKINV bit to sample RPOS/RNEG data on the falling edge of RxCLK
A1 U1 A16 U16 D9 P9	RPOS_0 RPOS_1 RPOS_2 RPOS_3 RPOS_4 RPOS_5	O	**Receive Positive Data Output - Channel 0:** **Receive Positive Data Output - Channel 1:** **Receive Positive Data Output - Channel 2:** **Receive Positive Data Output - Channel 3:** **Receive Positive Data Output - Channel 4:** **Receive Positive Data Output - Channel 5:** ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled in Single-rail mode, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are removed and replaced with '0'.*
B2 T2 B16 T16 D10 P10	RNEG_0/ LCV_0 RNEG_1/ LCV_1 RNEG_2/ LCV_2 RNEG_3/ LCV_3 RNEG_4/ LCV_4 RNEG_5/ LCV_5	O	**Receive Negative Data Output/Line Code Violation Indicator - Channel 0:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 1:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 2:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 3:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 4:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 5:** In Dual Rail mode, a negative pulse is output through RNEG. **Line Code Violation Indicator - Channel n:** If configured in Single Rail mode then Line Code Violation will be output.
A5 U5 A14 U14 A9 U9	RRING_0 RRING_1 RRING_2 RRING_3 RRING_4 RRING_5	I	**Receive Input - Channel 0:** **Receive Input - Channel 1:** **Receive Input - Channel 2:** **Receive Input - Channel 3:** **Receive Input - Channel 4:** **Receive Input - Channel 5:** These pins along with RTIP receive the bipolar line signal from the remote DS3/ E3/STS-1 Terminal.

RECEIVE INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
A6	RTIP_0	I	**Receive Input - Channel 0:**
U6	RTIP_1		**Receive Input - Channel 1:**
A13	RTIP_2		**Receive Input - Channel 2:**
U13	RTIP_3		**Receive Input - Channel 3:**
A10	RTIP_4		**Receive Input - Channel 4:**
U10	RTIP_5		**Receive Input - Channel 5:**
			These pins along with RRING receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.

CLOCK INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
E15	E3CLK	I	**E3 Clock Input (34.368 MHz ± 20 ppm):** If any of the channels is configured in E3 mode, a reference clock 34.368 MHz is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
G16	DS3CLK	I	**DS3 Clock Input (44.736 MHz ± 20 ppm):** If any of the channels is configured in DS3 mode, a reference clock 44.736 MHz. is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
C16	STS-1CLK/ 12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm):** If any of the channels is configured in STS-1 mode, a reference clock 51.84 MHz is applied on this pin.. In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the channels in E3, DS3 or STS-1 modes.
L15	SFM_EN	I	**Single Frequency Mode Enable:** Tie this pin "High" to enable the Single Frequency Mode. A reference clock of 12.288 MHz ± 20 ppm is applied. In the Single Frequency Mode (SFM) a low jitter output clock is provided for each channel if the CLK_EN bit is set thus eliminating the need for a separate clock source for the framer. Tie this pin "Low" if single frequency mode is not selected. In this case, the appropriate reference clocks must be provided. ***NOTE:*** *This pin is internally pulled down*
B1 T1 B17 T17 D11 P11	CLKOUT_0 CLKOUT_1 CLKOUT_2 CLKOUT_3 CLKOUT_4 CLKOUT_5	O	**Clock output for channel 0** **Clock output for channel 1** **Clock output for channel 2** **Clock output for channel 3** **Clock output for channel 4** **Clock output for channel 5** Low jitter clock output for each channel based on the mode selection (E3,DS3 or STS-1) if the CLKOUTEN_n bit is set in the control register. This eliminates the need for a separate clock source for the framer. ***NOTES:*** *1. The maximum drive capability for the clockouts is 16 mA.* *2. This clock out is available both in SFM and non-SFM modes.*

CONTROL AND ALARM INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
B7 R6 C14 R14 C6 D14	MRING_0 MRING_1 MRING_2 MRING_3 MRING_4 MRING_5	I	**Monitor Ring Input - Channel 0:** **Monitor Ring Input - Channel 1:** **Monitor Ring Input - Channel 2:** **Monitor Ring Input - Channel 3:** **Monitor Ring Input - Channel 4:** **Monitor Ring Input - Channel 5:** The bipolar line output signal from TRING_n is connected to this pin via a 270 Ω resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled up.*
B8 R7 C13 R13 C7 D13	MTIP_0 MTIP_1 MTIP_2 MTIP_3 MTIP_4 MTIP_5	I	**Monitor Tip Input - Channel 0:** **Monitor Tip Input - Channel 1:** **Monitor Tip Input - Channel 2:** **Monitor Tip Input - Channel 3:** **Monitor Tip Input - Channel 4:** **Monitor Tip Input - Channel 5:** The bipolar line output signal from TTIP_n is connected to this pin via a 270-ohm resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled up.*
C5 T4 B12 T12 D5 B15	DMO_0 DMO_1 DMO_2 DMO_3 DMO_4 DMO_5	O	**Drive Monitor Output - Channel 0:** **Drive Monitor Output - Channel 1:** **Drive Monitor Output - Channel 2:** **Drive Monitor Output - Channel 3:** **Drive Monitor Output - Channel 4:** **Drive Monitor Output - Channel 5:** If MTIP_n and MRING_n has no transition pulse for 128 ± 32 TxCLK_n cycles, DMO_n goes “High” to indicate the driver failure. DMO_n output stays “High” until the next AMI signal is detected.
C8 T7 C12 T11 B11 R8	RLOS_0 RLOS_1 RLOS_2 RLOS_3 RLOS_4 RLOS_5	O	**Receive Loss of Signal - Channel 0:** **Receive Loss of Signal - Channel 1:** **Receive Loss of Signal - Channel 2:** **Receive Loss of Signal - Channel 3:** **Receive Loss of Signal - Channel 4:** **Receive Loss of Signal - Channel 5:** This output pin toggles "High" if the receiver has detected a Loss of Signal Condition.

CONTROL AND ALARM INTERFACE

C9 T8 D12 R11 C11 R9	RLOL_0 RLOL_1 RLOL_2 RLOL_3 RLOL_4 RLOL_5	O	**Receive Loss of Lock - Channel 0:** **Receive Loss of Lock - Channel 1:** **Receive Loss of Lock - Channel 2:** **Receive Loss of Lock - Channel 3:** **Receive Loss of Lock - Channel 4:** **Receive Loss of Lock - Channel 5:** This output pin toggles "High" if a Loss of Lock Condition is detected. LOL (Loss of Lock) condition occurs if the recovered clock frequency deviates from the Reference Clock frequency (available at either E3CLK or DS3CLK or STS-1CLK input pins) by more than 0.5%.
L16	RXA	****	**External Resistor of 3.01K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.
K16	RXB	****	**External Resistor of 3.01K Ω ±1%.** Should be connected between RxA and RxB for internal bias.
P12	$\overline{ICT}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, tie this pin "High". ***NOTE:*** *This pin is internally pulled up.*
R12	TEST	****	**Factory Test Pin** ***NOTE:*** *This pin must be connected to GND for normal operation.*

MICROPROCESSOR INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
K3	$\overline{CS}$	I	**Chip Select** Tie this “Low” to enable the communication with the Microprocessor Interface.
R1	PCLK	I	**Processor Clock Input** To operate the Microprocessor Interface, appropriate clock frequency is provided through this pin. Maximum frequency is 66 Mhz.
K2	$\overline{WR}$	I	**Write Data :** To write data into the registers, this active low signal is asserted.
L2	$\overline{RD}$	I	**Read Data:** To read data from the registers, this active low pin is asserted.
J3	$\overline{RESET}$	I	**Register Reset:** Setting this input pin "Low" resets the contents of the Command Registers to their default settings and default operating configuration ***NOTE:*** *This pin is internally pulled up.*
L3	PMODE	I	**Processor Mode Select:** When this pin is tied “High”, the microprocessor is operating in synchronous mode which means that clock must be applied to the PCLK (pin 55). Tie this pin “Low” to select the Asynchronous mode. An internal clock is provided for the microprocessor interface.

MICROPROCESSOR INTERFACE

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
T3	$\overline{RDY}$	O	**Ready Acknowledge:** ***NOTE:*** *This pin must be connected to VDD via 3 kΩ ± 1% resistor.*
U3	$\overline{INT}$	O	**INTERRUPT Output:** A transition to "Low" indicates that an interrupt has been generated. The interrupt function can be disabled by clearing the interrupt enable bit in the Channel Control Register**.** ***NOTES:*** *1. This pin will remain asserted "Low" until the interrupt is serviced.* *2. This pin must be conneced to VDD via 3 kΩ ± 1% resistor.*
B4 A3 B3 C4 C3 C2 D3 D4	ADDR[0] ADDR[1] ADDR[2] ADDR[3] ADDR[4] ADDR[5] ADDR[6] ADDR[7]	I	**ADDRESS BUS:** 8 bit address bus for the microprocessor interface
N4 P3 P4 P5 R5 R4 R3 R2	D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	**DATA BUS:** 8 bit Data Bus for the microprocessor interface

ANALOG POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
E2	TxAVDD_0	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 0**
N2	TxAVDD_1	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 1**
E16	TxAVDD_2	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 2**
N16	TxAVDD_3	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 3**
J2	TxAVDD_4	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 4**
J16	TxAVDD_5	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 5**
D2	TxAGND_0	****	**Transmitter Analog GND - Channel 0**
M2	TxAGND_1	****	**Transmitter Analog GND - Channel 1**
D16	TxAGND_2	****	**Transmitter Analog GND - Channel 2**
M16	TxAGND_3	****	**Transmitter Analog GND - Channel 3**
H2	TxAGND_4	****	**Transmitter Analog GND - Channel 4**
H16	TxAGND_5	****	**Transmitter Analog GND - Channel 5**
A4	RxAVDD_0	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 0**
U4	RxAVDD_1	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 1**
A15	RxAVDD_2	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 2**
U15	RxAVDD_3	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 3**
A8	RxAVDD_4	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 4**
U8	RxAVDD_5	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 5**
A7	RxAGND_0	****	**Receiver Analog GND - Channel_0**
U7	RxAGND_1	****	**Receive Analog GND - Channel 1**
A12	RxAGND_2	****	**Receive Analog GND - Channel 2**
U12	RxAGND_3	****	**Receive Analog GND - Channel 3**
A11	RxAGND_4	****	**Receive Analog GND - Channel 4**
U11	RxAGND_5	****	**Receive Analog GND - Channel 5**
E4	JaAVDD_0	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 0**
K4	JaAVDD_1	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 1**
E14	JaAVDD_2	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 2**
K14	JaAVDD_3	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 3**
G4	JaAVDD_4	****	**Analog 3.3 V ± 5% VDD - Jitter Attenuator Channel 4**
G14	JaAVDD_5	****	**Analog 3.3 V ± 5% VDD - Jitter attenuator Channel 5**
F4	JaAGND_0	****	**Analog GND - Jitter Attenuator Channel 0**
J4	JaAGND_1	****	**Analog GND - Jitter Attenuator Channel 1**

ANALOG POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
F14	JaAGND_2	****	**Analog GND - Jitter Attenuator Channel 2**
J14	JaAGND_3	****	**Analog GND - Jitter Attenuator Channel 3**
H4	JaAGND_4	****	**Analog GND - Jitter Attenuator Channel 4**
H14	JaAGND_5	****	**Analog GND - Jitter Attenuator Channel 5**
C10	AGND	****	**Analog GND**
R10	AGND	****	**Analog GND**
H9	AGND	****	**Analog GND**
J9	AGND	****	**Analog GND**
K9	AGND	****	**Analog GND**
N15	REFAVDD	****	**Analog 3.3 V ± 5% VDD - Reference**
M15	REFGND	****	**Reference GND**

DIGITAL POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
F1	TxVDD_0	****	**Transmitter 3.3 V ± 5% VDD Channel 0**
L1	TxVDD_1	****	**Transmitter 3.3 V ± 5% VDD Channel 1**
F17	TxVDD_2	****	**Transmitter 3.3 V ± 5% VDD Channel 2**
L17	TxVDD_3	****	**Transmitter 3.3 V ± 5% VDD Channel 3**
K1	TxVDD_4	****	**Transmitter 3.3 V ± 5% VDD Channel 4**
K17	TxVDD_5	****	**Transmitter 3.3 V ± 5% VDD Channel 5**
C1	TxGND_0	****	**Transmitter GND - Channel 0**
P1	TxGND_1	****	**Transmitter GND - Channel 1**
C17	TxGND_2	****	**Transmitter GND - Channel 2**
P17	TxGND_3	****	**Transmitter GND - Channel 3**
G1	TxGND_4	****	**Transmitter GND - Channel 4**
G17	TxGND_5	****	**Transmitter GND - Channel 5**
B5	RxDVDD_0	****	**Receiver 3.3 V ± 5% VDD - Channel 0**
T5	RxDVDD_1	****	**Receiver 3.3 V ± 5% VDD - Channel 1**
B14	RxDVDD_2	****	**Receiver 3.3 V ± 5% VDD - Channel 2**
T14	RxDVDD_3	****	**Receiver 3.3 V ± 5% VDD - Channel 3**
B9	RxDVDD_4	****	**Receiver 3.3 V ± 5% VDD - Channel 4**
T9	RxDVDD_5	****	**Receiver 3.3 V ± 5% VDD - Channel 5**
B6	RxDGND_0	****	**Receiver Digital GND - Channel 0**
T6	RxDGND_1	****	**Receiver Digital GND - Channel 1**
B13	RxDGND_2	****	**Receiver Digital GND - Channel 2**
T13	RxDGND_3	****	**Receiver Digital GND - Channel 3**
B10	RxDGND_4	****	**Receiver Digital GND - Channel 4**
T10	RxDGND_5	****	**Receiver Digital GND - Channel 5**
P6	DVDD_1	****	**VDD 3.3 V ± 5%**
C15	DVDD_2	****	**VDD 3.3 V ± 5%**
L4	JaDVDD_1	****	**VDD 3.3 V ± 5%**
D6	DVDD(uP)	****	**VDD 3.3 V ± 5%**
L14	JaDVDD_2	****	**VDD 3.3 V ± 5%**
D15	DGND_1	****	**Digital GND**
D7	DGND(uP)	****	**Digital GND**
M14	JaDGND_2	****	**Digital GND**

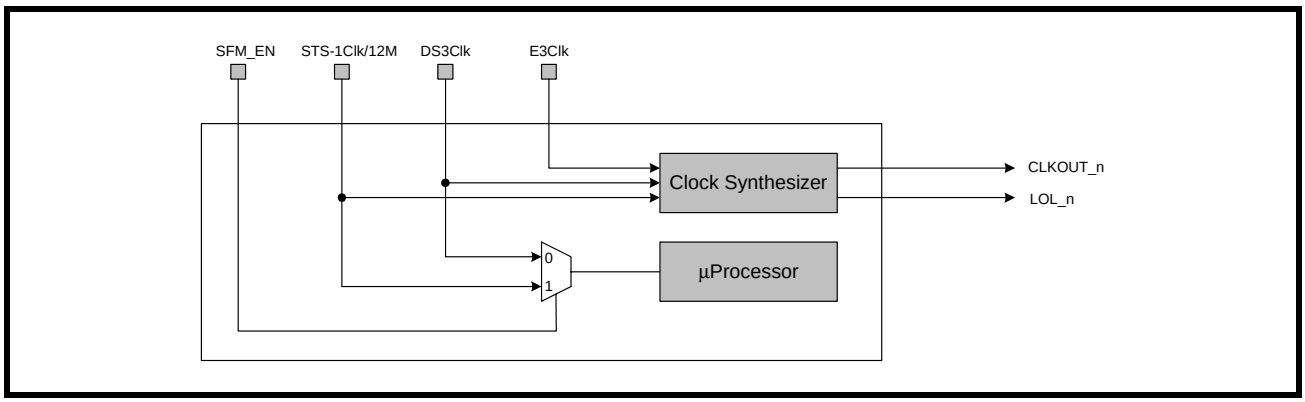
DIGITAL POWER AND GROUND

LEAD #	SIGNAL NAME	TYPE	DESCRIPTION
M4	JaDGND_1	****	**Digital GND**
P7	DGND	****	**Digital GND**
H8	DGND	****	**Digital GND**
J8	DGND	****	**Digital GND**
K8	DGND	****	**Digital GND**
H10	DGND	****	**Digital GND**
J10	DGND	****	**Digital GND**
K10	DGND	****	**Digital GND**

1.0 CLOCK SYNTHESIZER

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS-3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS-3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS-3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS-3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 3

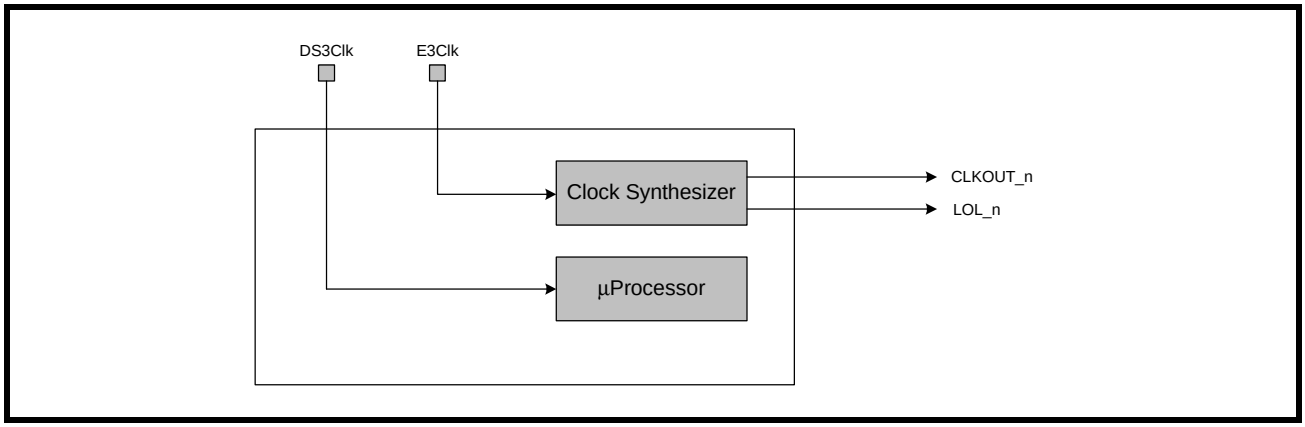
FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR



1.1 Clock Distribution

Network cards that are designed to support multiple line rates which are not configured for single frequency mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS-3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. If however, multiple line rates will not be supported, i.e. E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.

FIGURE 4. CLOCK DISTRIBUTION CONGIFURED IN E3 MODE WITHOUT USING SFM

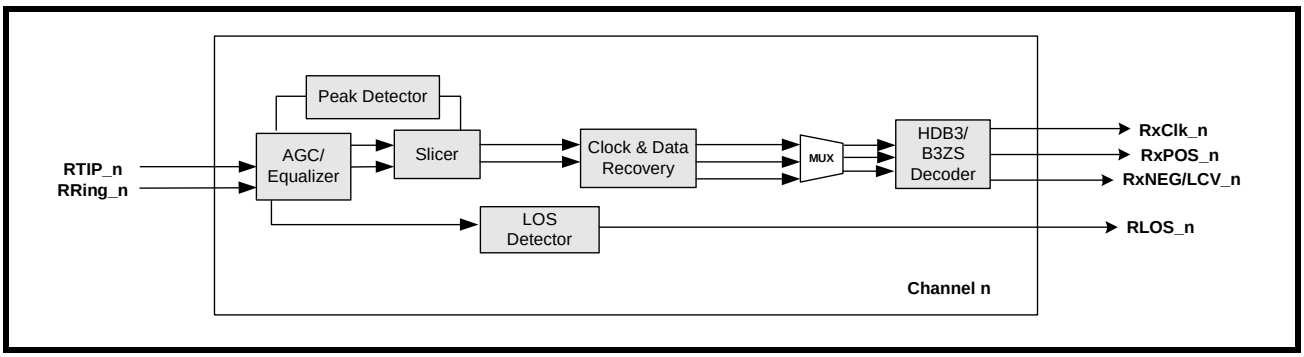


NOTE: *For one input clock reference, the single frequency mode should be used.*

2.0 THE RECEIVER SECTION

The receiver is designed so that the LIU can recover clock and data from an attenuated line signal caused by cable loss or flat loss according to industry specifications. Once data is recovered, it is processed and presented at the receiver outputs according to the format chosen to interface with a Framer/Mapper or ASIC. This section describes the detailed operation of various blocks within the receive path. A simplified block diagram of the receive path is shown in Figure 5.

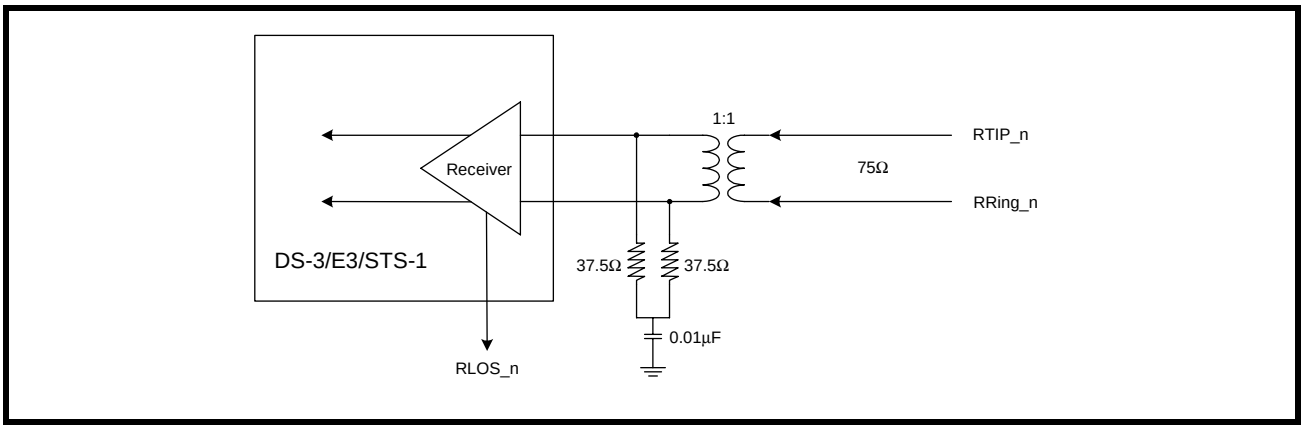
FIGURE 5. RECEIVE PATH BLOCK DIAGRAM



2.1 Receive Line Interface

Physical Layer devices are AC coupled to a line interface through a 1:1 transformer. The transformer provides isolation and a level shift by blocking the DC offset of the incoming data stream. The typical medium for the line interface is a 75Ω coxial cable. Whether using E3, DS-3 or STS-1, the LIU requires the same bill of materials, see Figure 6.

FIGURE 6. RECEIVE LINE INTERFACECONNECTION



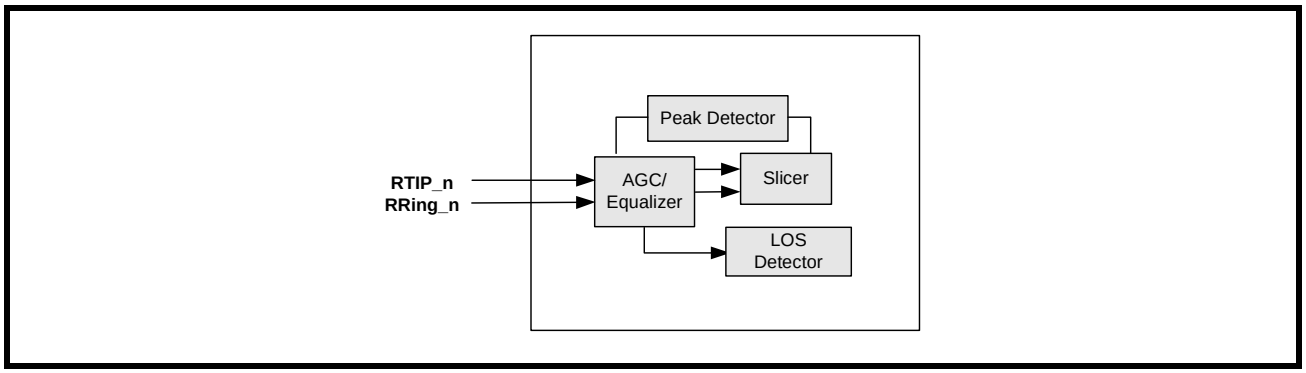
2.2 Adaptive Gain Control (AGC)

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB. The peak detector provides feedback to the equalizer before slicing occurs.

2.3 Receive Equalizer

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data. The equalizer can be disabled by programming the appropriate register.

FIGURE 7. ACG/EQUALIZER BLCOK DIAGRAM



2.3.1 Recommendations for Equalizer Settings

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/ STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be enabled. However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be disabled for cable length less than 300 feet. This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics. The Equalizer also contains an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. The equalizer gain mode can be enabled by programming the appropriate register.

NOTE: *The results of extensive testing indicate that even when the Equalizer was enabled, regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.*

2.4 Clock and Data Recovery

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder. The Clock Recovery PLL can be in one of the following two modes:

2.4.1 Data/Clock Recovery Mode

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

2.4.2 Training Mode

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin “High” or setting the RLOL_n bit to “1” in the control register. Also, the clock output on the RxClk_n pins are the same as the reference channel clock.

2.5 LOS (Loss of Signal) Detector

2.5.1 DS3/STS-1 LOS Condition

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to "1" in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses. Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 1.The status of the ALOS condition is reflected in the ALOS_n status control register. RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled "High" and the RLOS_n bit is set to "1" in the status control register.

TABLE 1: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS DEFECT	SIGNAL LEVEL TO CLEAR ALOS DEFECT
DS3	0	0	< 75mVpk	> 130mVpk
	1	0	< 45mVpk	> 60mVpk
	0	1	< 120mVpk	> 45mVpk
	1	1	< 55mVpk	> 180mVpk
STS-1	0	0	< 120mVpk	> 170mVpk
	1	0	< 50mVpk	> 75mVpk
	0	1	< 125mVpk	> 205mVpk
	1	1	< 55mVpk	> 90mVpk

2.5.2 Disabling ALOS/DLOS Detection

For debugging purposes it is useful to disable the ALOS and/or DLOS detection. Writing a "1" to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

2.5.3 E3 LOS Condition:

If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal is defined as no transitions for 10 to 255 consecutive zeros. No transitions is defined as a signal level between 15 and 35 dB below the normal. This is illustrated in Figure 8. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 9 shows the LOS declaration and clearance conditions.

FIGURE 8. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775

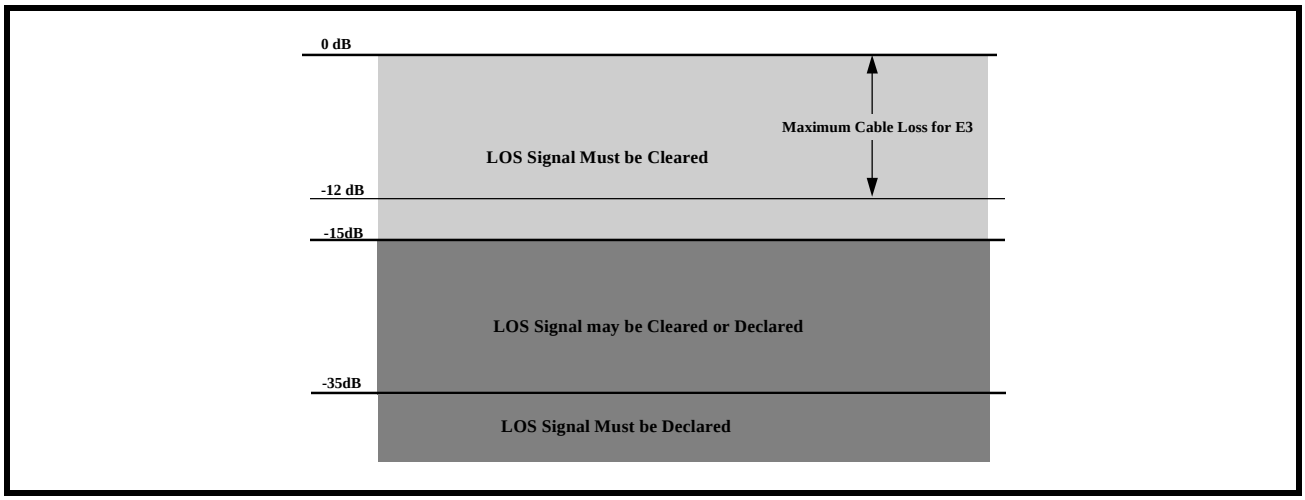
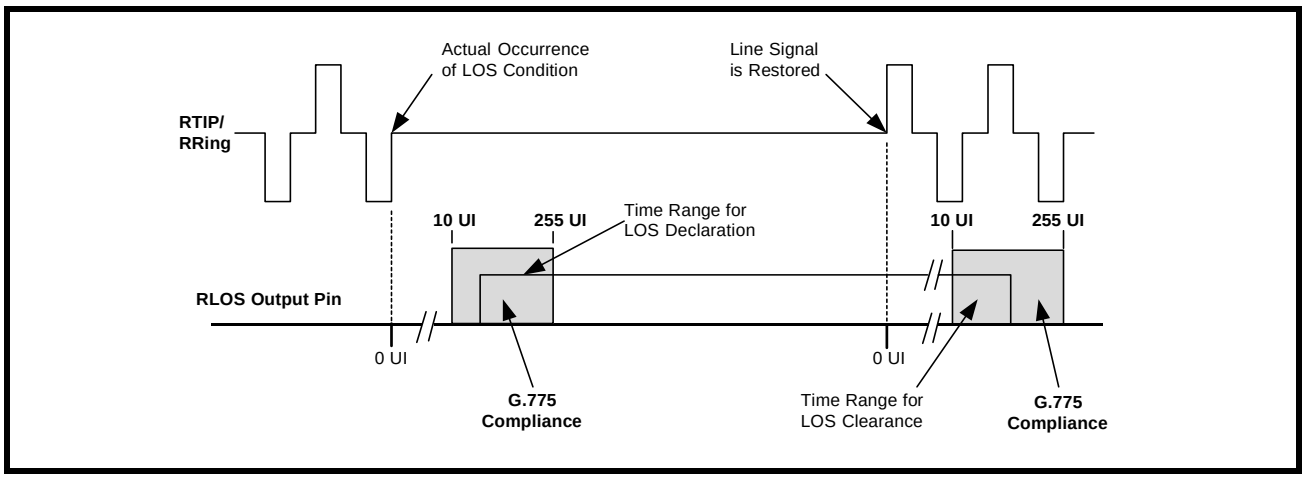


FIGURE 9. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



2.5.4 Interference Tolerance

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 10 shows the configuration to test the interference margin for DS3/ STS1. Figure 11 shows the set up for E3.

FIGURE 10. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

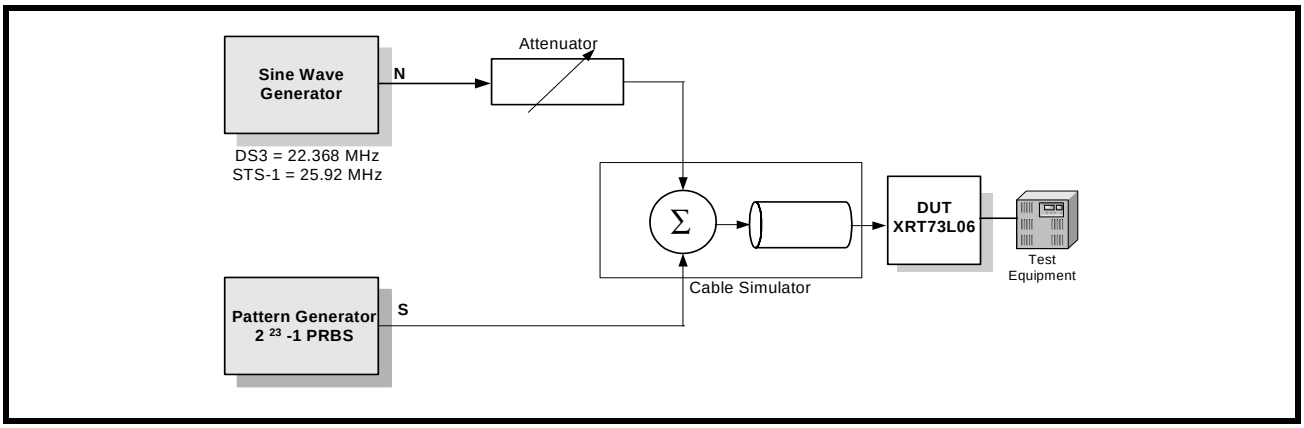


FIGURE 11. INTERFERENCE MARGIN TEST SET UP FOR E3.

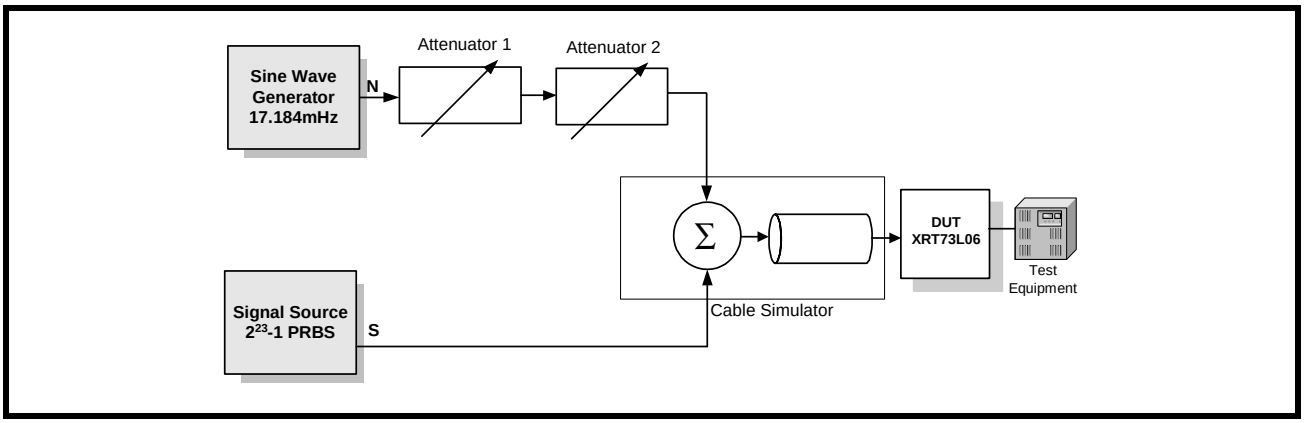


TABLE 2: INTERFERENCE MARGIN TEST RESULTS

MODE	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
E3	0 dB	Equalizer “IN”
		-17 dB
	12 dB	-14 dB
DS3	0 feet	-15 dB
	225 feet	-15 dB
	450 feet	-14 dB
STS-1	0 feet	-15 dB
	225 feet	-14 dB
	450 feet	-14 dB